



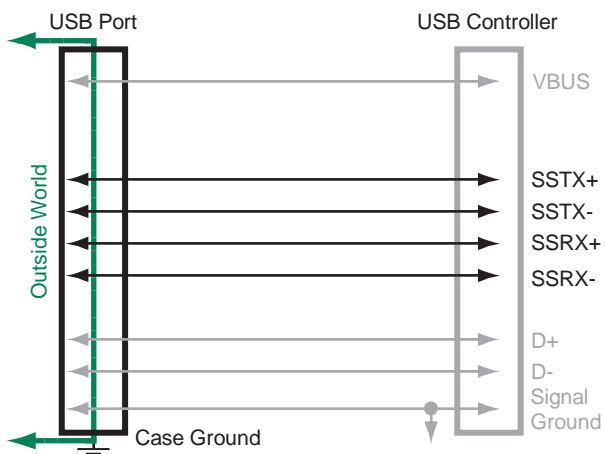
Released in 1996 to standardize connection between computer peripherals, Universal Serial Bus (USB) is expected to ship in more than 3 billion devices in 2011.

In 2010, the first devices with USB 3.0 were introduced, reaching about 100 million units. This number will begin to increase rapidly after 2011 as more chipsets incorporate the new standard

USB 3.0 devices incorporate four additional data channels providing 5Gbps communication speeds and 900mA max current on Vbus. These new USB 3.0 specifications combined with continuous shrinkage of integrated chip geometries, makes protection against electrical transients and overcurrent faults more critical and more complicated. The stakes are higher from smaller electrostatic discharge (ESD) and short circuit events.

With the faster throughput and chip sensitivity, signal integrity and system reliability should be of greater concern for systems designers. Parasitic capacitance, low clamping voltage and low resistance become key criteria in circuit protection component selection. Due to the higher currents available on Vbus, the low resistance of the overcurrent protector also becomes critical to ensure low voltage drop.

Understanding key selection criteria and tradeoffs between protection technologies (PTCs, varistors, and polymer and silicon-based devices) is key to achieving successful design. This article explains consideration factors and issues in detail.



**Fig.1 USB 3.0 adds dual differential data pairs.**

## USB 3.0 Operating Characteristics

Universal Serial Bus (USB) is a set of interface specifications for high speed wired communication between electronic systems. The USB 3.0 standard specifies increased data transfer rates, increased power output, and backward compatibility with USB 2.0.

The most significant physical change from USB 2.0 to USB 3.0 has been the introduction of two differential data pairs called SSRx+/SSRx- and SSTx+/SSTx- to run in parallel with the existing D-/D+ data bus. This allows full duplex simultaneous transfer of data as opposed to the single duplex unidirectional USB 2.0 bus.

Also the increase in available current from 500mA to 900mA expands the options for powering external devices, eliminating the need for extra power supplies.

## USB 3.0 Circuit Protection Challenges

With the increase in data transfer rate to 5 Gbits/s and required decrease in channel capacitance in order support the new data rate, ESD protection used in previous generations of USB maybe inadequate for use with USB 3.0. Designers are more challenged with finding voltage transient protection solutions that can protect sensitive data lines without adding signal distorting capacitance.

The introduction of additional differential data pairs requires more data lines to be protected against ESD than USB 2.0 and discrete ESD protection solutions used in the past to protect each individual data line may not be the ideal solution. New silicon array ESD protection devices, which are placed directly on the data pairs, not only protect legacy USB 2.0 data lines but also these additional data signal pairs.

For over-current protection, USB 3.0 Specification Section 11.4.1.1.1 states:

The host and all self-powered hubs must implement over-current protection for safety reasons, and the hub must have a way to detect the over-current condition and report it to the USB software.

The over-current limiting mechanism must be resettable without user mechanical intervention. Polymeric PTCs and solid-state switches are examples of methods that can be used for over-current limiting.

Overcurrent protection may also be required in some equipment per UL60950-1.

## Overcurrent Protection

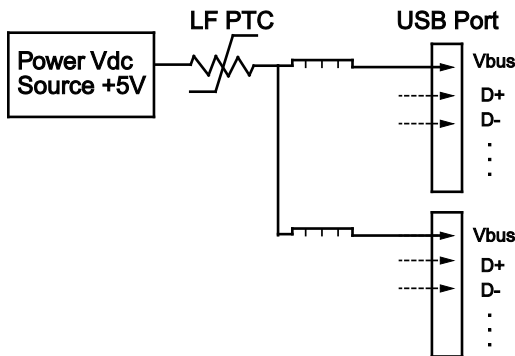
USB Bus Transceiver ICs (integrated circuits) or Power Management ICs may include some current limiting functions, however, when the ICs do not include current limiting features, or when supplemental protection is required, the circuit designer must use current limiting PTCs for the Vbus.

Installing a Polymeric PTC device on the USB Vbus (see figure 7) limits current in the event of a short circuit, and prevents overcurrent damage caused by a sudden short circuit downstream. It may also help achieve UL60950-1 compliance to Sec 2.5 (Limited Power Source, Table 2B), which states that short circuit current must be limited to less than 8A in 5 sec.

Related to USB hub applications, the USB 3.0 over-current protection specification 11.4.1.1.1 states:

Should the aggregate current drawn by a gang of downstream facing ports exceed a preset value, the over-current protection circuit removes or reduces power from all affected downstream facing ports. The preset value cannot exceed 5.0 A and must be sufficiently higher than the maximum allowable port current or time delayed such that transient currents.

Figure 2 below shows a PTC solution for multi-port hub configuration. For single port configurations see figures 7 and 8 later in this document.



**Fig.2 USB 3.0 multi-port hub configuration (See also Fig 7 & 8)**

The following table shows the recommended PTC parts for both single port and two ports ganged configurations. We have also identified the PTC solution for the new USB battery charging specification Rev 1.2.

**Fig.3 Littelfuse PTC products recommended for USB 3.0**

Number of USB 3.0 Ports	Littelfuse p/n	Footprint	Vmax (Vdc)	Ihold 20°C (A)	Ihold 60C (A)	8A trip (sec), 20°C	R1max (ohms)
1	0603L150SLYR	0603	6	1.5	0.95	0.5	0.08
1	1210L200SLYR	1210	6	2	1.29	3	0.024
2	1206L350SLYR	1206	6	3.5	2.19	5	0.018
Battery Charging 1.2 (1 port)	1206L260SLTHYR	1206	6	2.6	1.65	4	0.026

When selecting a PTC for USB port protection, one needs to consider a few key parameters:

1. Max port current (USB 3.0 is 900mA)
2. Operating temperature at the PTC location
3. Trip speed
4. DC Resistance

The PTCs in figure 3 have been selected for their optimal fit to USB 3.0 port protection. All the PTCs are capable of holding the max USB 3.0 port current of 900mA per port without tripping at max operating temperature of 60°C. PTCs de-rate due to temperature dramatically so this is an important aspect of selecting the PTC. Designers should also consider non-compliant USB 3.0 devices that draw more than 900mA when selecting the PTC. The hold current at max operating temperature needs to be above the max available current if drawing more than 900mA. Otherwise, the PTC has the possibility of nuisance tripping the port.

Each PTC is capable of tripping in less than 5 sec for an 8A short circuit fault. This is important in meeting the UL60950-1 Limited Power Source specification as well as the 5A current limit in the USB 3.0 Specification.

The last remaining critical parameter in selecting the optimal PTC is DC resistance. Since USB 3.0 is now running at 900mA max current, power dissipation in the circuit becomes critical and needs to be minimized. Also, the voltage drop across the components on Vbus needs to be minimized especially if the circuit has a tight resistance budget. The PTCs shown in figure 3 all are made of the Lo-Rho resistivity PTC formulation and are optimal for the USB 3.0 application.

The main objective in selecting a PTC is ensuring that the hold current for the device is at least 0.9A at design temperature. We have selected 60°C as worst case for the products shown in figure 3. For 1 port applications, the optimal choice is part number 0603L150SLYR as it is the smallest form-factor available that can still support the required amount of current (0.95A) at max design temperature 60°C.

For situations where the design requires more margin on hold current, part number 1210L200SLYR is a good choice since it holds 1.29A at 60°C. For 2 port applications where the designer can gang two ports together (total 1.8A output) and use one PTC to protect both ports, part number 1206L350SLYR is a good choice since it can hold 2.19A at 60°C. All the suggested parts are capable of tripping in < 5 sec at 8A fault current so all safety considerations are met.

## Electrostatic Discharge (ESD) Protection

The additional data pairs of USB 3.0 expose systems to greater ESD threats because it provides more possible sources for transients to transfer.

Interfaces such as USB 3.0 can be exposed to ESD by someone touching any of the pins on the connector or any of the pins on an open-ended cable connected to one of the ports. Even though modern IC chips often have some degree of protection (usually between 500V to 2kV), these ESD levels are based on the MIL-STD HBM model with 1500 ohms of resistance. With the MIL-STD model, 2kV is closer to the IEC model at 500V, which uses the 330ohm resistor.

ESD events often can reach 15kV or more and cause soft failures, latent damage or catastrophic failure. Supplemental ESD protection is needed to enhance the survivability of today's modern interface ports. To determine the immunity of systems to external ESD events, several test standards have been developed, with the International Electrotechnical Commission(IEC) 61000-4-2 being most widely recognized. This standard defines ESD test levels which relate to different environmental and installation conditions and establishes test procedures. Today's high speed USB 3.0 ports must be able to survive a direct contact ESD of at least 8kV, which is also an IEC 61000-4-2 level 4 requirement.

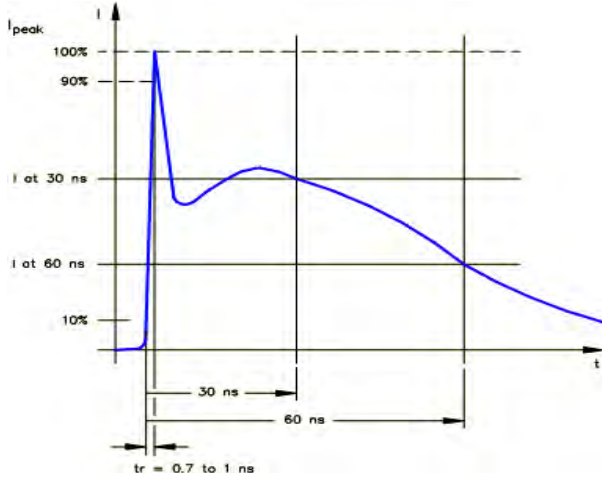


Fig. 4 IEC 61000-4-2 ESD current waveform

With the higher data rates particular attention needs to be paid to capacitance of the components selected to protect the circuitry. Device resistance power draw and size and configuration of devices should also be of concern to systems designers.

Important parameters to consider include:

- Dynamic resistance
- Off- state impedance
- Multiple pulse capability
- Parasitic capacitance
- Package geometry
- Voltage drop
- Resistance and power dissipation
- Device size, configuration and board space

Several different ESD suppression technologies such as MLVs (Multi-layer varistors), polymer ESD suppressors and silicon are available on the market today and selecting the right protection will determine whether a USB 3.0 port will survive a discharge event or not.

Designers must be especially mindful of device capacitance, clamping voltage and dynamic resistance as these parameters are critical in selecting the best ESD protection. Some protection device manufacturers have designed their products for a minimal parasitic capacitance to maximize signal integrity while others have maximized clamping performance at the cost of higher capacitance.

Silicon based devices such as TVS Diodes and Diode Arrays with the lowest dynamic resistance, offer superior clamping performance and have one of the lowest parasitic package capacitances. Fig. 5 illustrates clamping performance of Silicon vs. MLV ESD protection technologies. As can be seen, Silicon based solutions offer the lowest clamping voltage.

USB 3.0 eye diagram test results later in this article (figures 9 and 10) show how Littelfuse TVS Diode Arrays offer is the best technology for protecting USB 3.0 applications against ESD.

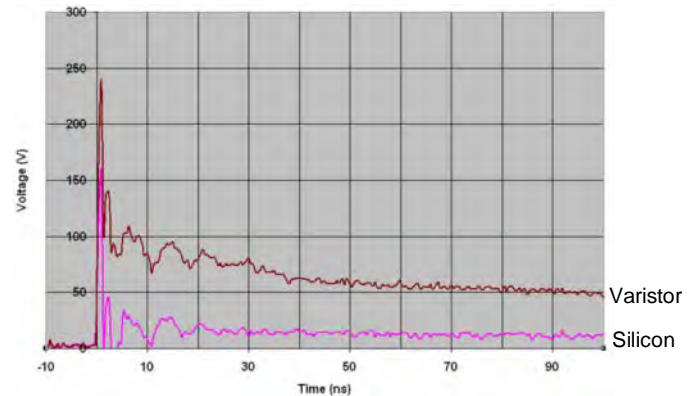


Fig. 5: Clamping performance of Silicon versus Varistor

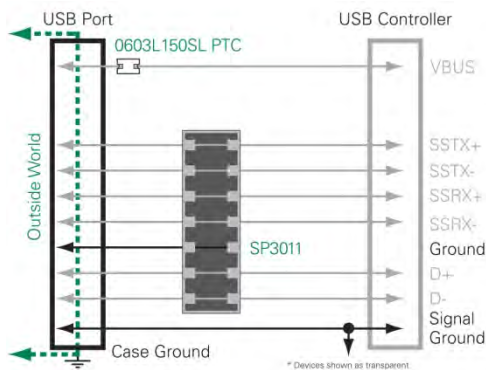
TVS Diode Array devices such as the Littelfuse SP3011 offer a multi-channel ESD protection solution ideal for USB 3.0 protection. Littelfuse SPA™ devices work in two ways, first, they absorb the transient with diodes, to steer the current, and then, an avalanche or zener diode, clamps the voltage level.



**Fig 6. Littelfuse SP3011 and SP3012 SPA™ TVS Diode Arrays were specifically designed for USB 3.0 protection.**

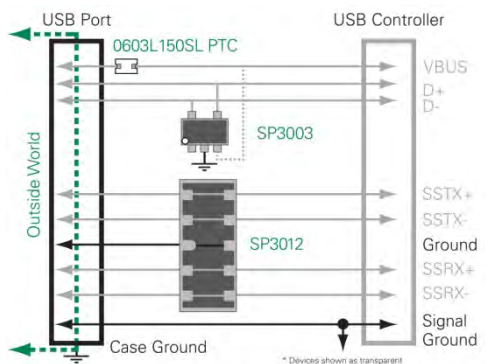
Fig.7 depicts a USB 3.0 ESD protection solution using a Littelfuse SP3011.

Offering six lines of  $\pm 8\text{kV}$  ESD protection, and being able to protect both USB 3.0 differential pairs and legacy USB 2.0 data lines in a single package, designers no longer have to worry about using multiple ESD protection devices which take up valuable board space.



**Fig. 7 USB 3.0 ESD protection with SP3011 device**

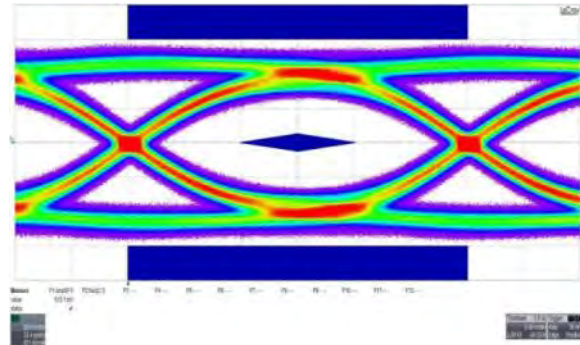
Alternatively, for designers who prefer to implement a two device solution, the SP3012 and SP3003 Series are recommended for protecting the six data lines (See figure 8). The SP3003 protects the legacy D+/D- pair while the SP3012 protects the two super-speed differential pair with it's extremely low dynamic resistance of only  $0.4\Omega$ . This provides best-in-class clamping performance for USB 3.0 chipsets or translator IC's that are very sensitive to overvoltage events.



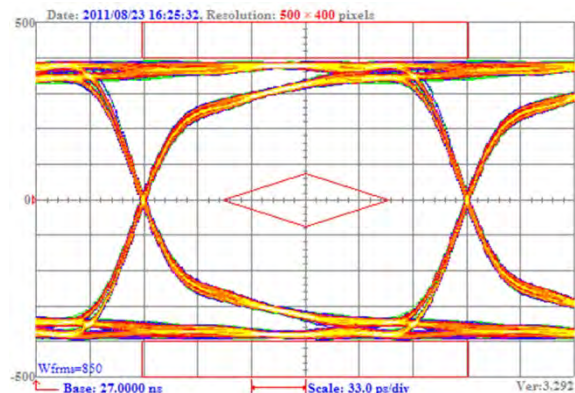
**Fig. 8 USB 3.0 ESD protection with SP3012 and SP3003**

## Signal Integrity

Maintaining USB 3.0 data integrity is critical and any small amount of added capacitance can cause signal distortion and degrade signal reliability. One way to evaluate what effect an ESD suppressor's parasitic capacitance will have on signal integrity is to conduct eye-diagram testing. This test involves repetitively sampling a digital signal and displaying the resulting eye pattern on an oscilloscope. A mask is often used to define acceptable signal qualities and compliance.



**Fig. 9 Eye-diagram of SP3011 at 5Gbits/s**



**Fig. 10 Eye-diagram of SP3012 at 5Gbits/s**

Figures 9 and 10 display eye-diagrams of Littelfuse SP3011 and SP3012 SPA TVS Diode Array devices using a 5Gbit/s USB 3.0 compliance test pattern and mask. In order to simulate a real world USB 3.0 data path, test boards were designed with 90ohm differential signal pairs and USB 3.0 connectors. It can be seen that signals are well within mask boundaries and wide eye width is maintained offering designers flexibility within a systems capacitance budget.

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