

Board-Level Design Considerations for ESD Circuit Protection

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Introduction

A topic of particular concern in the electronics design community today is the inadvertent damage that can be done by the end-users of electronic products. Normal day-to-day activities can cause people to build up static electricity which can later be transferred to objects (file cabinet, door, electronic devices, etc.).

As a person walks across a carpeted floor, a transfer of charge takes place. Similarly, the act of sliding out of an office chair can cause a transfer between the chair and its occupant. This effect is called *triboelectric charging*, and occurs anytime two dissimilar materials are brought into contact and then separated. The subsequent transfer of electrical charge (to an object at lower electrical potential) is referred to as *electrostatic discharge*, or ESD.

The issue at hand for the design, quality, and reliability communities is the effect that the transfer of static electricity has on their electronic products. For example, as people go about their daily activities (walking, getting out of chairs, etc.) and then interact with their equipment (cell phones, PDA's, laptop computers, etc.), they can barrage the devices with ESD pulses. If the ESD pulse finds its way into the electronic devices, physical damage can be done to the circuitry located inside.

The ESD Association has reported that the estimated average loss of product due to user-generated ESD is 27-33%. Whether the product loss occurs at the user-level or during the manufacturing process, the fact remains that ESD is a bottom-line effect that can reduce product reliability and company profit.

To help reduce losses due to ESD, chip manufacturers can incorporate transient voltage suppression structures into their integrated circuitry dies. This will make them more robust and help increase yields in the chip foundry and board manufacturing processes. There are various standards that apply to these environments and are used to verify the reliability of the chip design. These standards include Charged Device Model (CDM), Machine Model (MM), and Human Body Model (HBM).

The problem occurs when the electronic product transfers from the manufacturing environment to actual daily usage. The level of ESD that the end-user can generate, and introduce to the electronic device, is much more severe than the level found in the controlled manufacturing environment. This means that a design, which had high yields during manufacturing, can experience higher losses in the field. A model for the ESD transients that can be introduced by the user is typified in the IEC 61000-4-2 test methodology.

The focus of ESD protection has shifted from chip hardening to system hardening. The previously mentioned CDM, MM and HBM standards apply to chip hardening and do not guarantee system hardness. So a chip that reliably survived that manufacturing processes can experience higher failure rates after the end product is introduced to the

field. The bottom line is that there are two lines of defense against ESD; the chip level and the system (board) level. This article will focus on critical ESD suppressor selection criteria and recommendations and supporting data for guiding optimal ESD protection at the board level.

ESD Suppression

Having recognized that the ability of an integrated circuit (IC) or application specific integrated circuit (ASIC) to survive the manufacturing process doesn't guarantee that it will survive "real world" usage, the question becomes – what can be done to improve the survivability, or reliability, of my design? Currently, there are numerous protection options available to the designer. These include isolation circuits, filtering circuits, and suppression components (multilayer varistors, silicon diodes, and newly introduced polymer-based suppressors).

Suppression components protect the circuit by clamping the ESD voltage to a level that the circuit can survive. Connected in parallel with the signal lines, the suppressors clamp the ESD voltage and shunt the majority of the ESD current away from the data line (and the protected chip) to the appropriate reference. The power rail and chassis ground are typical references.

While all of these approaches can enhance the ESD survivability of the electronic device, there are inherent characteristics that should be considered during the selection process. The obvious characteristics include size, pin out, pad layout, and leakage current. However, as the need for circuits to provide higher informational throughput increases, another characteristic becomes very important – *capacitance*.

Capacitance and Signal Integrity

Today, and in the past, the inherent package capacitance of a suppressor could be used to the advantage of the circuit designer. Where there is a high degree of separation between the signal frequency and any unwanted frequencies (such as EMI "noise" and ESD transients), capacitance provides the additional benefit of filtering. Essentially acting like a low band pass filter, the suppressor provides clamping functions for transient suppression and can provide EMI filtering against unwanted, high-frequency signals that couple into the protected data line.

As an example, the headset terminals on a cell phone operate at relatively low frequency (audio range), while ESD and the cell phone operating frequency (800 – 1,900 MHz) are much higher. "High" capacitance multilayer varistors and diodes are ideal choices to provide ESD protection (from the user) and include the added benefit of filtering radiated cell phone signals out of the headset lines.

However, this "benefit" becomes a detractor when the signal speed is increased. The need for higher informational throughput (video, audio, and data) requires an increase in the data rates that are transmitted. Examples of these "high-speed" data lines include the USB2.0, IEEE 1394, Gigabit Ethernet, and Infiniband protocols. The data rates of all these protocols exceed 100 Mbps.

At these speeds, the capacitance that aided in the elimination of unwanted noise will also begin to filter the data signals themselves. The result will be distorted data

waveforms that can render that system inoperable. The distortion takes the form of rounded leading and trailing edges of high/low state transitions due to slower rise and fall times.

The slower rise/fall times introduce problems into the circuit. Most importantly, timing issues can be encountered. The circuit expects “high” and “low” states to be stable at specific times. As the transition time between states increases, the circuit can be caught sensing an incomplete transition and data errors can be introduced into the system.

Circuits will operate as they were designed as long as the information that controls them conforms to the intended protocol. As components of the signals degrade, the ability of the circuit to recognize the intended information is decreased. From a circuit protection standpoint, the goal is to provide ESD protection to the circuit **and** to maintain the integrity of the data (not interfere with circuit operation).

Refer to Figure 1 and Figure 2 for the following discussion. Data was collected at two data frequencies to investigate the effect that package capacitance has on data integrity. Littelfuse ESD products and ceramic capacitors were used. The specific technologies are not the focus here; the capacitance values are the important factors.

The products used in the test were:

PulseGuard® suppressor	0.050 pF	(PGB0010603)
ML ceramic capacitor	1.0 pF	
ML ceramic capacitor	10.0 pF	
Multilayer varistor	660 pF	(V5.5MLA0603)

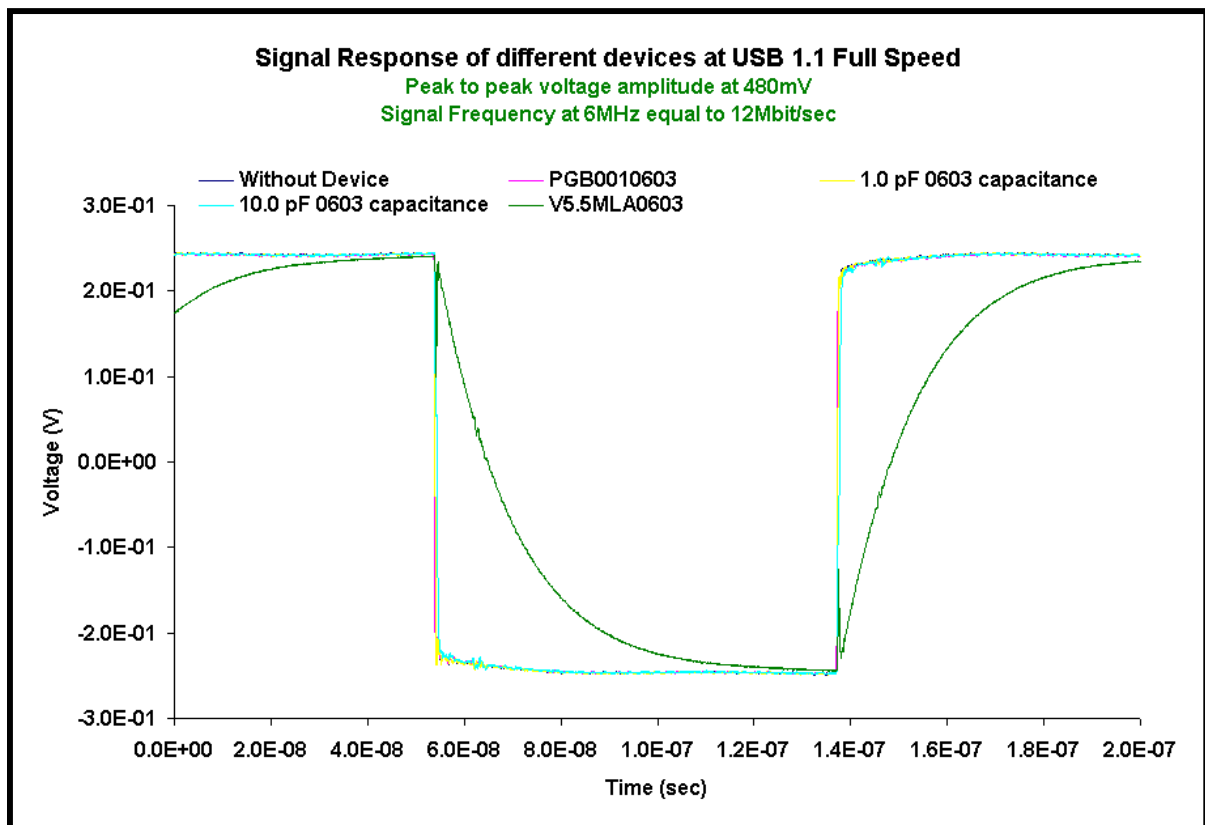


Figure 1. Response of 12 Mbit/sec waveform to various capacitance values.

The capacitance values represented here are 0.050 pF, 1.0 pF, 10 pF, and 660 pF. These values are from an 0603 PulseGuard® ESD suppressor, ceramic chip capacitors, and an 0603 ML series multilayer varistor, respectively. The premise is that as the capacitance value increases, so too does that signal distortion.

While the rise time (10/90%) of the 12Mbit/sec waveform is fast (0.242 ns), the time that it holds its level is considerably longer (80 ns). At this data rate, a capacitance value of 10 pF or less will allow the data to pass with minimal distortion. However, the 660 pF capacitance value clearly demonstrates how the leading and trailing edge of the data are rounded.

Contrast this information with Figure 2. Here we see the same devices tested with a data waveform of 480 Mbit/sec. The rise time for the two signals is the same (0.242 ns). However, the 480Mbit/sec signal has a much shorter level time of 2.0 ns. Note the different time scales of the two charts.

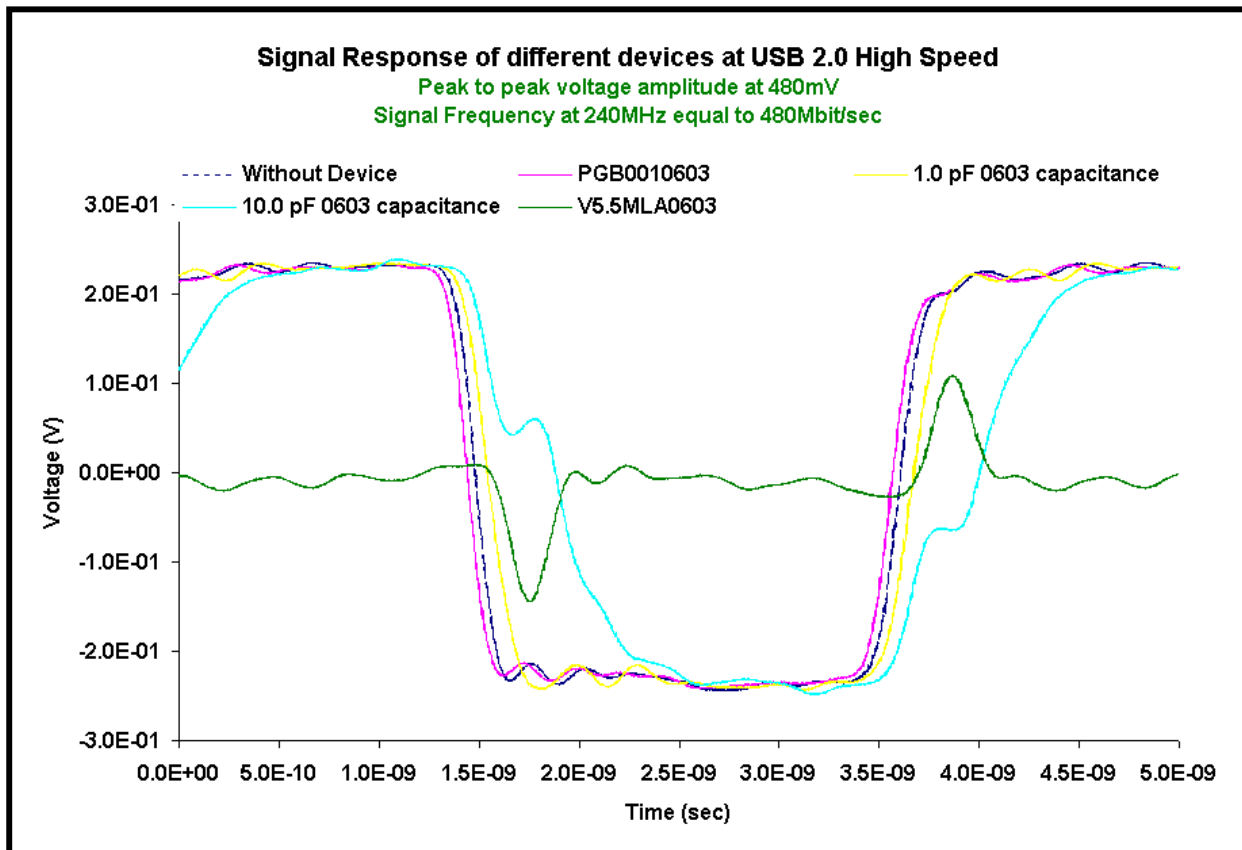


Figure 2. Response of 480Mbit/sec waveform to various capacitance values.

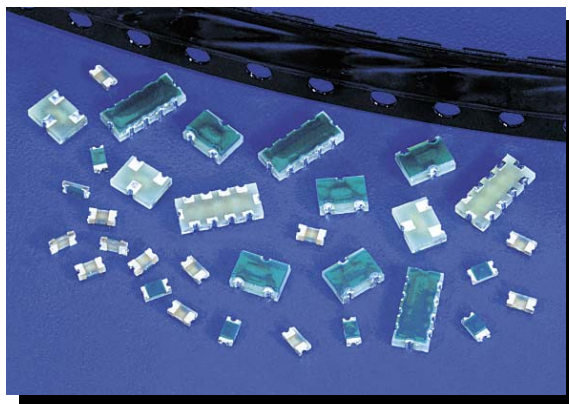
In this case, the 660 pF of capacitance causes so much distortion that the waveform is not able to reach the signal operating voltage. In essence, none of the data is being propagated down the signal line.

Even the capacitance value of 10 pF is high enough to cause substantial distortion to the waveform. Here we see a decrease in the amount of level time and significant changes in the leading and trailing edge shapes. The capacitance value of 1.0 pF shows a small amount of edge distortion, while the 0.050 pF capacitance value allows the data waveform to pass without distortion. The following chart shows the rise time (10/90%) data for each capacitance value. The data refers to the waveforms from Figure 2 (bit rate of 480 Mbps).

Measurement set-up	10/90% Rise time
Baseline, no devices	225 ps
0.050 pF – PulseGuard® suppressor	225 ps
1.000 pF – Ceramic chip capacitor	275 ps
10.00 pF – Ceramic chip capacitor	526 ps
660.0 pF – MultiLayer varistor	Not measurable, t_r longer than bit rate

The purpose in providing this data is to show that the capacitance characteristic of an ESD suppressor is extremely important when protecting data lines of systems that operate at very high speeds. While all existing suppressors can provide effective ESD protection, the signal integrity of the system cannot be compromised. So it is important to consider the capacitance of an ESD suppressor before adding it to the circuit design.

Extremely low capacitance ESD suppression devices such as Littelfuse PulseGuard ESD suppressors can provide ESD protection functionality, while maintaining the data integrity of high-speed data signals.



ESD Suppressor Installation Considerations

Having chosen an ESD suppressor whose suppression and electrical characteristics (leakage current, capacitance, etc.) are a good match for the circuit parameters, another decision remains to be made. Where should the suppressor be installed on the board to

optimize the ESD protection for the circuit? By “optimized” ESD protection, we mean that the protected chip sees as little of the ESD transient as possible.

High speed signals and transients (like ESD) bring another parasitic characteristic into play - *inductance*. Specifically, we are interested in the parasitic inductance of the board traces that are used as interconnects between the connector, the chip, and any support components.

Similar to capacitance, low frequency signals will be unaffected by the inductance that is presented by the board traces. However, at high speeds, the inductance will present an impedance component that can affect signal integrity. Recall the formula for inductive reactance: $X_L = \omega L$. This can also be written as: $X_L = 2\pi fL$.

So, a small amount of trace inductance can translate into substantial amount of impedance when a high frequency signal (e.g. ESD) is run through it. We can take advantage of this knowledge by putting as much distance between the ESD suppressor and the protected chip. Referring to Figure 3, the following inductance values are represented:

- L1 - between the connector and the ESD suppressor
- L2 - between the ESD suppressor and the I/O pin of the chip
- L3 - between the I/O line and the ESD suppressor (stub trace)

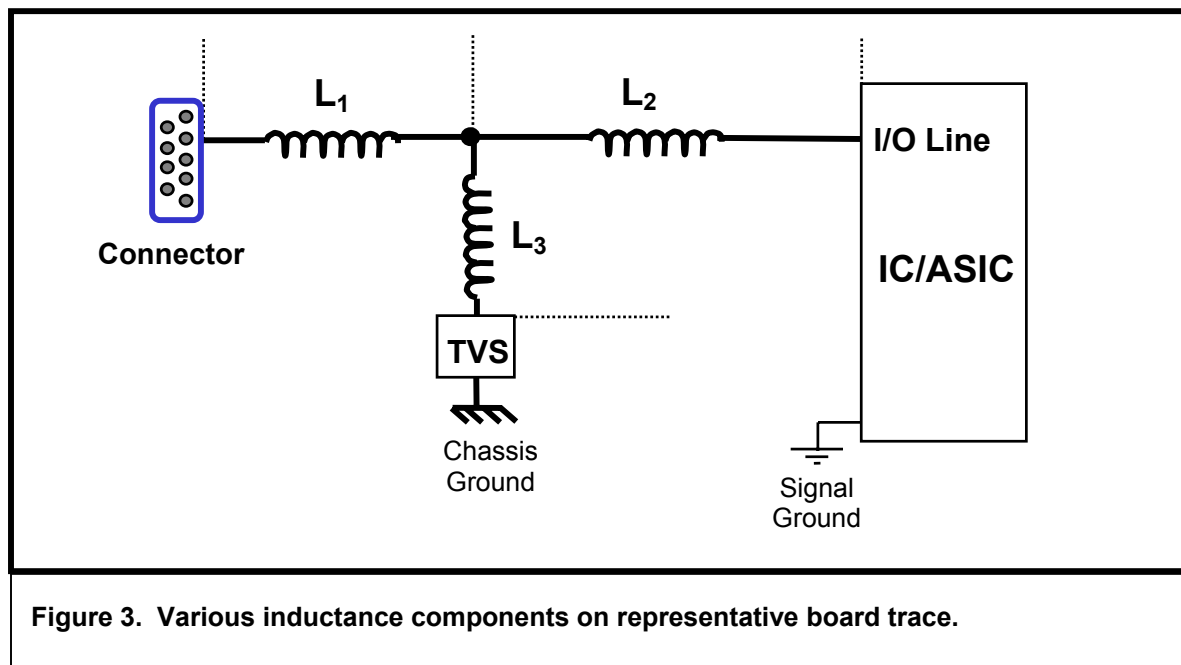


Figure 3. Various inductance components on representative board trace.

In essence, the inductance attributable to L2 will dissipate the energy of the ESD pulse that remains after the clamping action of the ESD suppressor. Attenuation of the ESD pulse’s voltage and current take place as the energy is stored and dissipated in the electromagnetic field around the board trace.

It can be seen that there is an inverse relationship between the length of board trace and ESD pulse energy that finally arrives at the chip’s I/O pin. As the length of the trace

increases, the strength of the ESD pulse (seen at the chip) decreases. The decreased ESD pulse translates into reduced stress on the chip.

Figure 4 demonstrates the attenuation of the ESD pulse as it propagates down the board trace.

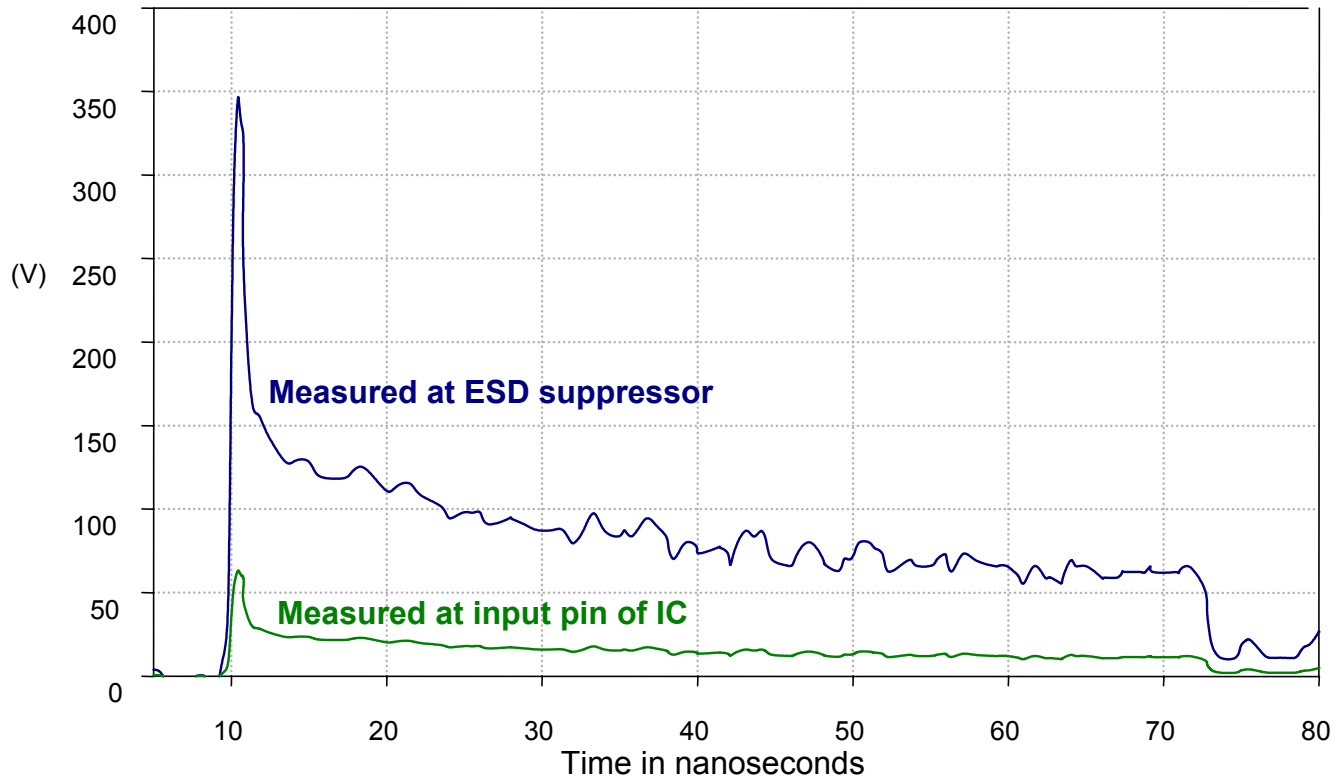


Figure 4. Voltage versus time plots of ESD transient at different board locations.

The plots in Figure 4 show the voltage versus time values that were measured at two locations on a test board. They begin to give us an understanding of the effects of placement location of the ESD suppression device. In this example, the suppressor was installed at the connector (entry point for ESD transients).

The blue waveform shows the voltage that was measured on the I/O line, at the location of the ESD suppressor. The suppressor has responded to the 1,000 Volt TLP pulse with a measured peak voltage of approximately 350 V and a “clamping”, or holding, voltage of about 75 V.

Contrast this with the green waveform, which shows the ESD pulse that actually gets to the IC. In this case, a 3-inch long trace (L2) connected the ESD suppressor site and the input pad for the IC. Here we see that the measured peak voltage has been reduced to 60 V and the “clamping” voltage is approximately 25 V.

What does this mean? For the circuit designer, this provides a tactic for minimizing the amount of ESD that is experienced on the I/O inputs of the IC's and ASIC's. By

increasing the amount of trace length between the ESD suppressor and the chip, the amount of stress that the IC experiences can be dramatically reduced. Referring to Figure 3, this means that by making the trace longer, the “L2” value is increased.

Plainly speaking, the ESD suppressor should be located directly behind the connector. It should be the first board-level component that the ESD transient encounters. Then, to the extent that it is practical, the chip(s) that is (are) to be protected should be located as far away as possible. As demonstrated in Figure 4, this tactic will drastically reduce the stress that the integrated circuitry experiences.

The following list is arranged to show the relative preference of ESD suppressor installation locations. The optimal location is listed first, and the least preferred site is listed last:

- Inside connectors which are the gateway in the system shielding (chassis),
- At the point where circuit board traces interact with the pins of the connector,
- On the circuit board immediately behind the connector,
- On robust, unprotected lines that may efficiently couple to I/O lines,
- Before a series resistive element on a data line,
- Before a fan-out point on a data line,
- And, the last and very least ideal location is near the IC and/or ASIC.

Another placement consideration is the distance from the board trace to the ESD suppressor itself. The goal is to minimize this distance. The inductance associated with the trace, and any parasitic package inductance, will insert impedance in the protection circuit. Referring back to Figure 3, we are looking at “L3” from the diagram.

In essence, the ESD suppressor becomes more “isolated” from the signal line that it is protecting as its distance from the line increases. Remember that the chip will experience that ESD voltage across the suppressor and the voltage across the trace impedance. The ideal solder pad placement would be right on top of the data line. If this is not possible, then this distance should be minimized.

Lastly, the recommendation is made that the chassis (frame) ground should be the ESD reference, not the signal (digital) ground (see Figure 3). The objective is to transfer the ESD out of the signal environment. By referencing the ESD (TVS) protection device to chassis ground, unintentional noise effects (ground bounce, etc.) can be avoided. We want to keep the signal (data) environment as clean as possible.

Summary

There are many concerns facing a circuit designer in their quest for a functional and reliable product. The evolution of the electronics marketplace towards higher data throughput and faster signal speeds adds to this complexity.

On-chip transient voltage suppression structures are designed to increase the yields of the chips in the foundry and board manufacturing environments. They are typified according to standards such as CDM, MM, and MIL-STD HBM. However, the severity of ESD in the “real-world” environment is much higher. Everyday users of electronic products (cell phones, PDA’s, laptop computers, etc.) will introduce a more severe level of ESD into those products. These ESD transients are typified in the IEC 61000-4-2 test

methodology. Survival through the manufacturing process **does not** guarantee survival in the hands of the end-user. “Supplemental” ESD protection such as ESD suppressors may be necessary.

It is important to understand the suppression characteristics of ESD protectors **and** their package characteristics as well. It is extremely important that stray characteristics (such as capacitance) are understood so that they can be taken into consideration during the board design. So make sure that the ESD suppressor is a good fit with the circuit parameters (data rates, leakage current, etc.).

Optimal placement of ESD suppressors begins at the location of ESD penetration into the system. This tactic reduces the ESD voltage and current experienced by the circuit and by attenuating the ESD pulse that propagates past the ESD suppressor. So make sure to design as much practical space between the ESD suppressor and the protected chip as possible.

The ESD effectiveness of a suppressor can be reduced if it is placed too far away from the line it is protecting. The board trace inductance can cause an additional amount of voltage, or “overshoot”, to be seen by the chip. So make sure to install the ESD suppressor as close to the protected line as possible.

Selecting an ESD “solution” is no longer as simple as choosing a suppressor that is rated for the operating voltage of the circuit. An effective solution now takes into account the layout of the circuit board as well as the non-suppression electrical characteristics of the ESD suppression devices.

Author Biography

James Colby has been a Marketing Engineer for Littelfuse, Inc. for three years, focusing on polymeric ESD suppression products. He has been involved in the circuit protection industry for ten years. His current responsibilities include New Product Development and New Business Development. He has a BSEE from Southern Illinois University and an MBA from Keller Graduate School of Business.