# ESD and Transient Protection Using the SP720

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The need for transient protection in integrated circuits is driven by the quest for improved reliability at lower cost. The primary efforts for improvement are generally directed toward the lowest possible incidence of over-voltage related stresses. While electrical overstress (EOS) is always a potential cause for failure; a discipline of proper handling, grounding and attention to environmental causes can reduce EOS causes for failure to a very low level. However, the nature of hostile environments cannot always be predicted. Electrostatic Discharge (ESD) in some measure, is always present and the best possible ESD interface protection may still be insufficient. As the technology of solid state progresses, the occurrence of ESD related IC failures is not uncommon. There is a continuing tendency for both ESD and EOS failures, due in part, to the smaller geometries of today's VLSI circuits.

The solid state industry has generally acknowledged a standard for the level of capability in LSI designs of ±2000V for the Human Body Model where the defined capacitance is 100pF and the series resistance is 1500Ω. However, this level of protection may not be adequate in many applications and can be difficult to achieve in some VLSI technologies. Normal precautions against ESD in the environment of broad based manufacturing are often inadequate. The need for a more rugged IC interface protection will continue to be an established goal.

Historically, it should be recognized that early IC development began to address the ESD problem when standards for handling precautions did not exist. High energy discharges were a common phenomena associated with monitor and picture tube (CRT) applications and could damage or destroy a solid state device without direct contact. It was recognized that all efforts to safeguard sensitive devices were not totally sufficient. Small geometry signal processing circuits continued to sustain varying levels of damage through induced circulating currents and direct or indirect exposure in handling. These energy levels could be substantially higher than the current standard referenced in MIL-STD-3015.7; also referred to as the Human Body Model.

The recognized need for improved ESD protection was first precipitated under harsh handling conditions; particularly in applications that interfaced to human contact or from the interaction of mechanical parts in motion. The popular features of component and modular electronic equipment have continued to generate susceptibility to IC damage while in continuing use. These market items include computers and peripherals, telecommunication equipment and consumer electronic systems. While some ICs may only see the need for ESD protection while in manufacturing

assembly or during service in the field, the most common cause for ESD failures can still be related to a human contact. Moreover, educational efforts have improved today's manufacturing environment substantially reduce failures that relate to the mechanical handling. The ESD failure causes that relate to mechanical handling now have a test standard referred to as a Machine Model which relates to the source of the generated energy.

While the electrical model for an energy source is generally accepted as a capacitor with stored charge and a series resistance to represent the charge flow impedance, the best means to handle the high energy discharge is not so clearly evident. The circuit of Figure 1 illustrates the basic concept that is applied as a method of ESD testing for the Human Body Model. The ESD energy source is shown as a charged capacitor $C_D$ and series connected, source impedance, resistor $R_D$. The point of contact or energy discharge is shown, for test purposes, as a switch external to the IC. A protection structure is often included on an IC to prevent damage from an ESD energy source. To properly protect the circuit on the IC the on-chip switch, $S_S$, is closed when a discharge is sensed and shunts the discharge energy through a low impedance resistor ($R_S$) to ground. It is imperative that the resistance of the discharge path be as low as practical to limit dissipation in the protection structure. It is not essential that the ground be the chip substrate or the package frame. The energy may be shunted via the shortest path external to the chip to an AC or DC ground.
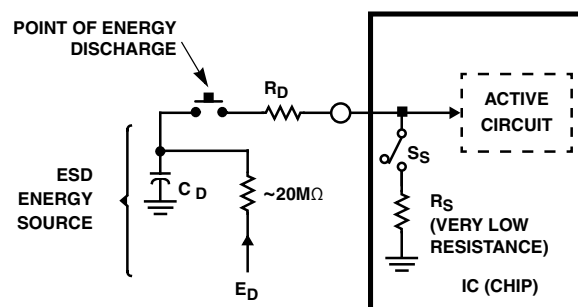


**FIGURE 1. ESD TEST FOR AN ON-CHIP PROTECTION CIRCUIT USING THE MIL-STD-883, METHOD 3015.7 (HUMAN BODY MODEL)**

This conceptual method has been used in many IC designs employing a wide variation of structures, depending the IC technology and degree of protection needed. The switch, $S_S$ is generally a threshold sensitive turn-ON at some voltage level above or below the normal signal range; however, it must be within the a safe operating range of the device being protected. The resistance, $R_S$ is shown as the inherent series resistance of the protection structure when it is

discharging (dumping) the ESD energy. In its simplest forms, the protection structures may be diodes and zeners, where the sensing threshold is the forward turn-ON or zener threshold of the device. The inherent resistance becomes the bulk resistance of the diode structure when it is conducting. Successful examples of two such protection structures that have been used to protect sensitive inputs to MOS devices are shown in Figure 2. The back-to-back zener structure shown for the dual-gate MOSFET was employed in the 3N - dual gate MOS devices before IC technology was firmly established. The series poly and stacked diode structure used to shunt ESD energy followed several variations for use in CMOS technology and was employ in the CD74HC/HCT - High Speed CMOS family of logic devices. This CMOS protection structure is capable of meeting the 2000V requirements of MIL-STD-883, Method 3015.7; where the $R_D$ in Figure 1 is 1500$\Omega$ and $C_D$ is 100pF.
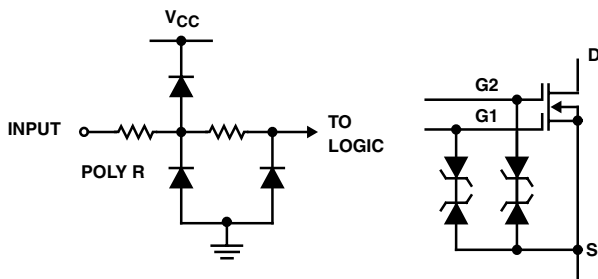


**FIGURE 2. ESD AND TRANSIENT PROTECTION EFFECTIVELY USED IN MOS AND CMOS DEVICES**

Due to greater emphasis on Reliability under harsh application conditions, more ruggedized protection structure have been developed. A variety of circuit configurations have been evaluated and applied to use in production circuits. A limited introduction to this work was published in various papers by L. Avery (See Bibliography). To provide the best protection possible within economic constraints, it was determined that SCR latching structures could provide very fast turn-ON, a low forward on resistance and a reliable threshold of switching. Both positive and negative protection structures were readily adapted to bipolar technology. Other defining aspects of the protection network included the capability to be self-protecting to a much higher level than the signal input line being protected. Ideally, when a protection circuit is not otherwise needed, it should have no significant loading effect on the operating circuit. As such, it should have very little shunt capacitance and require minimal series resistance to be added to the signal line of the active circuit. Also, where minimal capacitance loading is essential for a fast turn-ON speed, the need for a simpler structure is indicated.

The switching arrangement for a basic and simple protection structure is shown in Figure 3. Each high side and low side protection structure ($R_S$ and $S_S$) is an embedded device, taking advantage of the P substrate and epitaxial N material used in bipolar technology. Each cell contains an SCR with a

series dropping resistor to sense an over-voltage turn-ON condition and trip the SCR (Switch $S_S$) into latch. The ON-resistance ($R_S$) of the latched SCR is much lower than $R_D$ and, depending on the polarity of the ESD voltage, dumps energy from the input signal line through the positive or negative switch to ground. The return to ground for either ESD polarity is not limited by voltage supply definition, but may be to positive or negative supply lines, if this suits the needs of the application. When the energy is dissipated and forward current no longer flows, the SCR automatically turns-OFF.
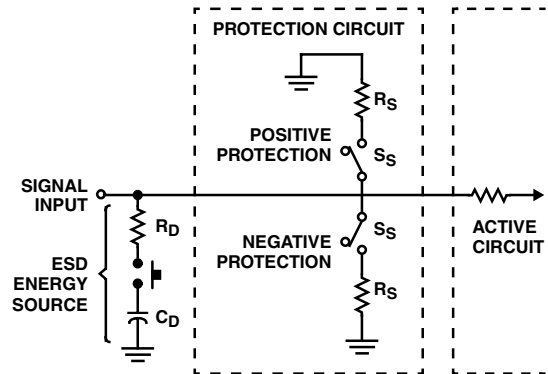


**FIGURE 3. ESD AND TRANSIENT PROTECTION CIRCUIT**

Figure 4 shows the diagram of a positive and negative cell protection circuit as it applies to the SP720. The PNP and NPN transistor pairs are used as the equivalent SCR structures. Protection in this structure allows forward turn-ON to go marginally above the +V supply to turn-ON the high-side SCR or marginally below the -V supply to turn-ON the low-side SCR. The signal line to the active device is protected in both directions and does not add series impedance to the signal input line. A shunt resistance is used to forward bias the PNP device for turn-ON but is not directly connected to the signal line. As an on-chip protection cell, this structure may be next to the input pad of the active circuit; which is the best location for a protection device. However, for many applications, the technology of the active chip may not be compatible to structures of the type indicated in Figure 4. This is particularly true in the high speed CMOS where the substrates are commonly N type and connected to the positive supply of the chip. The protection cell structure shown in Figure 4 is not required to be on the active chip because it does not sense series input current to the active device. The sense mechanism is voltage threshold referenced to the V+ and V- bias voltages.

The cell structure of the SCR pair of Figure 4 are shown in the layout sketch and profile cutouts of Figure 5. It should be noted that the layout and profiles shown here are equivalent structures intended for tutorial information. The structures are shown on opposite sides of the "IN" chip bonding pad, as is the case for the SP720. As needed for a preferred layout, the structures are adjacent to the pad and as close to the positive and negative supply lines as possible. The common and best choice for effective layout is to provide a ground

ring (V-) around the chip and to layout with minimum distance paths to the positive supply (V+). In the SP720 the V- line is common to the substrate and frame ground of the IC.

The equivalent circuit diagram of the SP720 is shown in Figure 6. Each switch element is an equivalent SCR structure where 14 positive and negative pairs as shown in Figure 4 are provided on a single chip. Each positive switching structure has a threshold reference to the V+ terminal, plus one $V_{BE}$ (based-to-emitter voltage equal to one diode forward voltage drop). Similarly, each negative switching pair is referenced to the V- terminal minus one $V_{BE}$.
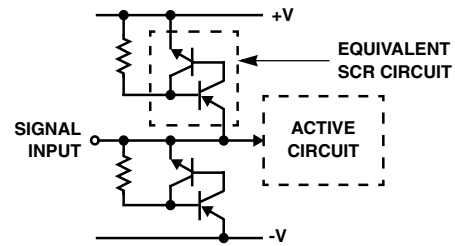


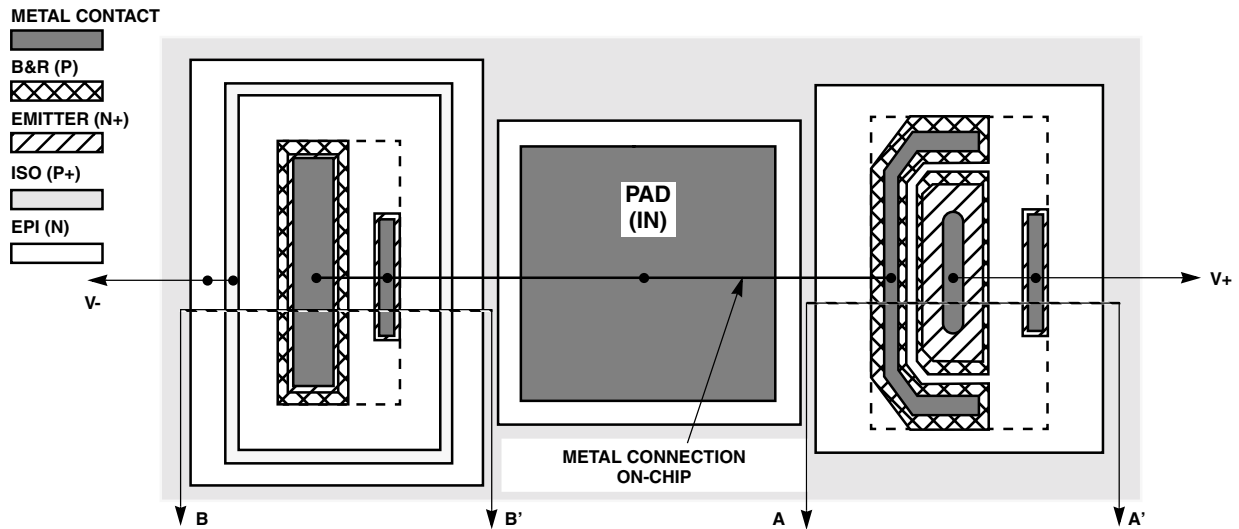**FIGURE 4. PROTECTION CELLS OF THE SP720 SCR ARRAY**



**FIGURE 5A. HIGH AND LOW CELL PAIR LAYOUT; SHOWN WITHOUT PROTECT, METAL AND FIELD OXIDE LEVELS (NOT TO SCALE)**
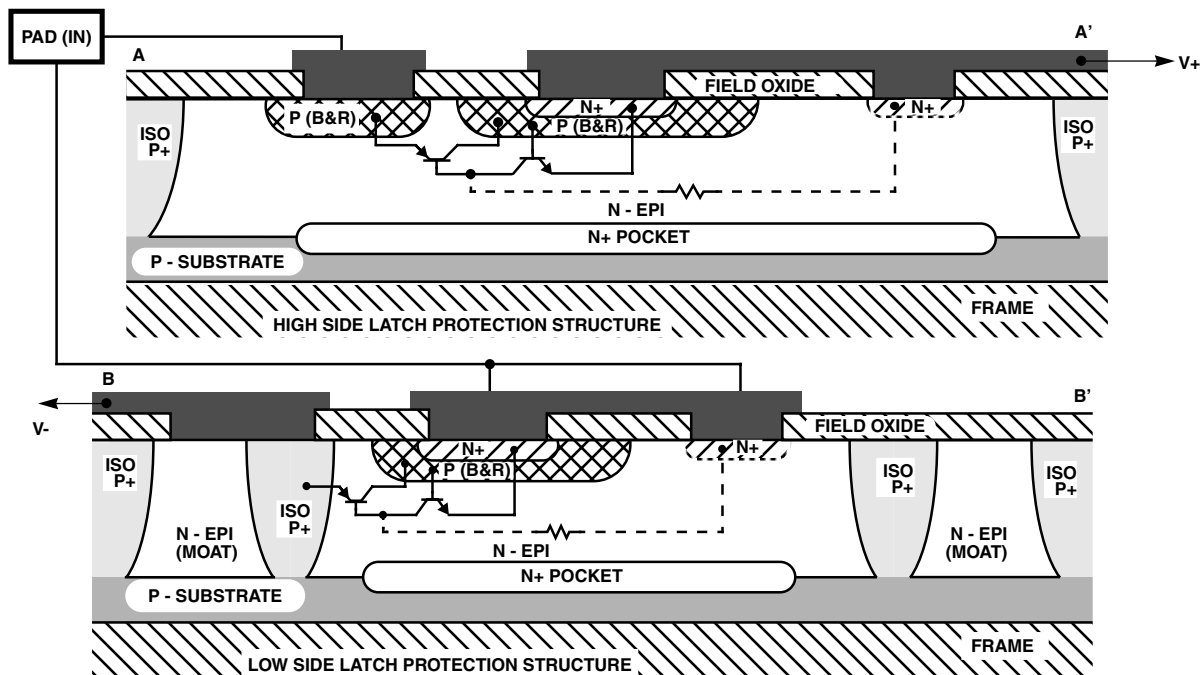


**FIGURE 5B. PROFILES OF THE HIGH AND LOW SIDE SP720 SCR PROTECTION PAIR (NOT TO SCALE)**

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The internal protection cells of the SP720 are directly connect to the on-chip power supply line (+V) and the negative supply line (-V), which are substantial in surface metal content to provide low dropping resistance for the high peak currents encountered. Since both positive or negative transients can be expected, the SCR switches direct the positive voltage energy to V+ and the negative voltage sourced energy to V- (substrate) potential to provide fast turn-ON with low ON resistance to protect the active circuit.
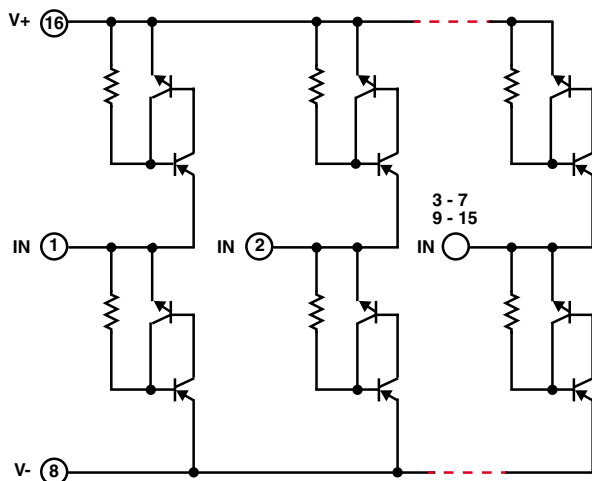
**FIGURE 6.  EQUIVALENT CIRCUIT DIAGRAM OF THE SP720**

The V+ and V- supply lines of the SP720 are not required to be the same as those of the circuit to be protected. However, overvoltage protection is referenced to the V+ and V- supply voltages for all of the signal input terminals, IN1-IN7 and IN9-IN15. The V+ and V- supply voltages to the SP720 may be changed to suite the needs of the circuit under protection. The range of voltage may be power supply levels ranging from 4.5V up to the 35V maximum rating of the SP720. Lower levels of voltage are possible but with some degradation of the switching speed which is nominally 2ns. Also, the input capacitance which is nominally 3pF can be expected to increase. There is no significant quiescent current in the SP720 other than reverse diode junction current which nominally less than 50nA over the rated -40°C to 105°C operating temperature. At room temperatures, this may be as low as a few nanoamperes. Because of the low dissipation of the SP720, the chip temperature can be expected to be close to the environment of the physical location where it is applied to use.

### Protection Levels of the SP720

For a given level of voltage or power, there is a defined degree of protection compatible to that need. For the SP720, the protection circuits are designed to clamp over-voltage within a range of peak current that will substantially improve the survival input expectancy of average monolithic silicon circuits used for small signal and digital processing applications. Within itself, the SP720 should be expected to survival peak current and

voltage surges within the maximum ratings defined in the data sheet. For voltage, the static DC and short duration transient capability is essentially the same. The process capability is typically better than 45V, allowing maximum continuous DC supply ratings to be conservatively rated at 35V. The current capability of any one SCR section is rated at 2A peak but is duration limited by the transient heating effect on the chip. As shown in Figure 7, the resistance of the SCR, when it is latched, is approximately 0.96Ω and the SCR latch threshold has 1.08V of offset. For EOS, the peak dissipation can be calculated as follows:

For:     2A Peak Current, $R_D = 1500\Omega$,

Then:   $V_{IN(PK)} = 1.08V$ (Offset) + (0.96Ω x 2A) = 3V

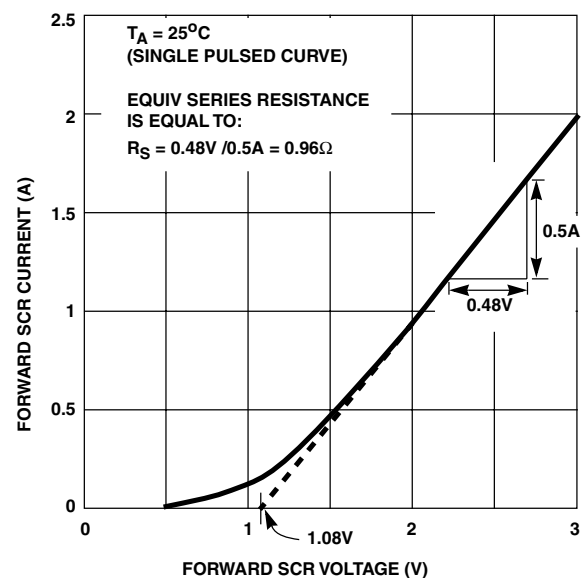The peak dissipation is $P_D = 3V \times 2A = 6W$

**FIGURE 7.  SCR FORWARD CURRENT vs VOLTAGE CHARACTERISTICS**

While 2A through 1500Ω is 3000V, which is not an exceptionally high ESD level of voltage, it does represent the EOS capability, provided the time duration for the 6W of dissipation is limited to a few milliseconds. The dissipation of the 16 pin DIP and 16 pin SOIC packages are typically less than 1W for steady state conditions. The thermal capacity of the chip will allow discharge levels several times higher than this because ESD normally has a much shorter duration. The actual results for ESD tests on the SP720 as an isolated device are as follows:

1. Human Body Model using a modified version of the MIL-STD-883, Method 3015.7; with V+ and V- grounded and ESD discharge applied to each individual IN pin - Passed all test levels from ±9kV to ±16kV (1kV steps).

2. Human Body Model using the MIL-STD-883, Method 3015.7 (with V- only grounded) and ESD discharge applied to each individual IN pin - Passed all test levels to ±6kV, failed ±7kV (1kV steps).

3. Machine Model using EIAJ IC121 ($R_D$ = 0Ω); discharge applied to IN pins with all others grounded - Passed all test levels to ±1kV, failed ±1.2kV; (200V steps).

4. While there are many potential uses for the SP720, the circuit of Figure 8 shows a normal configuration for protecting input lines to a sensitive digital IC. Each line is connected to an IN- Input of the SP720 in a shunt connection. As a test model a 2μ digital ASIC CMOS IC was used to evaluate the ESD level of capability provided by the SP720. Without external protection, the ESD level of capability of the CMOS process was typically no better than ±2.5kV. When the SP720 was applied to use as shown in Figure 8, the ESD resistance to damage was better than ±10.2kV. (Higher levels were not evaluated at the time due to high voltage limitations.)

It should be noted that the MIL-STD-883, Method 3015.7 test allows for one pin as a reference when testing. While this cannot be disputed as handling limitation, it is not a test for all aspects of applied use. To properly apply the SP720 to use in the application specifically requires that the V- pin be connected to a negative supply or ground and the V+ pin be connected to a positive supply. The SP720 was designed to be used with the supply terminals bias and, as such, has better than ±16kV of ESD capability. For this reason, the modified test method as described, with the V+ pin connected via a ground return, is correct when the circuit is assembled for use.

## SP720 CMOS Protection Model

Where the need to provide ESD protection for CMOS circuits is the primary interest for the application of the SP720, interface characteristics of the device to be protected may lead to some specific problems. Application related issues and precautions are discussed here to assist the circuit designer in achieving maximum success in EOS/ESD protection.

### CMOS Input Protection

CMOS logic has limited on-chip protection and may contain circuit elements that add difficulty to the task of providing external protection. Consider the case where the input structure of a CMOS device has on-chip protection but only to the extent that it will withstand Human Body Model minimum requirement for ESD when tested under the MIL-STD-883, Method 3015.7. This is normally ±2kV where the charged capacitor is 100pF and the series resistor to the device under test is 1500Ω. The circuit of Figure 9 shows the typical network for an HC logic circuit where the input polysilicon resistor, $R_P$ is typically 120Ω.
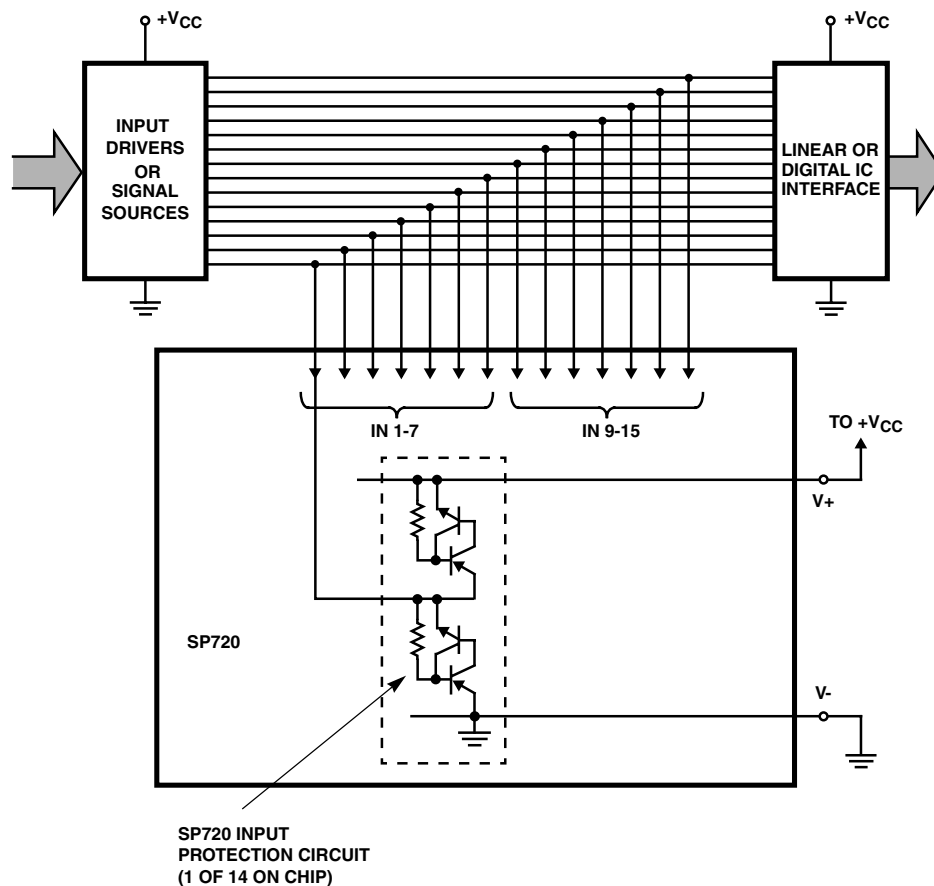


FIGURE 8. PRACTICAL APPLICATION AND TEST EVALUATION CIRCUIT

When there is a surge or ESD voltage applied to the input structure, the diodes shunt current to $V_{CC}$ or GND to protect the logic circuits on the chip. The on-chip series resistors limit peak currents. If there is a positive transient voltage, $V_{CS}(t)$, applied to the input of the CMOS device, the diode, $D_1$ will conduct when the forward voltage threshold exceeds the power supply voltage, $V_{CC}$ plus the forward diode voltage drop of $D_1$, $V_{FWD1}$. As the voltage at the input is further increased, the CMOS current, $I_{CS}$ is shunted through $R_P$ and $D_1$ to $V_{CC}$ such that the transient input voltage is

$$V_{CS}(t) = I_{CS}(t) \cdot R_P + V_{FWD1} + V_{CC} \quad \text{[for Pos. } V_{CS}(t)] \qquad \text{(EQ. 1)}$$

or

$$I_{CS}(t) = [V_{CS}(t) - (V_{FWD1} + V_{CC})]/R_P \qquad \text{(EQ. 1A)}$$

Similarly, when there is a negative transient, current initially conducts at the negative threshold of diode $D_2$, $V_{FWD2}$ to shunt negative current at the input, i.e.,

$$V_{CS}(t) = I_{CS}(t) \cdot R_P + V_{FWD2} \quad \text{[for Neg. } V_{CS}(t)] \qquad \text{(EQ. 2)}$$

or

$$I_{CS}(t) = [V_{CS}(t) - V_{FWD2}]/R_P \qquad \text{(EQ. 2A)}$$

While the circuit of Figure 9 is specifically that of the HC logic family (one cell of the Hex Inverter, 74HCU04), many CMOS devices have a similar or an equivalent internal protection circuit. When compared to the SCR structure of the SP720, the on-chip diodes of the protection network in Figure 9 have lower conduction thresholds.
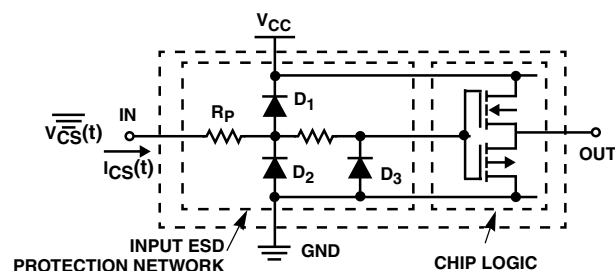


**FIGURE 9. TYPICAL CMOS IC INPUT PROTECTION CIRCUIT**

### SP720 to CMOS Interface

Figure 10 shows the SCR cell structures of one protection pair in the SP720. In this example, the V+ of the SP720 is connected to the $V_{CC}$ logic supply and the V- is connected to logic GND. The IN terminal of the SP720 is connected to the CMOS logic device input through a resistor $R_I$. When a negative transient voltage is applied to the input circuit of Figure 10, the Reverse SCR Protection Circuit turns on when voltage reaches the forward threshold of the PNP device and current conducts through the SCR resistor to forward bias the PNP transistor. The PNP device then supplies base current to forward bias and turn on the NPN device. Together, the PNP and NPN transistors form an SCR which is latched on to shunt transient current from IN to V-. The Forward SCR Protection Circuit has the same sequence for turn on when a positive

transient voltage is applied to the input and conducts to shunt transient current from IN to V+ ($V_{CC}$).
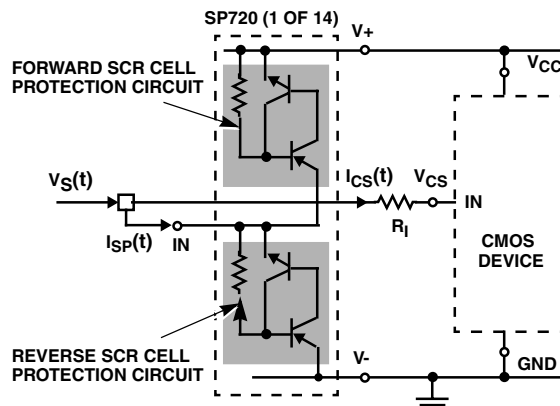


**FIGURE 10. SP720 SCR INTERFACE TO A CMOS INPUT WITH $R_I$ ADDED TO ILLUSTRATE MORE EFFECTIVE ESD PROTECTION FOR CMOS DEVICES**

The Voltage-Current characteristic of the SCR is similar to a diode at low currents but changes to low saturated on resistance at high currents. As shown in the SP720 data sheet, the forward SCR (latched on) voltage is ~1V at 60mA which is ~0.2V higher than a typically junction diode. The fully saturated turn on approaches 0.5A at 1.5V. When the SCR is paralleled with the a CMOS device input having an on-chip protection circuit equivalent to Figure 9, some of the current necessary to latch the SCR is shunted into the CMOS input. For some devices this may be sufficient for an ESD discharge to damage the CMOS input structure before the SP720 is latched on.

The trade-off for achieving a safe level of ESD protection is switching speed. The most effective method is the addition of the series resistor, $R_I$ as shown in Figure 10. The series input resistor, as shown, is a practical method to limit current into the CMOS chip during the latch turn on of the SP720 SCR network. The value of $R_I$ is dependent on the safe level of current that would be allowed to flow into the CMOS input and the loss of switching speed that can be tolerated. The level of transient current, $I_{CS}$ that is shunted into the CMOS device is determined by the series resistor, $R_I$ and the voltage developed across the CMOS protection devices, $R_P$ and $D_1$ or $D_2$, plus some contribution from the path of diode, $D_3$ for negative transients.

As shown in Figure 11, the voltage across the SP720 SCR element is determined by its turn on threshold, $V_{TH}$ and the saturated resistance, $R_S$ when latched. The empirically derived equation for the voltage drop across the SP720 voltage is

$$V_{SP}(t) = I_{SP}(t) \cdot R_S + V_{TH} \qquad \text{(EQ. 3)}$$

or

$$I_{SP}(t) = [V_{SP}(t) - V_{TH}]/(R_S) \qquad \text{(EQ. 3A)}$$

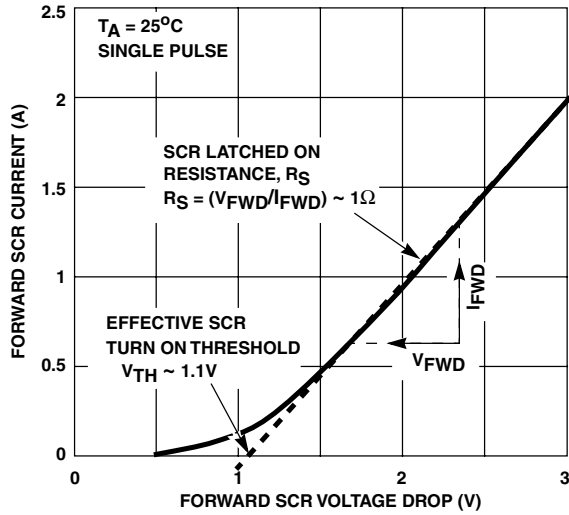where $V_{TH} \sim \pm 1.1V$ and $R_S \sim 1\Omega$.

**FIGURE 11. FORWARD TURN ON CHARACTERISTIC OF AN SP720 SCR CELL**

where current conduction in the SP720 may be positive or negative, depending on the polarity of the transient. For the circuit of Figure 10, $V_S(t)$ is also the input voltage to the resistor, $R_I$ in series to the input of the CMOS device. When latched on, the impedance of the SP720 is much less than the input impedance of either $R_I$ or the CMOS input protection circuit. Therefore, the CMOS loop current can be determined by the voltage, $V_S(t)$ and the known conditions from Equation 3.

For a **negative** transient input to the CMOS HCU04, the loop equation is:

$$V_S(t) = I_{CS}(t) \cdot (R_I + R_P) + V_{FWD2} \qquad \text{(EQ. 4)}$$

or

$$I_{CS}(t) = [V_S(t) - V_{FWD2}]/(R_I + R_P) \qquad \text{(EQ. 4A)}$$

An equation solution for an input transient may be more directly solved by empirical methods because of the nonlinear characteristics. Given a transient voltage, $V_S(t)$ at the input, a value for $R_I$ can be determined for a safe level of peak current into a CMOS device. The input Voltage-Current characteristic of CMOS device should be known. As a first order approximation, the CMOS V-I curve tracer input characteristics of the 74HCU04 are shown in Figure 12. As indicated in Figure 12, the voltage drop across $R_P$ and $R_I$ in series ($R_P$~120$\Omega$) will be significantly larger than the delta changes in the forward voltage drop of the $D_1$ or $D_2$ diodes over a wide range of current. As such, we can effectively assume $V_{FWD}$ ~ 0.75V for moderate levels of current.

### Example Transient Solution

Based on the circuit of Figure 10, negative and positive ESD discharge circuit models of the SP720 and HCU04 are shown in Figure 13A and 13B. The negative ESD voltage is taken as the worse case condition because a positive ESD

voltage will discharge to the $V_{CC}$ power supply and the positive offset voltage will reduce the forward current. Using the negative model, a peak current value for $I_{SP}$ can be determined by the transient conditions of the applied voltage, $V_S(t)$ at the input.
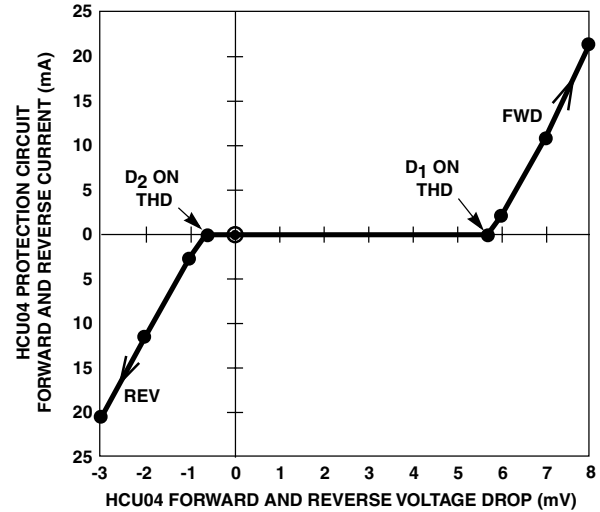


**FIGURE 12. FORWARD AND REVERSE PROTECTION CIRCUIT INPUT VOLTAGE-CURRENT CHARACTERISTIC OF THE HCU04 SHOWN FOR $V_{CC}$ = 5V (i.e., $D_1$ THD ~ 5V + 0.7V)**
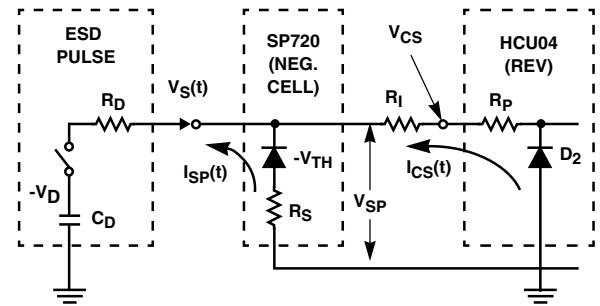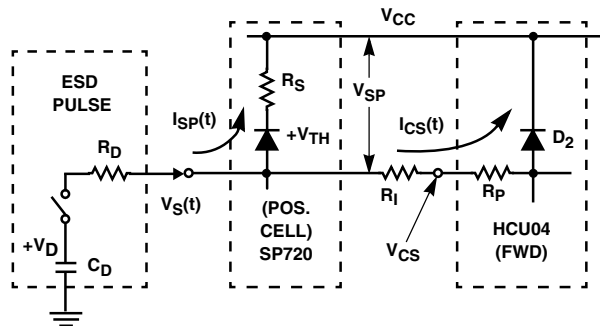


**FIGURE 13A. NEGATIVE ESD DISCHARGE MODEL**



**FIGURE 13B. POSITIVE ESD DISCHARGE MODEL**

Given MIL-STD ESD HBM test conditions ($C_D$ = 100pF and $R_D$ = 1500Ω), Equation 3 with the resistors $R_D$ and $R_S$ in series, we can calculate the peak current for a specified voltage, $V_D$ on the capacitor, $C_D$.

$$I_{SP}(t) = [V_D(t) - V_{TH}]/(R_D + R_S) \sim V_D(t)/R_D \qquad \text{(EQ. 5)}$$

Here, $V_D$ replaces $V_S$ as the driving voltage; and assumes that (1) $R_S$ is much less than $R_D$; (2) $R_S$ is much less than ($R_I + R_P$); and (3) $V_{TH}$ is much less than $V_D$. This may or may not be the general case but is true for the values indicated here. As such,

$$[I_{SP}]_{t=0} \sim V_D/1500.$$

Given an ESD discharge of -15KV, neglecting inductive effects and distributed capacitance, the peak current at time t = 0 will be ~10A. And, with the SP720 latched on as shown in Equation 3, the 10A peak current will result in an ESD pulse at the input of the SP720 of ~11V. For the HCU04 to withstand this surge of voltage, it is required that the dropping resistor, $R_I$ attenuate the peak voltage, $V_{CS}$ at the HCU04 input to within acceptable ratings.

The negative reverse current path is through $R_I$, $R_P$ and $D_2$; where $R_P$ and $D_2$ are part of the HCU04. For a negative ESD discharge voltage, $V_D$ from capacitor $C_D$, the equation for the peak voltage, $V_{CS}$ at the input to the HCU04 is derived as follows:

Substituting Equation 5 into Equation 3, we have:

$$V_S \sim (V_D/R_D) \bullet R_S - 1.1 \qquad \text{(EQ. 6)}$$

and from Equation 2 and Equation 4A, a general solution for the $V_{CS}$ voltage is

$$V_{CS} = [(V_S - V_{FWD2})/(R_I + R_P)] \bullet R_P + V_{FWD2} \qquad \text{(EQ. 7)}$$

For a simpler approach, one can work backwards to arrive at the correct solution. The reverse CMOS voltage vs current curve of Figure 11 indicates that a peak voltage, $V_{CS}$ of -3V will produce a negative current of approximately -20mA which is the rated absolute maximum limit. For a -15kV ESD discharge and from Equation 6, the peak voltage, $V_S$ is:

$$V_S = (V_D/R_D) \bullet R_S - 1.1 = (-15/1500) - 1.1 = -11.1V$$

The peak current, $I_{CS}$ from Equation 4A is

$$I_{CS} = [(V_S - V_{FWD2})/(R_I + R_P)]$$
$$\quad = [(-11.1 -(-0.7))]/(R_I + 120Ω)$$

Given the $I_{CS}$ current of -20mA and solving for $R_I$,

$$R_I = 397.5Ω$$

The same result can be derived from Equation 7 but is more susceptible to rounding errors and the assumed voltage drop of $V_{FWD2}$ due to the ($V_{CS} - V_{FWD2}$) difference that appears in the equation.

The approximation solution given here is based on a ±20mA current rating for the HCU04 device; although, input voltage ratings are exceeded at this level of current. As such, the solution is intended to apply only to short duration pulse

conditions similar to the MIL-STD-883, Method 3015.7 specifications for ESD discharge conditions. For long periods of sustained dissipation, the SP720 is limited by the rated capability of its package.

Figure 14 shows the distribution of currents for the circuit of Figure 10 given a specific value of $R_I$. Curves are shown for both $I_S$ (HCU04 + SP720) and $I_{SP}$ (SP720) versus a negative input voltage, $V_S$. The resistor, $R_I$ value of 10Ω is used here primarily to sense the current flow into the HCU04. (This data was taken with the unused inputs to the HCU04 connected to ground and the unused inputs to the SP720 biased to $V_{CC}/2$ on a resistive divider.) The Figure 14 curves verify the model condition of Figure 13A with the exception that resistive heating at higher currents increases the resistance in the latched on SCR. This curve explains the ESD protection of the Littelfuse High Speed Logic "HC" family and, in particular, demonstrates the value of the $R_P$ internal resistor as protection for the HCU04 gate input. Added series resistance external to a signal input is always recommended for maximum ESD protection.
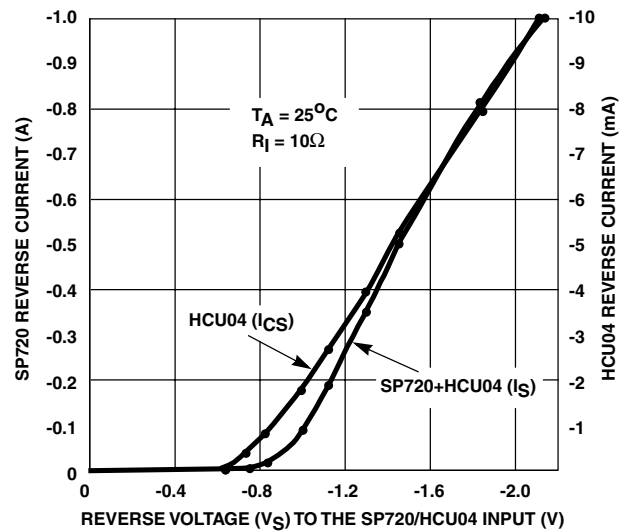


**FIGURE 14. MEASURED REVERSE CURRENT vs VOLTAGE CHARACTERISTIC OF THE SP720/HCU04 FOR THE FIGURE 10 CIRCUIT PROTECTION MODE**

### Range of Capability

While the SP720 has substantially greater ESD self protection capability than small signal or logics circuits such as the HCU04, it should be understood that it is not intended for interface protection beyond the limits implied in the data sheet or the application note. The MIL-STD-883, Method 3015.7 condition noted here defines a human body model of 100pF and 1500Ω where the capacitor is charged to a specified level and discharged through the series resistor into the circuit being tested. The capability of the SP720 under this condition has been noted as ±15kV. And, for a machine model where no resistance is specified, a

200pF capacitor is discharged into the input under test. For the machine model the level of capability is ±1kV; again demonstrating that the series resistor used in the test or as part of the application circuit has pronounced effect for improving the level of ESD protection.

While a series resistor at the input to a signal device can greatly extend the level of ESD protection, a circuit application, for speed or other restrictions, may not be tolerant to added series resistance. However, even a few ohms of resistance can substantially improve ESD protection levels. Where an ESD sensitive signal device to be protected has no internal input series resistance and interfaces to a potentially damaging environment, added resistance between the SP720 and the device is essential for added ESD protection. Circuits often contain substrate or pocket diodes at the input to GND or $V_{CC}$, and will shunt very high peak currents during an ESD discharge. For example, if the HCU04 of Figure 14 is replaced with device having a protection diode to ground and no series resistor, the anticipated increase in input current is 10 times.

Shunt capacitance is sometimes added to a signal input for added ESD protection but, for practical values of capacitance, is much less effective in suppressing transients. For most applications, added series resistance can substantially improve ESD transient protection with less signal degradation.

A further concern for devices to be protected is forward or reverse conduction thresholds within the power supply range (not uncommon in analog circuits). Depending on the cost considerations, the power supply V+ and V- levels for the SP720 could be adjusted to match specific requirements. This may not be practical unless the levels are also common to an existing power supply. The solution of this problem goes beyond added series resistance for improved protection. Each case must be treated with respect to the precise V-I input characteristics of the device to be protected.

## Interface and Power Supply Switching

Where separate system components with different power supplies are used for the source signal output and the receiving signal input, additional interface protection circuitry maybe needed. The SP720 would normally have the same power supply levels as the receiving (input) device it is intended to protect. When the SP720 with its receiving interface circuit is powered off, a remote source signal may be activated from a separate supply (i.e., remote bus connected systems). The user should be aware that the SP720 remains active when powered down and may conduct current from the IN input to the V+ (or V-) supply.

Within its own structure, **any** IN input of the SP720 will forward conduct to V+ when the input voltage increases to a level greater than a $V_{BE}$ threshold above the V+ supply. Similarly, the SP720 will reverse conduct to V- when the input voltage decreases to a level less than a $V_{BE}$ threshold below the V- supply. Either condition will exist as the V+ or V-

level changes and will continue to exist as the V+ collapses to ground (or V-) when the SP720 supply is switched off. If a transient or power surge is provided from the source input to the IN terminal of the SP720, after the V+ has been switched off, forward current will be conducted to the $V+/V_{CC}$ power supply line. Without a power supply to clamp or limit the rising voltage, a power surge on the input line may damage other signal devices common to the $V_{CC}$ power supply. Bypassing the $V_{CC}$ line may not be adequate to protect for large energy surges. The best choice for protection against this type of damage is to add a zener diode clamp to the $V_{CC}$ line. The zener voltage level should be greater than $V_{CC}$ but within the absolute maximum ratings of all devices powered from the $V_{CC}$ supply line.

### *Power Supply Off Protection, Rise/Fall Speed*

To illustrate the active switching of the SP720 and the speed of the SCR for both turn on and turn off, oscilloscope traces were taken for the circuit conditions of Figure 15. A pulse input signal is applied with **NO** supply voltage applied to the SP720. Figure 15 shows the positive and negative pulse conditions to V+ and V- respectively. The trace scales for Figure 15 are 10ns/division horizontal and 1V/division vertical. Input and output pulses are shown on each trace with the smaller pulse being the output. The smaller output trace is due to an offset resulting from the voltage dropped across the SCR in forward conduction. The OUT+ and OUT- pulses quickly respond to the rising edge of the input pulse, following within ~2ns delay from the start of the IN pulse and tracking the input signal. The output falls with approximately the same delay.

## *References*

[1] L.R. Avery, *"Electrostatic Discharge: Mechanisms, Protection Techniques, and Effects on Integrated Circuit Reliability"*, RCA Review, Vol. 45, No. 2, June 1984, Pg. 291 - 302.

[2] L.R. Avery, *"Using SCRs as Transient Protection Structures in Integrated Circuits,"* EOS/ESD Symp. Proc., 1983, Pg. 90 - 96.

[3] MIL-STD-883D, 15 Nov 91, *Electrostatic Discharge Sensitivity Classification, Method 3015.7*, 22 Mar 89.

[4] *Machine Model Standard ($R_D = 0\Omega$),* EIAJ IC121.

[5] EOS/ESD-DS5.2, Proposed Standard, *"EOS/ESD Association Standard for the Discharge (ESD) Sensitivity Testing - Machine Model (MM) - Component Level,"* Oct 92.

[6] Harris Suppression Products, *SP720 Data Sheet*, File No. 2791, Electronic Protection Array for ESD and Overvoltage Protection. (16 Lead Plastic IC available in DIP and SOIC packages).

[7] Harris Suppression Products, *SP721 Data Sheet*, File No. 3590, Electronic Protection Array for ESD and Overvoltage Protection (8 Lead Plastic IC in the SP720 family available in DIP and SOIC packages).

**POSITIVE/FORWARD CONDUCTION
HIGH SPEED ON/OFF PULSE (OUT+)**
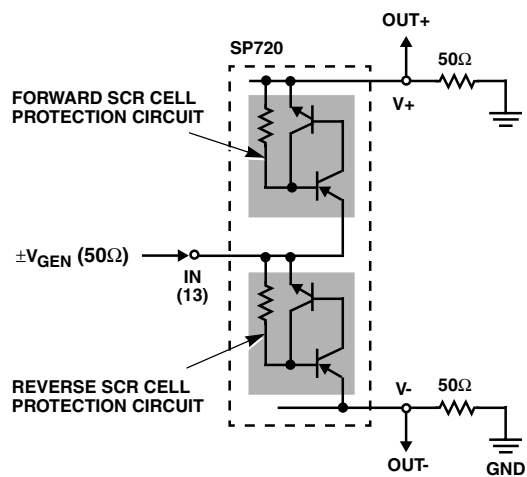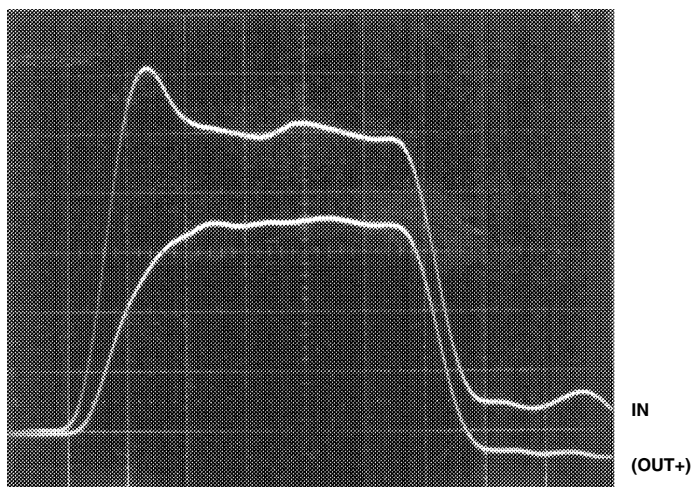


**NEGATIVE/REVERSE CONDUCTION
HIGH SPEED ON/OFF PULSE (OUT-)**



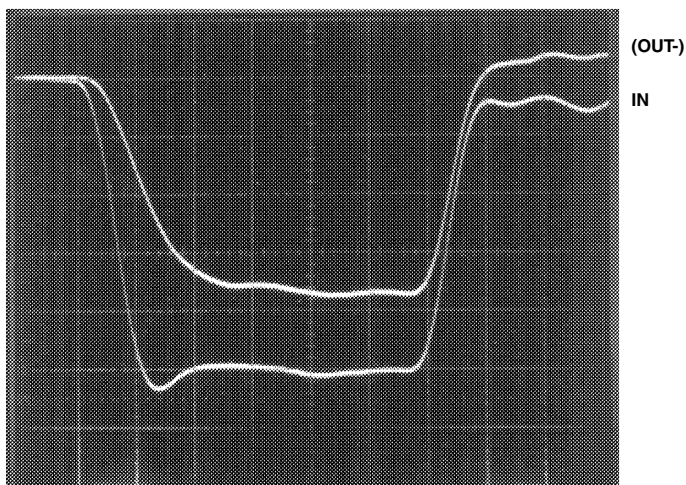**FIGURE 15. SP720 CIRCUIT WITH NO POWER SUPPLY INPUT PULSE TEST WITH 50Ω, (0V TO ±5V) INPUT. THE TRACE SCALES
FOR OUT+ AND OUT- ARE 1V/DIV VERTICAL AND 10ns/DIV HORIZONTAL**