

Protecting Electronic Devices Against ESD

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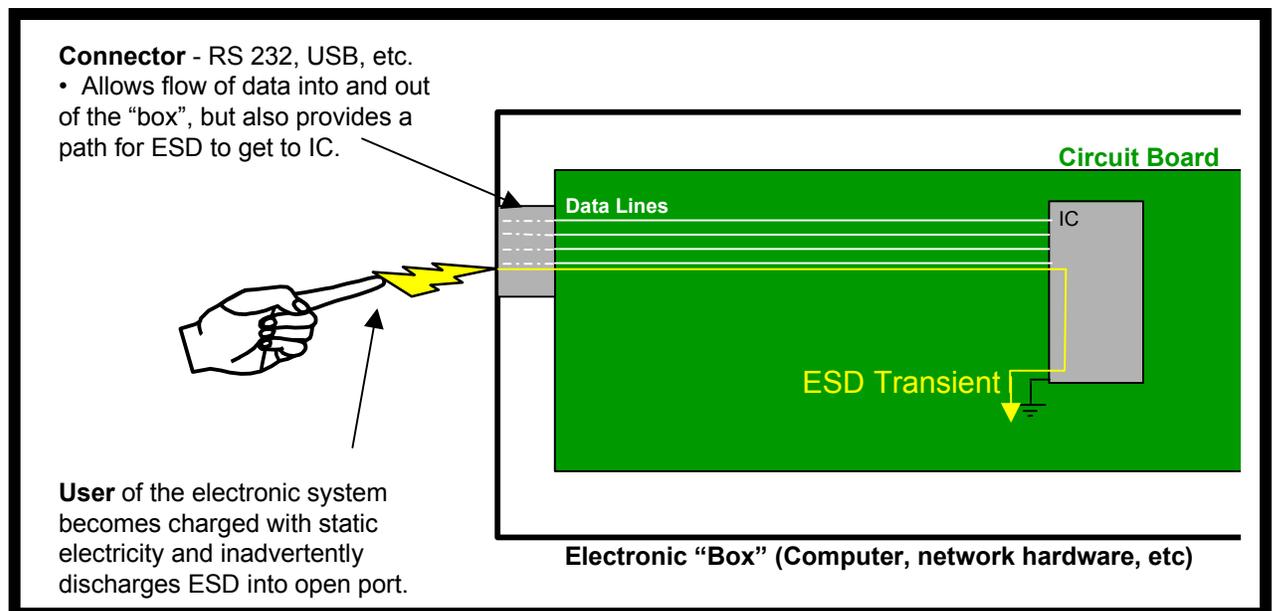
Introduction

The quest to provide reliable electronic products (computers, network hardware, cell phones, PDA's, etc.), requires a look at the "brains" of those devices. At the core of modern electronics is integrated circuitry (IC) that provides processing and communication functions. Because they are so crucial to the product, they need to be protected against electrical transients that can be generated by their users.

Specifically, Electrostatic Discharge (ESD) transients can be introduced to the devices (and ultimately to the IC's) during normal usage by the end user. But how does this occur? Picture an electronic device as a black box. Inside are various circuits (IC's, ASIC's, magnetics, etc.) that provide functionality; outside are various components (switches, buttons, keypads, data ports, etc.) to control the device.

Connecting the outside and inside environments are physical interconnects (cables, connectors/ports) that allow the flow of information (data). These input and output channels are necessary for the data flow, but they can also allow the introduction of ESD into the "box". Once in the "box", ESD seeks to dissipate its energy, a portion of which will gain exposure to the integrated circuitry.

Referring to the following schematic, we see that the input/output (data) lines can also become "gateways" for ESD to enter the "box". For example, a person can become electrically charged with static electricity by walking across a carpet. Then in the course of moving/connecting a computer, for example, they may inadvertently discharge the static electricity into an open data port (RS 232, USB, 1394, etc.). The ESD transient can then follow the data line and establish a path to the IC.



Chip-level ESD Protection

Before discussing the board-level strategies for protecting IC's, it must be noted that IC's typically have basic levels of ESD protection. Along with the functional parts of the IC (processor, communications, etc.), manufacturers typically include structures on the die that will provide ESD protection.

These structures are provided to increase the survivability of the IC's as they progress through the manufacturing process – chip foundry and board assembly. ESD will be present in these environments and including ESD protection increases yield rates.

There are several standards that have been established to determine the overall immunity of the IC's to ESD in the factory environment. These include:

- Charged Device Model (CDM)
- Machine Model (MM)
- Human Body Model (HBM)

These standards are meaningful in the controlled manufacturing environments, where precautions are taken to ensure that static electricity levels on personnel and equipment are minimized. For example, wrist straps, anti-static garments, grounded workstations, and various environmental controls (humidity/air ionization) are implemented.

With these treatments in place, and on-board structures designed to typically withstand ESD levels of 1 – 2 kV, good yield values for IC's can be achieved. However, the picture changes as the IC's move from the manufacturing environment to the real world (i.e., residence within electronic products). Since electronic products need to move information to and from the IC via data lines (Figure 1), the IC can ultimately be exposed to ESD generated by the user of the device.

In the “uncontrolled” world of everyday usage, the person that is interacting with the electronic product can generate ESD that is of much greater severity than that in the manufacturing environment. Under the right conditions, it is possible for a person to generate an ESD event of over 30 kV.

There are no standards that cover the finished electronic systems. There is however, a test methodology that has been developed to help companies determine the ESD immunity (susceptibility) of their products. The IEC 61000-4-2 document provides a test methodology (waveform, voltage/current values, how to test, etc.) to give companies guidance with respect to user-generated ESD.

A very important issue to remember is that IC's that survive the manufacturing environment (i.e. surpass CDM, MM, HBM standards) are not guaranteed to withstand ESD transients that are introduced into the systems by their users. The CDM, MM, HBM standards use slower rise-time and lower energy waveforms than those used in the IEC methodology, which is generally recognized as more indicative of user-generated ESD.

Supplemental ESD Protection – ESD Suppressors

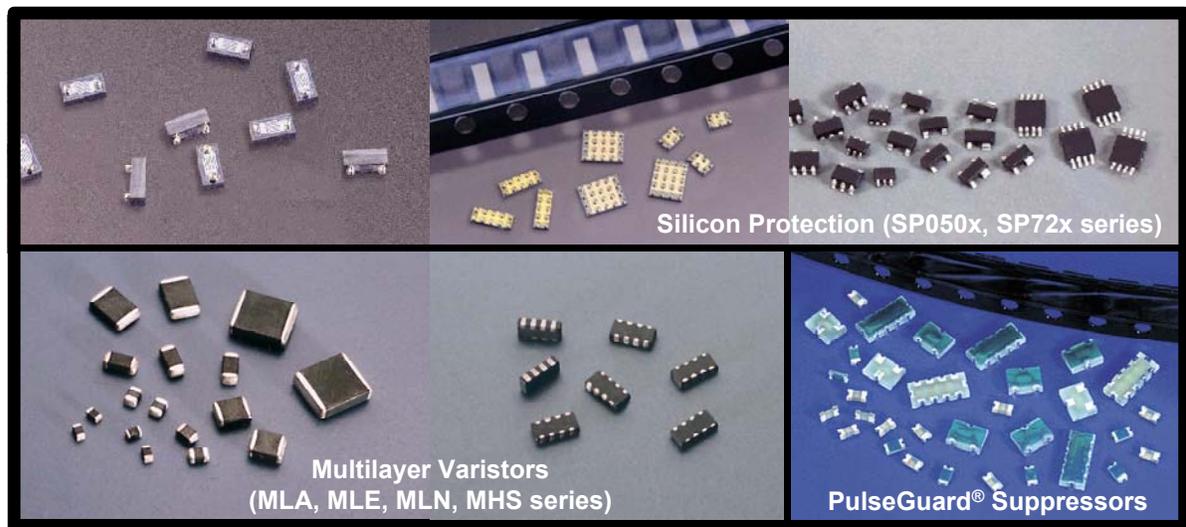
Even though product users can generate ESD transients in excess of the chip capabilities, all is not lost. At the board level, it is possible to add components that will

enhance the survivability of the IC's by reducing the ESD transient before it gets to the IC. A popular choice is to install surface mount devices on the susceptible lines.

Looking back at Figure 1, a mechanism for allowing ESD to be transmitted directly into the "box" is for an ESD transient to be introduced onto a data line (the informational pipeline into and out of the "box"). Without additional components, the ESD transient passes down the data line directly to the I/O pin of the IC. If the ESD level surpasses the ESD capability of the IC, damage can be done.

In order to reduce the ESD transient that an IC experiences, ESD suppressors can be installed on the data lines. They are connected in parallel with the IC, creating a bridge between the data line and a reference portion of the circuit. Typical references include the power rail, signal (logic) ground, and chassis (shield) ground. Chassis ground is preferred since it keeps unwanted ESD transient remnants out of the circuit that is used by the IC.

There are various options available for ESD protection. Littelfuse, Inc., for example, provides multilayer varistors, SCR diodes, TVS Avalanche diodes, and polymeric devices for ESD suppression (see Figure 2 below). Other options include filter circuits, circuit isolation, and spark gaps.



The purpose of suppression products is to "clamp", or reduce, the ESD threat voltage to a level that the IC can withstand. In short, the ESD transient causes the suppressor to transition from a high-resistance state to a low-resistance state. After turning "on", the suppressor shunts the ESD transient to the selected reference (power rail or grounds). By clamping the ESD transient, the overall system "hardness" against ESD can be increased. While the overall ESD capabilities of the IC have not been modified, the system's ESD capabilities have increased.

The need for board-level ESD protection will vary from system to system. Factors that influence the need include board layout, the ESD capabilities of the IC, and the physical ability of ESD transients to get on the data lines. Empirical testing can also be done to help determine the system's susceptibility.

If it is determined that supplemental ESD protection is desired, the next step is to identify the appropriate suppressor. There are many characteristics that should be considered during the selection process, for example:

- Capacitance
- Peak voltage and clamping level
- Leakage current
- System operating voltage
- Number of lines to be protected

Capacitance is becoming an extremely important criterion since the data rates at which electronic products are communicating continue to increase. If the capacitance of the suppressor is too high, it will load the data signal and can cause distortion that will affect signal integrity. For high-speed systems (USB 2.0, IEEE 1394, InfiniBand, etc.), an extremely low capacitance device like the PulseGuard[®] ESD suppressor is appropriate.

On the other hand, if the data in the system is relatively low frequency (audio, RS 232, IEEE 1284, etc.), additional capacitance can be beneficial. The capacitance provides an effective low-pass filter, which can minimize high-frequency noise in the system. For these instances, the MLA, MLE, MLN, and MHS series of suppressors are appropriate.

As previously mentioned, the **Clamping Level** of the suppressor determines how much of the ESD transient is eliminated. A related value is the **Peak Voltage**. As the suppressor transitions from high to low resistance, a portion of the ESD wave front is transmitted before the clamping voltage is established.

These are important factors for those IC's that do not have a substantial amount of on-chip ESD protection. In this case, it is important that as little ESD as possible is actually experienced by the IC. For these circuits, the SP050x and SP72x product lines are ideal. They have extremely low peak and clamping voltages to provide ultimate protection to the IC.

Leakage Current describes the amount of current that is passed through the ESD suppressor while the circuit is operating normally (i.e. at rated voltage). It is an important consideration for applications where the main power supply is battery-driven. In these cases, it is desirable for the suppressor to allow as little leakage as possible, so the battery drain time is not increased. All of the Littelfuse ESD suppressors have very low typical leakage current.

Suppressors tend to have varied **System Operating Voltage** specifications that are determined by their construction. This is used to determine if the part is suitable for given circuit parameters. For example, a 5 VDC-rated part should not be used where the ESD reference is a 9 VDC bus. The excess voltage may cause degradation of the part.

Another consideration is the **Number of Lines to be Protected**. This is determined by the system's data protocol. For example, USB buses have two data lines, RS 485 uses two lines per differential pair, 10/100BaseT Ethernet uses four lines, etc. In cases where multiple data lines will be protected, it may be desirable to use a multi-line suppressor to save board space and installation costs. This will be weighed against the flexibility in

using multiple single line devices. Littelfuse suppressors are available in single and multiple line packages to offer a broad selection to the circuit designer.

Lastly, it is important to take into account the installation location of the ESD suppressor. In order to optimize the protection scheme, the suppressor should be located as close to the source of ESD as possible. If at all possible, the ESD suppressor should be the first board level device that the ESD transient experiences after it reaches the PC board.

Also, the suppressor should be located as close as possible to the line that it is protecting. Because ESD is such a fast rise-time event, any distance between the protected line and the ESD suppressor will translate into more transient voltage experienced by the IC.