

Thyristor \ Diode Module

$$V_{RRM} = 2 \times 1200 \text{ V}$$

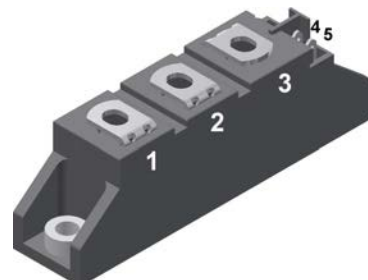
$$I_{TAV} = 85 \text{ A}$$

$$V_T = 1,18 \text{ V}$$

Phase leg

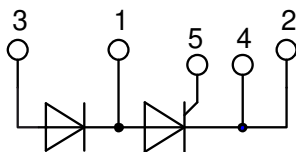
Part number

MCMA85PD1200TB



Backside: isolated

 E72873



Features / Advantages:

- Thyristor for line frequency
- Planar passivated chip
- Long-term stability
- Direct Copper Bonded Al₂O₃-ceramic

Applications:

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

Package: TO-240AA

- Isolation Voltage: 4800 V~
- Industry standard outline
- RoHS compliant
- Soldering pins for PCB mounting
- Base plate: DCB ceramic
- Reduced weight
- Advanced power cycling

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Rectifier				Ratings			
Symbol	Definition	Conditions		min.	typ.	max.	Unit
$V_{RSM/DSM}$	max. non-repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}\text{C}$				1300	V
$V_{RRM/DRM}$	max. repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}\text{C}$				1200	V
$I_{R/D}$	reverse current, drain current	$V_{R/D} = 1200\text{ V}$	$T_{VJ} = 25^{\circ}\text{C}$			100	μA
		$V_{R/D} = 1200\text{ V}$	$T_{VJ} = 140^{\circ}\text{C}$			10	mA
V_T	forward voltage drop	$I_T = 85\text{ A}$	$T_{VJ} = 25^{\circ}\text{C}$			1,21	V
		$I_T = 170\text{ A}$				1,47	V
		$I_T = 85\text{ A}$	$T_{VJ} = 125^{\circ}\text{C}$			1,18	V
		$I_T = 170\text{ A}$				1,51	V
I_{TAV}	average forward current	$T_C = 85^{\circ}\text{C}$	$T_{VJ} = 140^{\circ}\text{C}$			85	A
$I_{T(RMS)}$	RMS forward current	180° sine				135	A
V_{T0}	threshold voltage	} for power loss calculation only	$T_{VJ} = 140^{\circ}\text{C}$			0,85	V
r_T	slope resistance					3,9	m Ω
R_{thJC}	thermal resistance junction to case					0,38	K/W
R_{thCH}	thermal resistance case to heatsink				0,2		K/W
P_{tot}	total power dissipation		$T_C = 25^{\circ}\text{C}$			300	W
I_{TSM}	max. forward surge current	$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}\text{C}$			1,50	kA
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$			1,62	kA
		$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 140^{\circ}\text{C}$			1,28	kA
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$			1,38	kA
I^2t	value for fusing	$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}\text{C}$			11,3	kA ² s
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$			10,9	kA ² s
		$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 140^{\circ}\text{C}$			8,13	kA ² s
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$			7,87	kA ² s
C_J	junction capacitance	$V_R = 400\text{ V}$ $f = 1\text{ MHz}$	$T_{VJ} = 25^{\circ}\text{C}$		74		pF
P_{GM}	max. gate power dissipation	$t_p = 30\text{ }\mu\text{s}$	$T_C = 140^{\circ}\text{C}$			10	W
		$t_p = 300\text{ }\mu\text{s}$				5	W
P_{GAV}	average gate power dissipation					0,5	W
$(di/dt)_{cr}$	critical rate of rise of current	$T_{VJ} = 140^{\circ}\text{C}; f = 50\text{ Hz}$ repetitive, $I_T = 255\text{ A}$				150	A/ μs
		$t_p = 200\text{ }\mu\text{s}; di_G/dt = 0,45\text{ A}/\mu\text{s};$ $I_G = 0,45\text{ A}; V_D = \frac{2}{3} V_{DRM}$ non-repet., $I_T = 85\text{ A}$				500	A/ μs
$(dv/dt)_{cr}$	critical rate of rise of voltage	$V_D = \frac{2}{3} V_{DRM}$ $T_{VJ} = 140^{\circ}\text{C}$ $R_{GK} = \infty$; method 1 (linear voltage rise)				1000	V/ μs
V_{GT}	gate trigger voltage	$V_D = 6\text{ V}$	$T_{VJ} = 25^{\circ}\text{C}$			1,5	V
			$T_{VJ} = -40^{\circ}\text{C}$			1,6	V
I_{GT}	gate trigger current	$V_D = 6\text{ V}$	$T_{VJ} = 25^{\circ}\text{C}$			95	mA
			$T_{VJ} = -40^{\circ}\text{C}$			200	mA
V_{GD}	gate non-trigger voltage	$V_D = \frac{2}{3} V_{DRM}$	$T_{VJ} = 140^{\circ}\text{C}$			0,2	V
I_{GD}	gate non-trigger current					10	mA
I_L	latching current	$t_p = 10\text{ }\mu\text{s}$	$T_{VJ} = 25^{\circ}\text{C}$			200	mA
		$I_G = 0,45\text{ A}; di_G/dt = 0,45\text{ A}/\mu\text{s}$					
I_H	holding current	$V_D = 6\text{ V}$ $R_{GK} = \infty$	$T_{VJ} = 25^{\circ}\text{C}$			200	mA
t_{gd}	gate controlled delay time	$V_D = \frac{1}{2} V_{DRM}$	$T_{VJ} = 25^{\circ}\text{C}$			2	μs
		$I_G = 0,45\text{ A}; di_G/dt = 0,45\text{ A}/\mu\text{s}$					
t_q	turn-off time	$V_R = 100\text{ V}; I_T = 85\text{ A}; V_D = \frac{2}{3} V_{DRM}$ $T_{VJ} = 125^{\circ}\text{C}$ $di/dt = 10\text{ A}/\mu\text{s}; dv/dt = 20\text{ V}/\mu\text{s}; t_p = 200\text{ }\mu\text{s}$			150		μs

Package TO-240AA				Ratings			
Symbol	Definition	Conditions		min.	typ.	max.	Unit
I _{RMS}	<i>RMS current</i>	per terminal				150	A
T _{VJ}	<i>virtual junction temperature</i>			-40		140	°C
T _{op}	<i>operation temperature</i>			-40		125	°C
T _{stg}	<i>storage temperature</i>			-40		125	°C
Weight					81		g
M _D	<i>mounting torque</i>			2,5		4	Nm
M _T	<i>terminal torque</i>			2,5		4	Nm
d _{Spp/App}	<i>creepage distance on surface striking distance through air</i>	<i>terminal to terminal</i>	13,0	9,7			mm
d _{Spb/Apb}		<i>terminal to backside</i>	16,0	16,0			mm
V _{ISOL}	<i>isolation voltage</i>	t = 1 second	50/60 Hz, RMS; I _{ISOL} ≤ 1 mA	4800			V
		t = 1 minute		4000			V



Part description

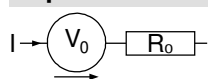
M = Module
 C = Thyristor (SCR)
 M = Thyristor
 A = (up to 1800V)
 85 = Current Rating [A]
 PD = Phase leg
 1200 = Reverse Voltage [V]
 TB = TO-240AA-1B

Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	MCMA85PD1200TB	MCMA85PD1200TB	Box	36	513043

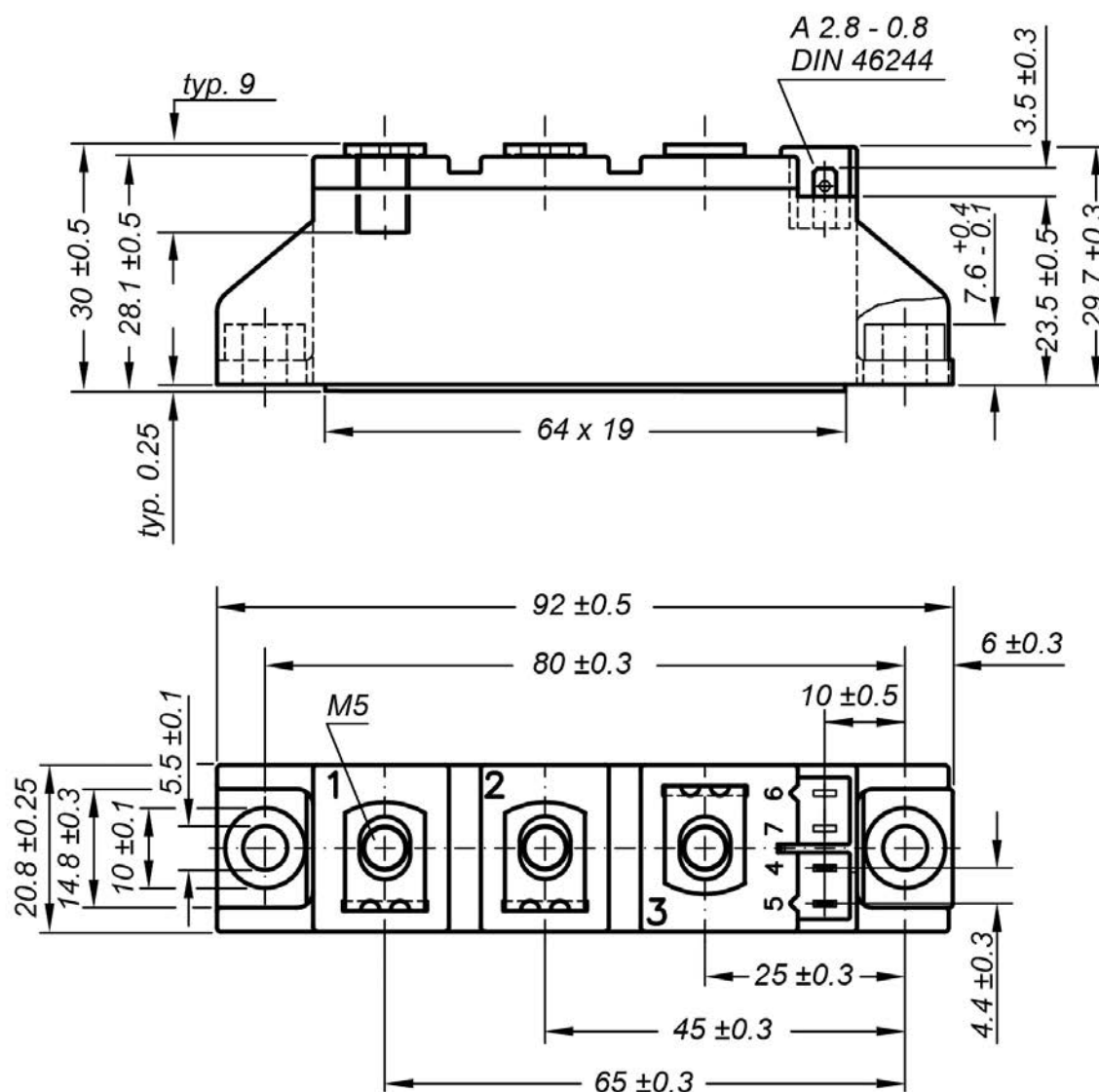
Equivalent Circuits for Simulation

* on die level

$T_{VJ} = 140^{\circ}\text{C}$

		Thyristor	
$V_{0\max}$	<i>threshold voltage</i>	0,85	V
$R_{0\max}$	<i>slope resistance *</i>	2,7	mΩ

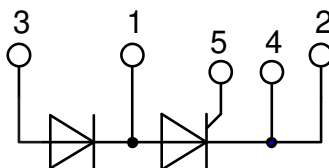
Outlines TO-240AA



Optional accessories for modules

Keyed gate/cathode twin plugs with wire length = 350 mm, gate = white, cathode = red
Type ZY 200L (L = Left for pin pair 4/5) UL 758, style 3751

Type ZY 200L (L = Left for pin pair 4/5) UL 758, style 3751



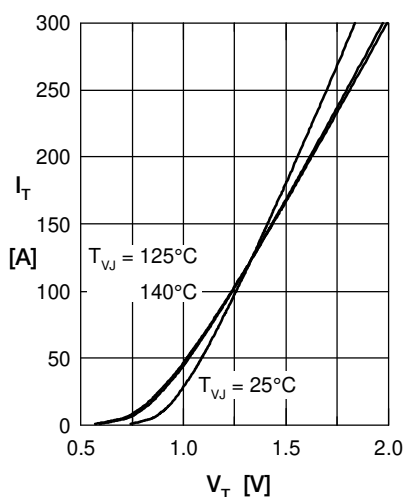
Thyristor


Fig. 1 Forward characteristics

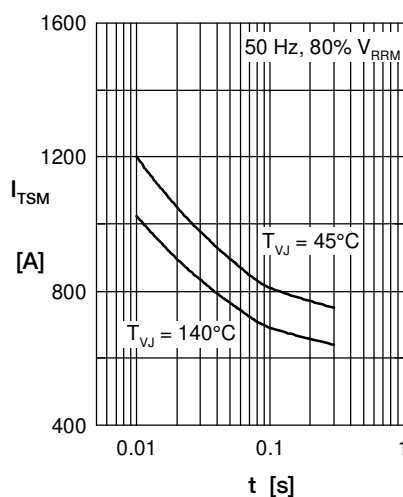
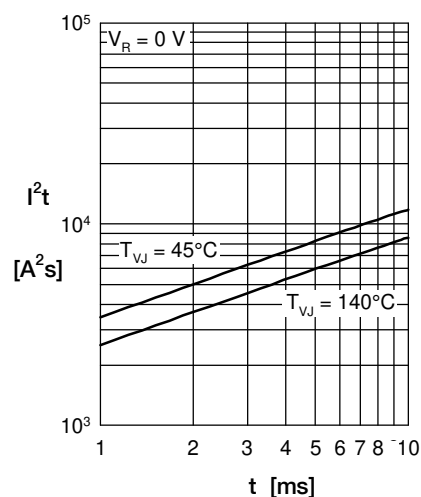
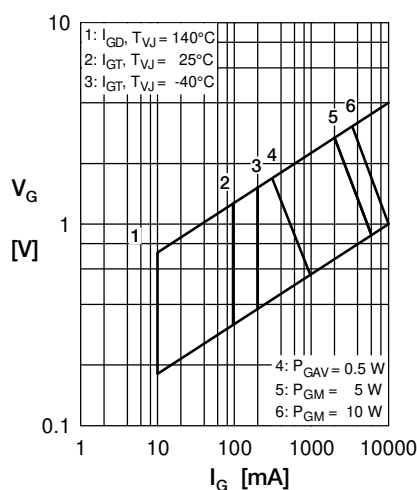

 Fig. 2 Surge overload current
 I_{TSM} : crest value, t: duration

 Fig. 3 I^2t versus time (1-10 s)


Fig. 4 Gate voltage & gate current

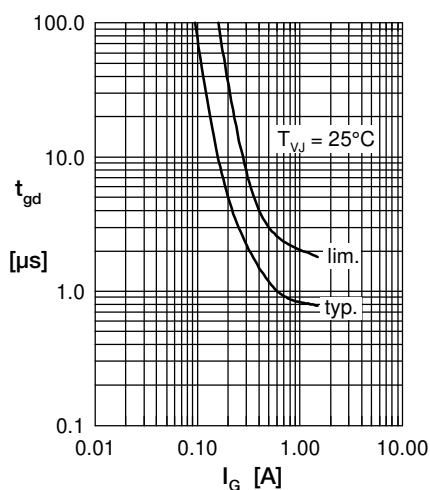
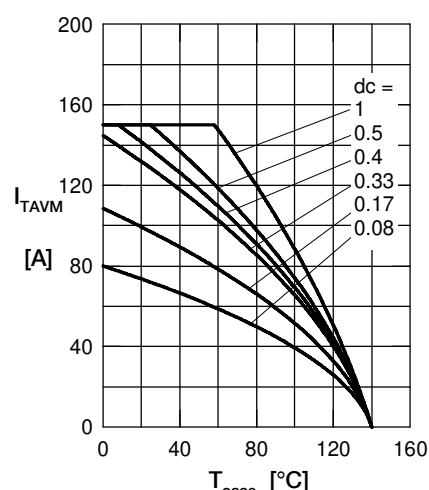

 Fig. 5 Gate controlled delay time t_{gd}


Fig. 6 Max. forward current at case temperature

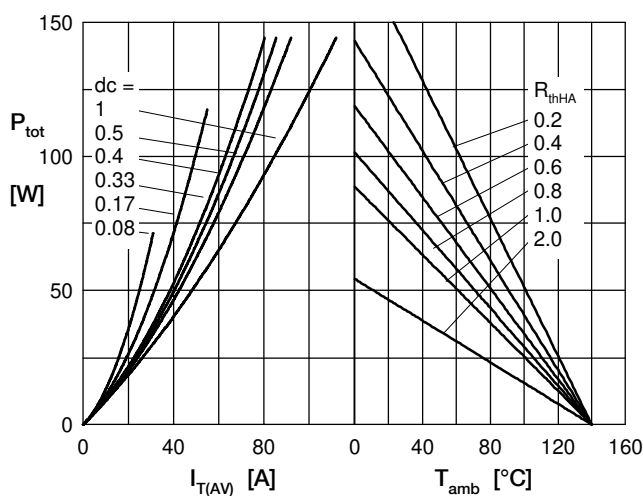
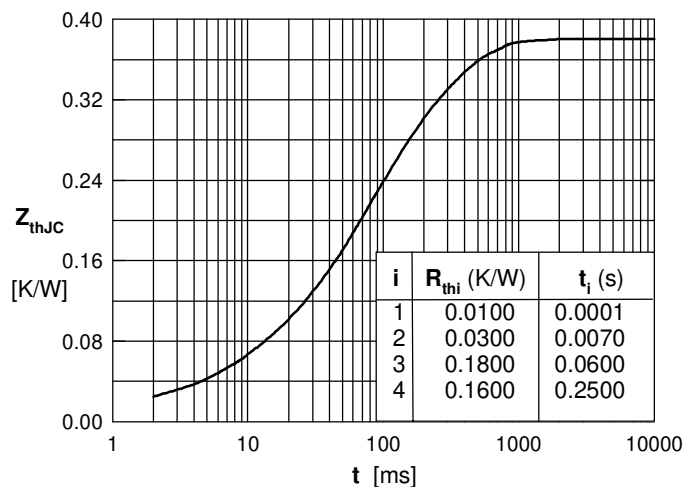

 Fig. 7a Power dissipation versus direct output current
 Fig. 7b and ambient temperature


Fig. 8 Transient thermal impedance junction to case