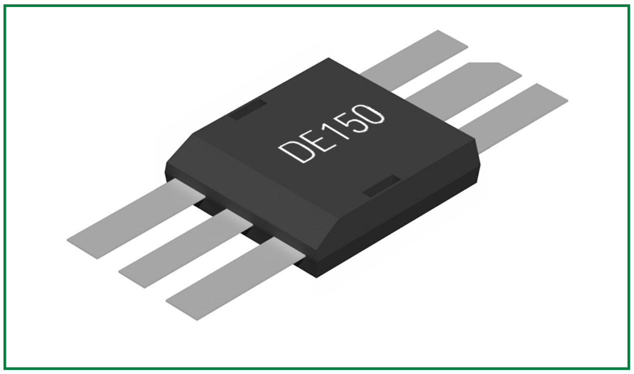
DE150-102N02A

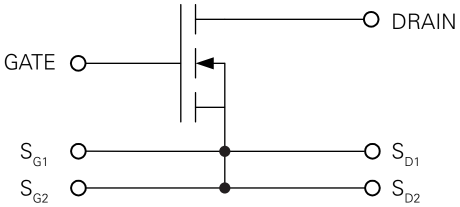
RF Power MOSFET

Key Attributes

Characteristic	Rating	Unit
V_{DSS}	1000	V
$R_{DS(on)}$	≤9.4	Ω
I_{D25}	2	A
P_{tot}	140	W



Pinout Diagram (DE150)



S_{G1}, S_{G2}: Gate side source pins

S_{D1}, S_{D2}: Drain side source pins

Description

The DE150-102N02A is a 1000V, N-channel, enhancement mode MOSFET fabricated with Littelfuse's advanced low Q_g process.

With high input impedance and a low maximum on-resistance of 9.4 Ω, the DE150-102N02A offers high power output in a small package with low input drive requirements. Low input capacitance and low gate charge enable operation at full power up to 30 MHz.

The DE150-102N02A is available in a flat, 6-lead SMD power package that incorporates an electrically isolated bottom side pad that enables efficient heat sinking.

Features

- 1000 V breakdown voltage
- 9.4 Ω maximum on-resistance
- V_{GS}: 2.5 V to 4.5 V
- $T_{vj(max.)}$: 125 °C
- High input impedance
- Electrically isolated substrate
  - High isolation voltage (> 2500 V)
  - Excellent thermal transfer
  - Increased temperature and power
- Littelfuse advanced low Q_g process
- Low gate charge and capacitances
  - Easier to drive
  - Faster switching
- Very low insertion inductance (< 2 nH)

Benefits

- High speed switching at frequencies up to 30 MHz
- Easy to mount - no insulators needed
- High power density

Ordering Information

Part Number	Description
DE150-102N02A	6-lead SMD (40/Tube)

Absolute Maximum Ratings

Characteristic	Symbol	Conditions	Value	Unit
Drain-source voltage	V_{DSS}	$T_{vj} = 25\,°C$ to $125\,°C$	1000	V
Drain-gate voltage	V_{DGR}	$T_{vj} = 25\,°C$ to $125\,°C$; $R_{GS} = 1\,M\Omega$	1000	
Gate-source voltage:				
Continuous	V_{GS}	—	±20	V
Transient	V_{GSM}		±30	
Drain current:				
Continuous	I_{D25}	$T_c = 25\,°C$	2	A
Pulse [1]	I_{DM}		12	
Repetitive avalanche current	I_{AR}		1.5	A
Repetitive avalanche energy	E_{AR}		6	mJ
Rate of rise of voltage	dV/dt	$I_S \leq I_{DM}$, $dI/dt \leq 100\,A/\mu s$, $V_{DD} \leq V_{DSS}$, $T_{vj} \leq 125\,°C$, $R_G = 0.2\,\Omega$ (External)	3	V/ns
		$I_S = 0$	>200	
Power dissipation:				
Total	P_{tot}	$T_c = 25\,°C$	140	W
Heat Sink	P_{DHS} [2]		70	
Ambient	P_{DAMB}		2.3	
Operating Temperature	T_a	—	0 to 100	°C

[1] *Pulse width limited by* $T_{vj\,(max.)}$

[2] *Derate 0.7W/°C above 25 °C*

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

Thermal Resistance

Characteristic	Symbol	Conditions	Value	Unit
Junction-to-case	$R_{th(j\text{-}c)}$	—	0.71	K/W
Junction-to-heatsink	$R_{th(j\text{-}s)}$		1.41	

Package Weight

Characteristic	Symbol	Conditions	Value	Unit
Weight (Typ.)	—	—	2	g

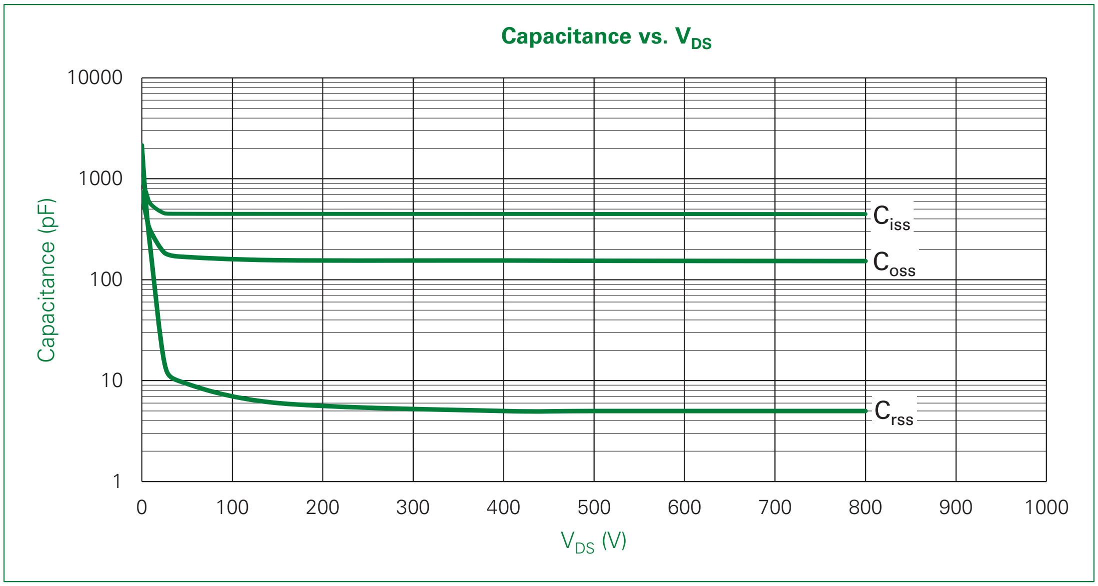
Electrical Characteristics

Unless otherwise specified, device characteristics are at $T_{vj} = 25\,°C$. Typical values are characteristic of the device at $T_{vj} = 25\,°C$ and are the result of engineering evaluations. They are provided for informational purposes only and are not part of the manufacturing testing requirements.

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Drain-source breakdown voltage	V_{DSS}	$V_{GS} = 0V$, $I_D = 3\,mA$	1000	—	—	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 4\,mA$	2.5	—	4.5	V
Gate leakage current	I_{GSS}	$V_{GS} = \pm 20V_{DC}$, $V_{DS} = 0$	—	—	±100	nA
Drain-source leakage current	I_{DSS}	$V_{DS} = 0.8\,V_{DSS}$, $V_{GS} = 0$, $T_{vj} = 25\,°C$	—	—	50	µA
		$V_{DS} = 0.8\,V_{DSS}$, $V_{GS} = 0$, $T_{vj} = 125\,°C$	—	—	500	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 15V$, $I_D = 0.5\,I_{D25}$, Pulse test: $T \le 300\,\mu s$, $D \le 2\,\%$	—	—	9.4	Ω
Forward transconductance	g_{fs}	Pulse test: $V_{DS} = 15V$, $I_D = 0.5\,I_{D25}$	0.8	2	—	S
Temperatures:						
Maximum Virtual Junction Temp.	$T_{vj(max.)}$	—	—	—	125	°C
Storage Temperature	T_{stg}	—	0	—	125	
Lead Temperature	T_L	1.6 mm (0.063 in) from case, t ≤ 10 s	—	300	—	
Gate resistance	R_G	—	—	—	5	Ω
Capacitance:						
Input	C_{iss}	$V_{GS} = 0V$, $V_{DS} = 0.8\,V_{DSS(max.)}$, f = 1 MHz	—	500	—	pF
Output	C_{oss}		—	150	—	
Reverse Transfer	C_{rss}		—	3	—	
Stray Inductance Back Metal to any Pin	C_{stray}	f = 1 MHz	—	16	—	pF
Switching speeds:						
Turn-on delay	$t_{d(on)}$	$V_{GS} = 15V$, $V_{DS} = 0.8\,V_{DSS}$ $I_D = 0.5\,I_{DM}$ $R_G = 0.2\,\Omega$ (External)	—	4	—	ns
Turn-on	t_{on}					
Turn-off delay	$t_{d(off)}$					
Turn-off	t_{off}					
Charge:						
Gate	$Q_{G(on)}$	$V_{GS} = 10V$, $V_{DS} = 0.5\,V_{DSS}$, $I_D = 0.5\,I_{D25}$	—	23	—	nC
Gate-source	Q_{GS}		—	4.5	—	
Gate-drain	Q_{GD}		—	14	—	

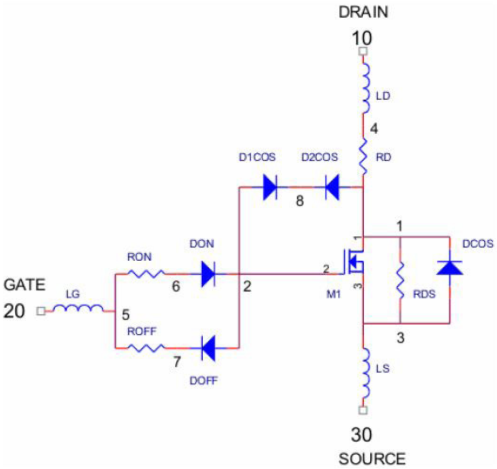
Source-Drain Diode

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Continuous source current	I_S	$V_{GS} = 0V$	—	—	1.5	A
Maximum pulsed source current	I_{SM}	Repetitive, Pulse width limited by $T_{vj(max.)}$	—	—	12	A
Forward voltage drop	V_{SD}	$I_F = I_S$, $V_{GS} = 0V$, Pulse test: $T \le 300\,\mu s$, $D \le 2\,\%$	—	—	1.8	V
Reverse recovery time	t_{rr}	—	—	710	—	ns


Capacitance vs. V_{DS}
Capacitance (pF)
10000
1000
100
10
1
0
100
200
300
400
500
600
700
800
900
1000
V_{DS} (V)
C_{iss}
C_{oss}
C_{rss}

Spice model for DE150-102N02A

The DE-SERIES SPICE Model is illustrated in Figure 1. The model is an expansion of the SPICE level 3 MOSFET model. It includes the stray inductive terms LG, LS and LD. RD is the $R_{DS(on)}$ of the device, RDS is the resistive leakage term. The output capacitance, C_{oss}, and reverse transfer capacitance, C_{rss}, are modeled with reversed biased diodes. This provides a varactor type response necessary for a high power device model. The turn on delay and the turn off delay are adjusted via RON and ROFF.



Net List:

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*SYM=POWMOSN
.SUBCKT 102N02A 10 20 30
* TERMINALS: D G S
* 1000 Volt 1.4 Amp 9.4 ohm N-Channel Power MOSFET 10-30-2000
M1 1 2 3 3 DMOS L=1U W=1U
RON 5 6 4.0
DON 6 2 D1
ROF 5 7 2.0
DOF 2 7 D1
D1CRS 2 8 D2
D2CRS 1 8 D2
CGS 2 3 500Pf
RD 4 1 9.4
DCOS 3 1 D3
RDS 1 3 5.0MEG
LS 3 30 .5N
LD 10 4 1N
LG 20 5 1N
.MODEL DMOS NMOS (LEVEL=3 VTO=3 KP=.3)
.MODEL D1 D (IS=.5F CJO=10P BV=100 M=.5 VJ=.2 TT=1N)
.MODEL D2 D (IS=.5F CJO=100P BV=1000 M=.6 VJ=.6 TT=1N RS=10M)
.MODEL D3 D (IS=.5F CJO=150P BV=1000 M=.35 VJ=.6 TT=400N RS=10M)
.ENDS
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Manufacturing Information

Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. Littelfuse classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
DE150-102N02A	MSL 1

ESD Sensitivity

This product is ESD Sensitive, and should be handled according to the industry standard **JESD-625**.

Soldering Profile

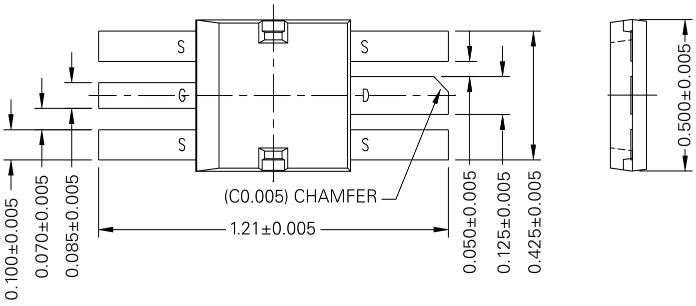
Provided in the table below is the **IPC/JEDEC J-STD-020** Classification Temperature (T_C) and the maximum dwell time the body temperature of these surface mount devices may be (T_C – 5) °C or greater. The Classification Temperature sets the Maximum Body Temperature allowed for these devices during reflow soldering processes.

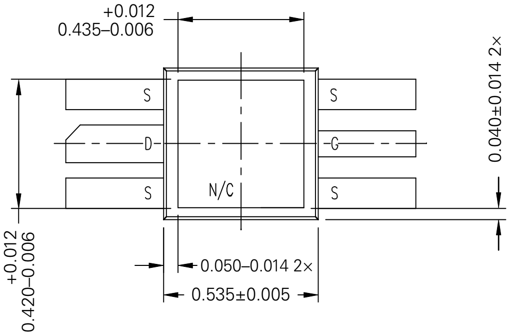
Device	Classification Temperature (T_c)	Dwell Time (t_P)	Maximum Reflow Cycles
DE150-102N02A	260 °C	30 seconds	3

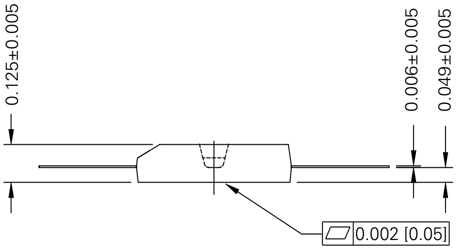
Board Wash

Littelfuse recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: Using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to halide flux or solvents.

Mechanical Dimensions







N/C – DCB metalized bottom heatsink.
2500 V_{RMS} AC, 1 minute isolation to leads.
LEADS – Pre-full silver plated (1.5–4 µm).
BOTTOM SIDE OF DCB – Pre Ni plated (2–6 µm).