Holistic Approach to Maximize Lifetime and Power Density in High Power Semiconductor Modules

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Abstract

The challenge in power electronics is, to achieve higher power throughput in smaller housings using less resources while increasing efficiency and reduce cost. As these targets have contradicting solutions, compromises need to be chosen. Higher currents increase the thermal stress in a given device, reducing its lifetime. To counteract, exchanging IGBTs using wide band gap SiC-MOSFETs is considered. However, the solution becomes more expensive in turn. Adapting an approach as done in press-pack-devices and allow electrically active heat sinks opens the path to massive improvement. The present work shows how this can be done in IGBT-based designs.

1 Comparing power modules and disc-style devices

Increasing power density always causes increased losses per area and thus typically higher temperatures. In turn, higher stress appears to interconnecting joints which recently lead to the replacement of soft-soldered connections by sintering [1]. Higher stability of the interconnecting technology can counteract the lifetime-reduction that results from higher temperature swings.

Another obvious solution countering stress due to temperature changes is improved cooling. Today, when building power semiconductors with insulating DCBs, the ceramic layers involved pose a physical limit to thermal transfer. A sketch of a power semiconductor module as it is built today is given in Fig. 1.

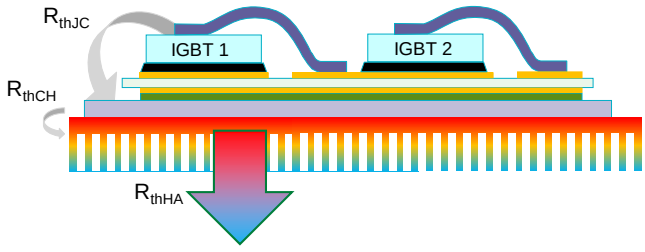

Fig. 1 Power semiconductor setup using DCBs for insulation

As a rule of thumb, any material that features electrical isolation also is a bad thermal conductor.
In contrast to power semiconductor modules, high-power disc-devices are often combined with electrically active cold-plates as higher performing cooling systems. A correlating stack-assembly along with a detailed view is given in Fig. 2:

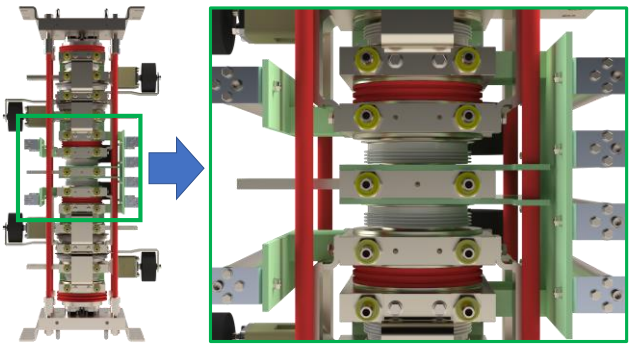

Fig. 2 3-Level IGBT-stack using electrically active cold-plates

The stack forms a 2400 A / 4500 V 3-level phase-leg [2]. The aluminum-made cold-plates are electrically active and additionally serve as terminals to the disc-devices and connecting point for snubber circuits, thus contributing to material savings and space reduction.

Consequently, a non-conducting cooling liquid must be used, typically a deionized water-glycol mixture.

2 Feasibility study

To eliminate the dominating thermal resistance of the DCB's ceramic, a different solution was followed. In this, the IGBT-dies rated 1200 V/200 A are directly soldered to a suitable liquid cooled plate. This way, the cold-plate becomes the electric connection to the IGBT's collector and isolated islands in the design are solely required to mount the power-terminal at the emitter-side as well as the control-terminals. Using bond-wires to connect the individual parts in the setup was the obvious choice which led to a first device under test (DUT) as presented in Fig. 3.

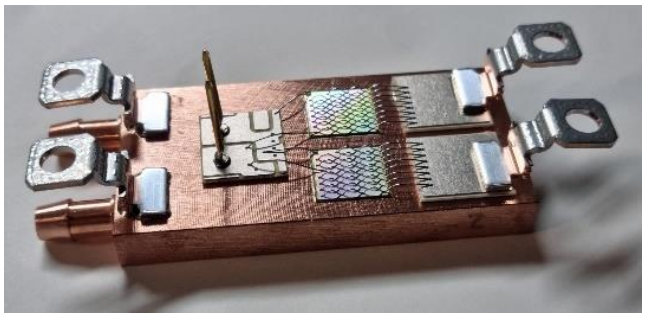

Fig. 3 First device for feasibility study and thermal measurements

The die used in this first scheme is a 200 A IGBT with a size of approximately 200 mm². Eight bond-wires with 25 A current carrying capability were used per die to connect the emitters to the power terminals.
The device was blackened to conduct thermal measurements using infrared imaging. Current was applied from a laboratory supply, liquid cooling flowrate was set to about 6 L/min. Fig. 4 is a close-up view to the DUT within the setup.

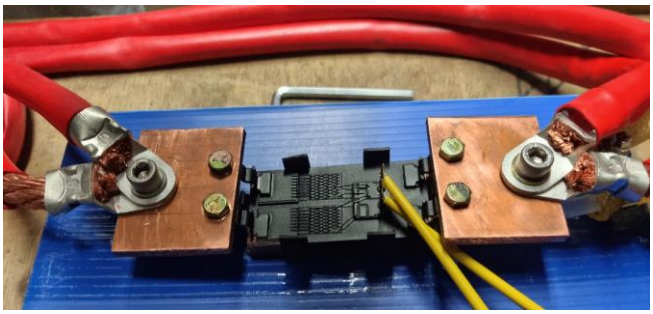

Fig. 4 DUT prepared for thermal imaging

The DUT is powered from a high-current, low-voltage source, capable to deliver 1 kA at 10 V. This way, safety precautions only are concerned with high temperatures but not with high voltages.
It was expected that the 200 A-chip remains well below it's thermal limits of 150°C even with much higher currents than 200 A being applied.

Conducting the experiment started with just 50 A and was repeated after increasing the current in 50 A-steps.

Reaching the rated chip current of 200 A, the die-temperature rose by about 70 K, leaving a margin for further 50 K before the maximum temperature of 150°C would be reached. However, with 25 A per bond wire another physical limit is reached as the bond wires' temperature already exceeded 400°C. The IR-image at 200 A per die can be seen in Fig. 5.

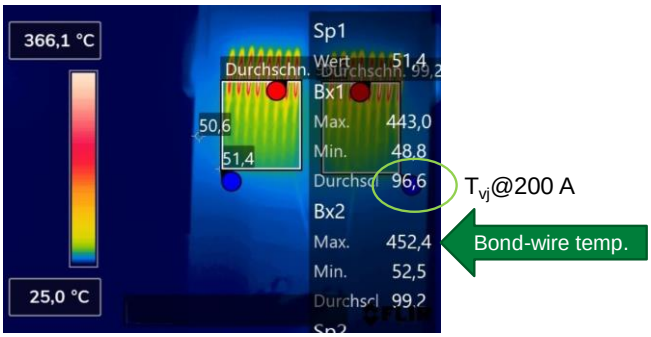

Fig. 5 Thermal image taken at 200 A per die

Continuing the experiment by increasing the current, the bond wires fused at 250 A per die.

Very clearly, the assembly technology in such an approach becomes the weak link and a second approach was done using clip-soldered connections instead of bond wires.

This is only possible due to a new solderable chip-metallization applied to the emitter of the die.

Figure 6 is a photo of the second device, **Fig. 7** reveals the thermal development at 200 A per die, measured within the same setup as before.

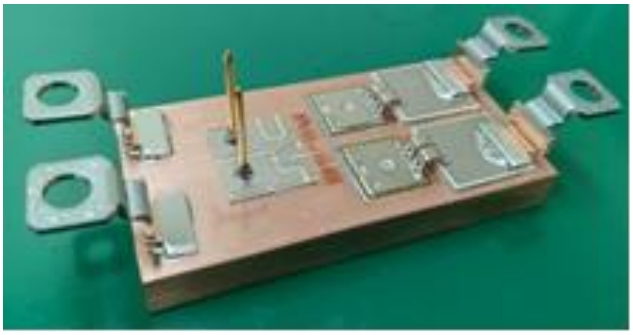

Fig. 6 DUT Version 2 with clip-soldered connections instead of bond wires

With this new construction, the chip temperature at 200 A reached 94°C while the connecting clip remained at a maximum temperature of 78°C and thus about 370°C below the bond wires' temperature in the previous design.

Operating temperature of T_{vj} = 150°C was reached with a current exceeding 275 A.

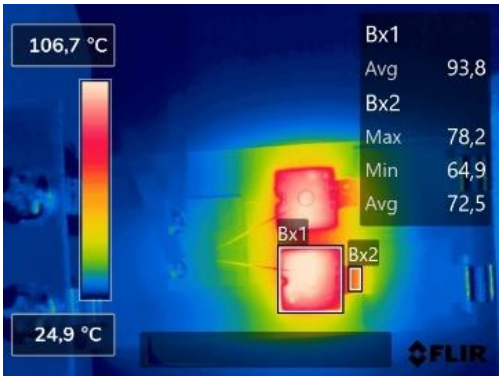

Fig. 7 Thermal result at 200 A in the clip-soldered device

It is obvious, that the limitation imposed by using bond-wires has been removed. The clip's temperature remains well below 100°C which is about 350 K less than what was observed on the bond-wires.

As the IGBTs used in the two DUT were not identic, a direct comparison based on current only is not revealing the true picture. DUT1 was equipped with a chip designed for 200 A rated current and very low forward voltage of only 1.2 V at rated current. The transfer characteristic of the die used is displayed in Fig. 8.

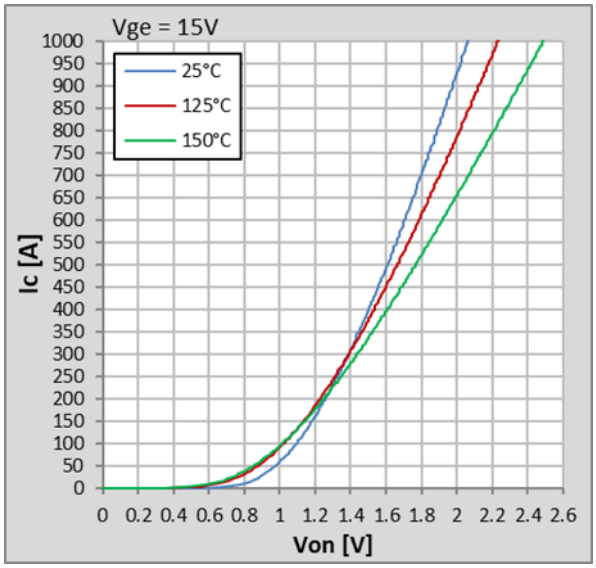

Fig. 8 Transfer Characteristic of the newly developed 200 A-IGBT

A special feature of the chip is the high ratio between desaturating current and rated current. Typical IGBT-designs desaturate in a range of four to five times the rated current. This new chip won't desaturate below six to eight times it's nominal current. It becomes obvious, that exploiting this feature to the full potential would lead to power loss densities easily exceeding 600 W/cm². This assumes operation at 650 A, resulting in 2 V forward voltage and 1300 W of losses on a 200 mm² die.

As this die does not feature a solderable front-side metallization, it was not an option to be used in the second DUT.

Instead, a standard die upgraded with a solderable metallization but a lower current rating of only 150 A rated current was used.

Besides the different chip area of only 183 mm², the forward voltage characteristic of the chip is different as is seen in Fig. 9.

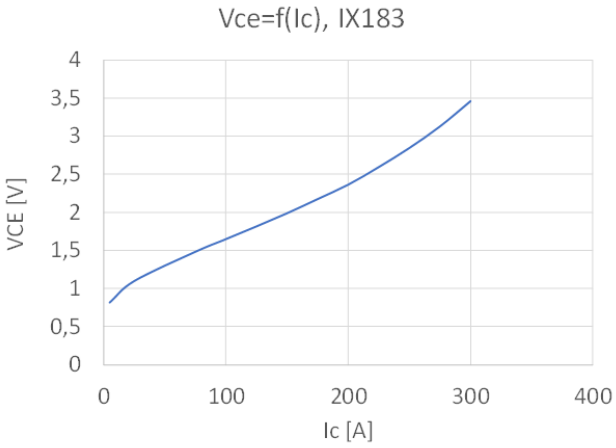

Fig. 9 Forward characteristic of the IX183-IGBT

Therefore, a fair analysis can best be done considering power loss density [W/cm²] or be condensed in the thermal resistance calculated from both trials.

From the measurement done, a thermal transfer capability of the setup was calculated, allowing power-loss-densities of up to 380 W/cm² at a temperature swing of 100 K. This represents the difference between a maximum junction temperature of 175°C and an inlet temperature of the cooling liquid of 65°C.

For the newly designed chip with 2 cm² area, this allows to handle 760 W per die, leading to a maximum current of 450 A.

The 150 A /183 mm² standard die could be operated within it's thermal limits carrying up to 250 A.

3 Electric testing

Though the focus of the study was on the thermal performance, the basic electrical behaviour of the setup was also tested.

The result from a double-pulse-test is summarized in Fig. 10.

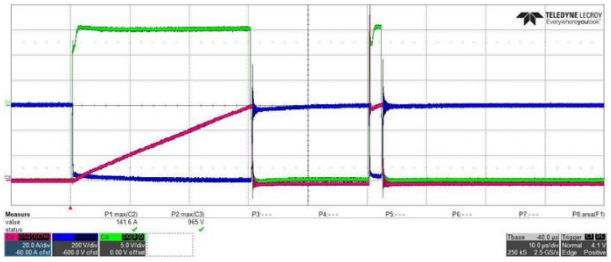

Fig. 10 Results from the dynamic testing in double-pulse test equipment

The tests revealed a sufficiently clean switching but due to the nature of the test setup, no further details were investigated. Though the layout of the devices studied was not optimized for switching and a perfect switching behaviour was not expected, the results were still good enough to later be transferred into a potential series-development.

4 Cyclic load testing

The outstanding thermal performance is a key factor in increasing the lifetime of a power electronic component.
From the second design, several devices were subjected to a power cycling test (PC_{sec}) as defined in IEC 60749 [2].

The expectation was that the pad-and-clip assembly achieves a higher lifetime than a system using bond-wires as the failure mechanisms of bond-lift-off and bond-heel-crack are eliminated. However, as the pad is soldered to the chip's front-side, delamination of this interface is expected to happen eventually.

The test was conducted with an inlet temperature of 12°C. In a cycle of 4 seconds with 50% duty-cycle, the chip temperature swing observed was 90 K with a load current of 250 A.

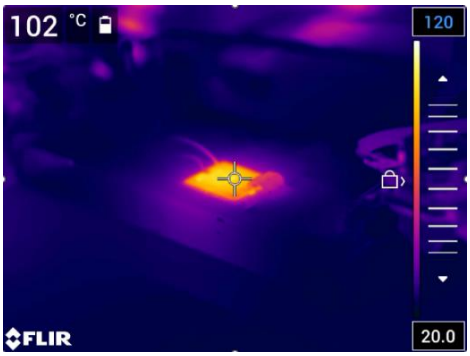

Fig. 11 Thermal image of the chip during PC_{sec}-Test

As only very few DUTs were available, the chips were tested in a single arrangement.

Figure 11 reveals the outstanding thermal performance achieved and the low spreading of heat within the cold-plate.

The results from the long-term test conducted are summarized in the graph in Fig. 12.

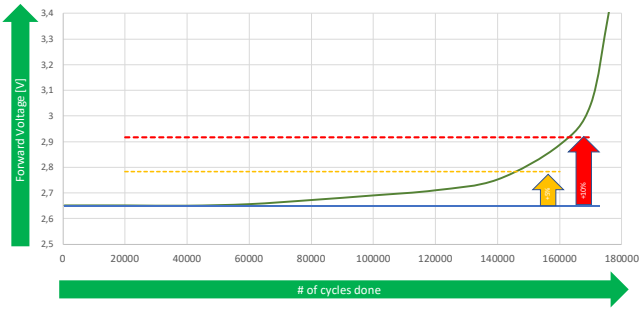

Fig. 12 Results from PC_{sec}-Testing

It remains to be noted, that the IGBT in this test had a rated chip current of only 150 A, so despite staying within the given thermal limits for chip temperature, the chip was operated well beyond parameters that would be used in a real-world application.

The end-of-life criteria for this test is an increase of the forward voltage of 5%. This value was reached after roughly 145.000 cycles. Classical solder-bond-technology reaches about 80.000 cycles under these conditions. As further potential for improvement is seen in the chip metallization as well as in solder alloys and solder processes, achieving at least twice the power-cycling capability compared to solder-bond devices does seem reasonable.

5 Applications in focus and resulting benefits

From the structure chosen and power density achieved, it is obvious, that such a design is meant to operate in a high-power application.
Especially applications that already feature liquid cooling and demand high power throughput can benefit from a non-insulated power semiconductor arrangement.
Main targets for such an approach can be found in renewable energy generation in windmills or in the steel industry in metal melting or metal welding by induction heating.
With the heat sink forming the connection to the IGBT's collector, the scheme is a good choice for building single switches with high current carrying capabilities to replace existing designs based on current power modules with the same single-switch topology.

What could potentially be achieve can be estimated from the rendered image in Fig. 13.

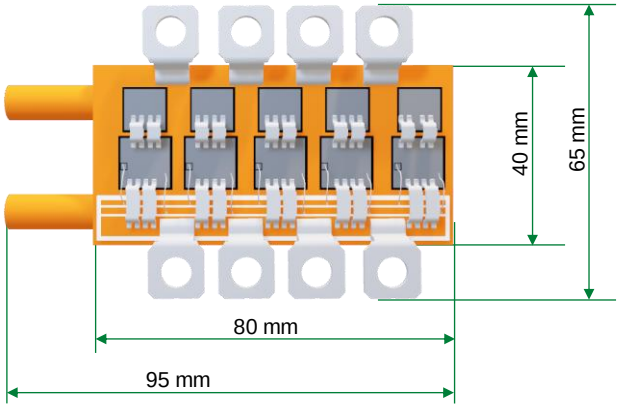

Fig. 13 1200 A-Device in non-isolated setup

Equipped with a 250 A-chipset, this version resembles a 1200 A single switch with an envelope of 123.5 cm³.
A half-bridge consisting of two such devices consumes about 250 cm³ of space. In comparison, common high-power modules used today demand up to 700 cm³ [3].
Besides single switch arrangements, the setup is also a good replacement when building bidirectional switches as used in DC-circuit breakers in battery-charging or UPS-systems as well as AC-circuit breakers.
A further benefit arising from the integrated liquid cooling is, that the necessary surrounding housing is no longer burdened with the high temperatures commonly seen in power semiconductors. This opens a path to use lower-grade plastics, potentially even materials that are easy to recycle, which will be a major topic in the years ahead.
In contrast to the classical approach, the terminals also benefit from the intense cooling, reducing the heat that is transferred to surrounding components like DC-link capacitors.
As for the use of resources, a half-bridge built from the device in Fig. 13 has a mass below 0.7 kg which is less than half the weight of a current design.
Sacrificing a fraction of the performance by replacing the copper heat sink using aluminum would allow for both, cost and weight reduction.

Conclusions

The omnipresent trend of increasing power density in power semiconductors as they are built today starts reaching physical limits due to the isolation requirement. To push these limits further, new methods to extract heat from power semiconductors more efficiently need to be identified.

One way of doing so is direct liquid cooling combined with a suitable chip- and interconnection technology as presented.

The shift from classical isolated assemblies to non-isolated counterparts opens the door to increase power density by a factor of 10, compared to today's options.

6 Reference

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