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White **Paper**

Holistic Approach to Maximize Lifetime and Power Density in High Power Semiconductor Modules

Abstract

The challenge in power electronics is to achieve higher power throughput in smaller housings, using fewer resources, while increasing efficiency and reducing cost. As these targets involve contradicting solutions, compromises must be made. Higher currents increase thermal stress in a given device, reducing its lifetime. To counteract this, exchanging IGBTs with wide band gap SiC-MOSFETs is considered. However, the solution tends to be more expensive. Adopting an approach similar to that used in press-pack-devices and allowing electrically active heat sinks opens the path to massive improvement. This paper demonstrates how this concept can be applied to IGBT-based designs.

1. Comparing Power Modules and Disc-style Devices

Increasing power density always causes increased losses per area and, consequently, higher temperatures. This, in turn, places greater stress on interconnecting joints which has recently led to the replacement of soft-soldered connections by sintering [1]. Higher stability of the interconnecting technology can counteract the reduction in lifetime caused by larger temperature swings.

Another obvious solution to counter stress from temperature changes is improved cooling. Today, when building power semiconductors with insulating DCBs, the ceramic layers involved impose a physical limit on thermal transfer. A sketch of a power semiconductor module, as it is currently built, is given in Figure 1.

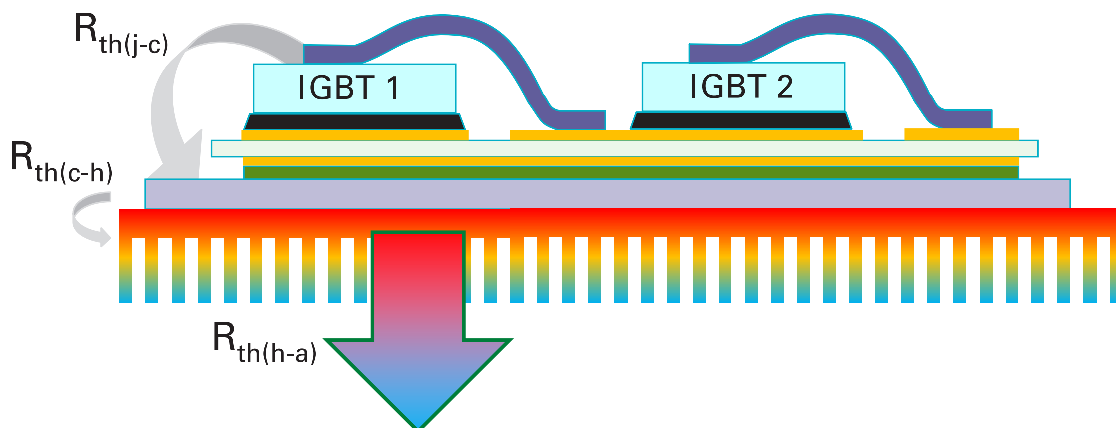

Figure 1.Power semiconductor setup using DCBs for insulation

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As a rule of thumb, any material that features electrical isolation is typically a poor thermal conductor. In contrast to power semiconductor modules, high-power disc-devices are often combined with electrically active cold-plates, which serve as more efficient cooling systems. A corresponding stack-assembly, along with a detailed view, is displayed in Figure 2.

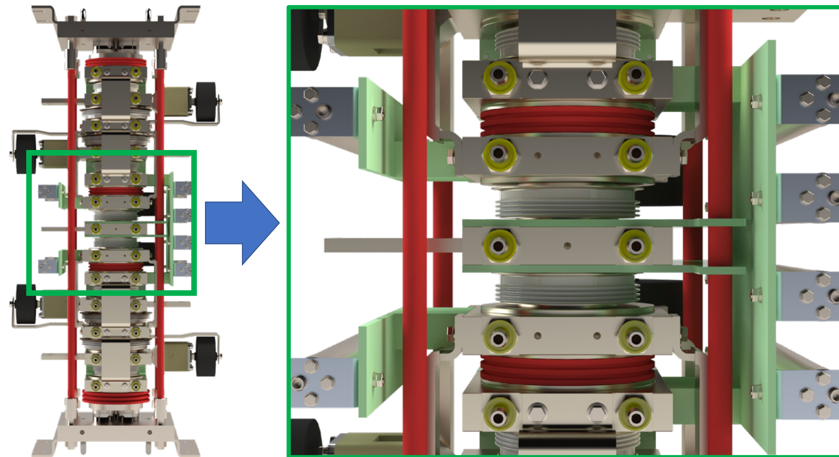

Figure 2.3-level IGBT-stack using electrically active cold-plates

The stack forms a 2400 A / 4500 V 3-level phase-leg [4]. The aluminum-made cold plates are electrically active and additionally serve as terminals for the disc-devices and connection points for snubber circuits, thereby contributing to material savings and space reduction. Consequently, a non-conducting cooling liquid must be used, typically a deionized water-glycol mixture.

2. Feasibility Study

To eliminate the dominating thermal resistance of the DCB's ceramic, a different solution was followed. In this approach, IGBT dies rated 1200 V/200 A are directly soldered to a suitable liquid-cooled plate. This allows the cold plate to serve as the electrical connection to the IGBT's collector, while isolated islands in the design are only required for mounting the power terminal at the emitter-side and the control terminals. Using bond wires to connect the individual parts in the setup was the obvious choice, which led to the development of the first device under test (DUT), as presented in Figure 3.

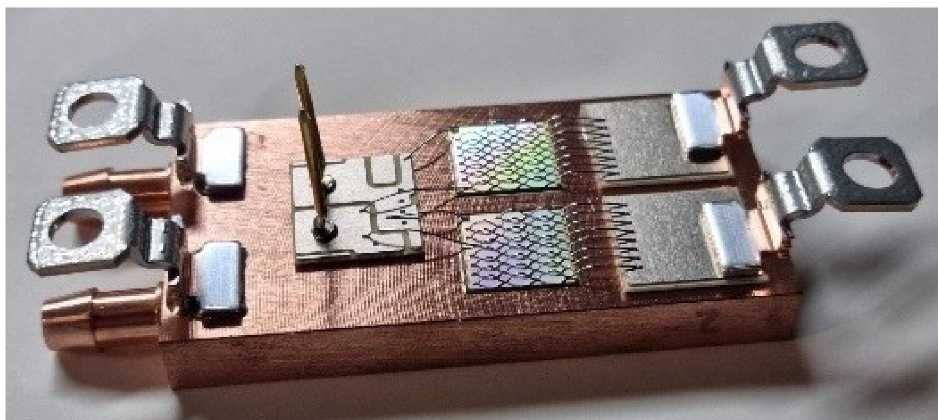

Figure 3. First device for feasibility study and thermal measurements

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The die used in this initial setup is a 200 A IGBT with an approximate size of 200 mm². Eight bond wires with 25 A current-carrying capability were used per die to connect the emitters to the power terminals.

The device was blackened to conduct thermal measurements using infrared imaging. Current was applied from a laboratory supply and the liquid cooling flow rate was set to approximately 6 L/min. Figure 4 is a close-up view of the DUT within the setup.

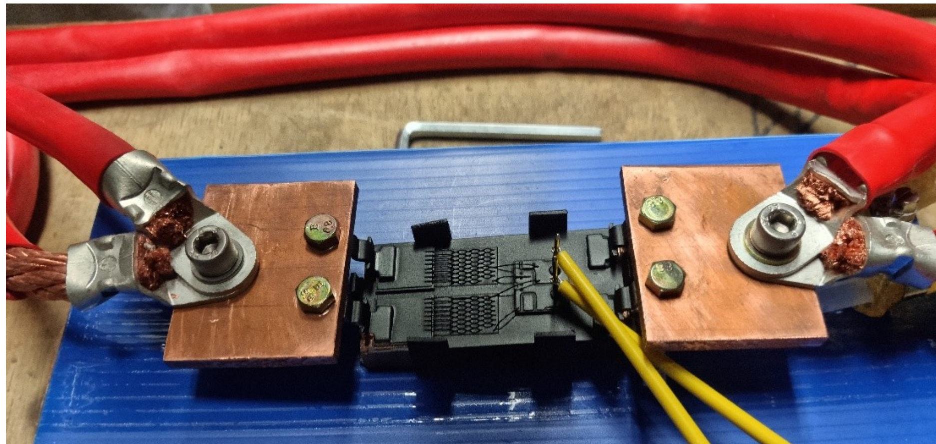

Figure 4. DUT prepared for thermal imaging

The DUT is powered from a high-current, low-voltage source, capable of delivering 1 kA at 10 V. This way, safety precautions focus solely on high temperatures and not on high voltages. The 200 A-chip was expected to remain well below its thermal limits of 150 °C, even with much higher currents than 200 A being applied.

The experiment began with a current of 50 A and was repeated in 50 A increments. Upon reaching the rated chip current of 200 A, the die temperature rose by approximately 70 K, leaving a margin of a further 50 K before the maximum allowable temperature of 150 °C would be reached. However, with 25 A per bond wire, another physical limit was encountered, as the bond wire temperature exceeded 400 °C. The I_R image at 200 A per die can be seen in Figure 5.

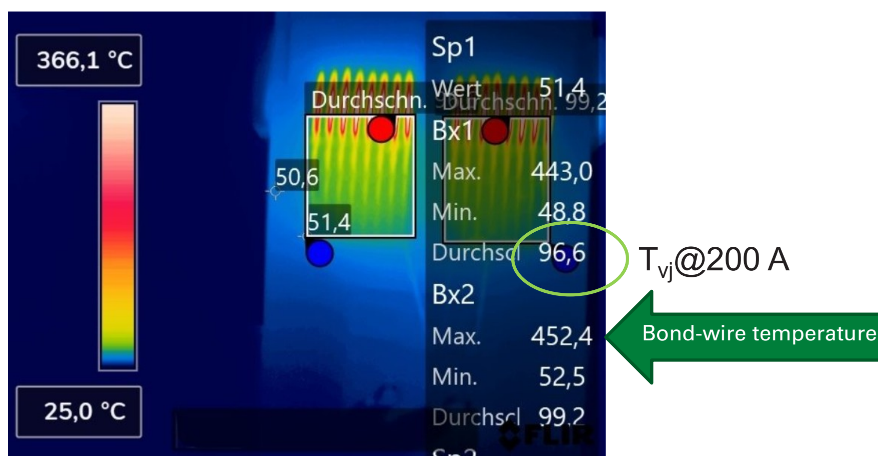

Figure 5. Thermal image taken at 200 A per die

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Continuing the experiment by increasing the current, the bond wires fused at 250 A per die. Clearly, the assembly technology in such an approach becomes the weak link. As a result, a second approach was implemented using clip-soldered connections instead of bond wires. This was made possible by a new solderable chip-metallization applied to the emitter of the die.

Figure 6 is a photo of the second device, while Figure 7 reveals the thermal development at 200 A per die, measured using the same setup as before.

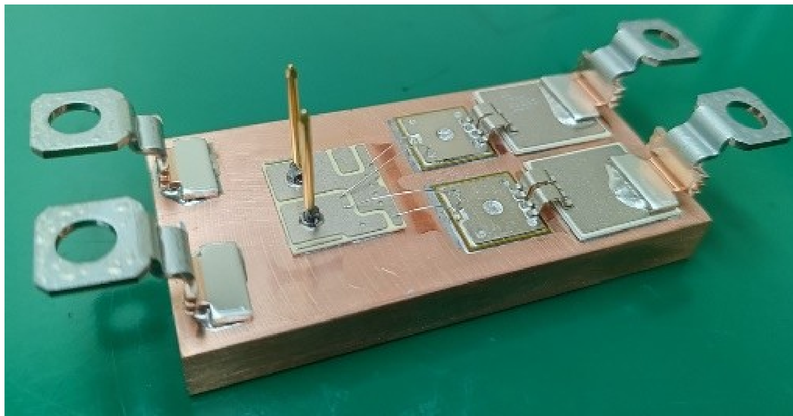

Figure 6. DUT version 2 with clip-soldered connections instead of bond wires

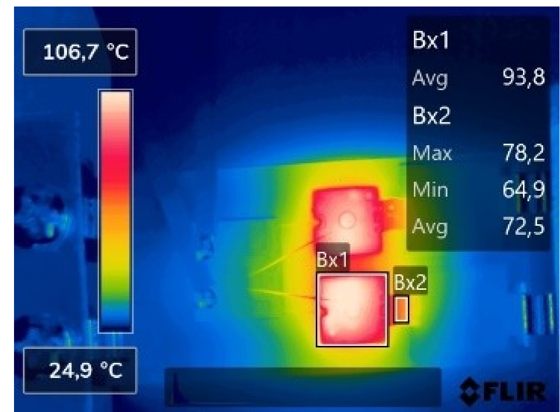

Figure 7. Thermal result at 200 A in the clip-soldered device

With this new construction, the chip temperature at 200 A reached 94 °C, while the connecting clip remained at a maximum temperature of 78 °C and thus about 370 °C below the bond wire temperature in the previous design. The operating temperature of T_{vj} = 150 °C was reached with a current exceeding 275 A.

It is obvious that the limitation imposed by using bond wires was eliminated. The clip's temperature remained well below 100 °C, which is about 350 K lower than what was observed with bond wires. However, as the IGBTs used in the two DUTs were not identical, a direct comparison based solely on current does not provide a complete picture. DUT1 was equipped with a chip designed for a rated current of 200 A and a very low forward voltage of only 1.2 V at rated current. The transfer characteristic of the die used is displayed in Figure 8.

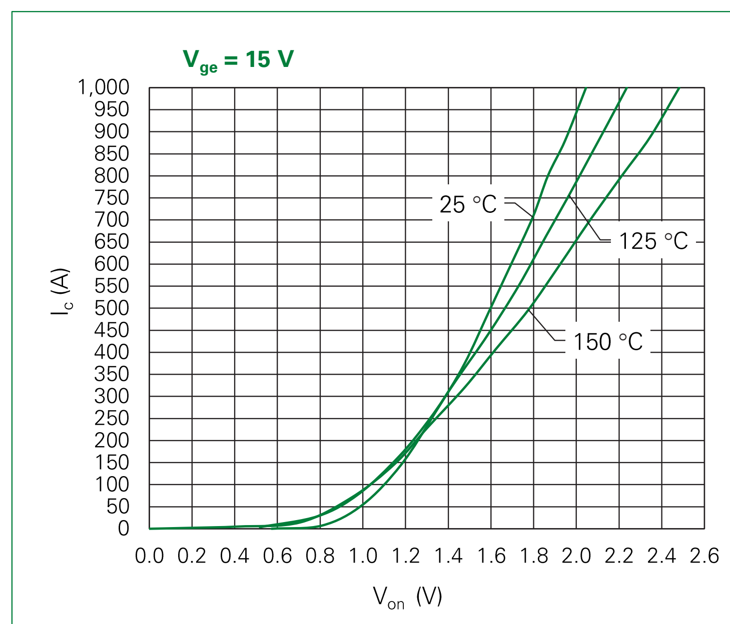

Figure 8. Transfer characteristic of the newly-developed 200 A-IGBT

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A special feature of the chip is the high ratio between desaturating current and rated current. Typical IGBT designs desaturate at four to five times the rated current. In contrast, this new chip does not desaturate below six to eight times its nominal current. It is evident that exploiting this feature to the full potential would lead to power loss densities easily exceeding 600 W/cm². This assumes operation at 650 A, resulting in a forward voltage of 2 V and 1300 W of losses on a 200 mm² die.

As this die does not feature a solderable front-side metallization, it was not suitable for use in the second DUT. Instead, a standard die upgraded with a solderable metallization, but with a lower rated current of only 150 A, was used. In addition to the different chip area of only 183 mm², the forward voltage characteristic of the chip differs, as is seen in Figure 9.

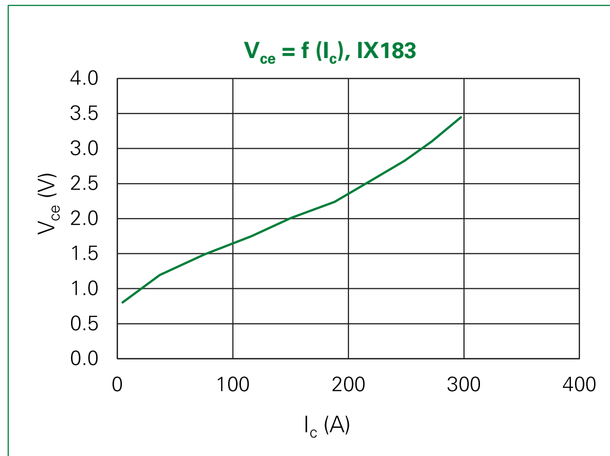

Figure 9. Forward characteristic of the IX183-IGBT

Therefore, a fair analysis can best be performed by considering the power loss density [W/cm²] or by summarizing the results in terms of the thermal resistance calculated from both trials. From the measurement done, a thermal transfer capability of the setup was calculated, allowing power-loss densities of up to 380 W/cm² at a temperature swing of 100 K. This represents the difference between a maximum junction temperature of 175 °C and an inlet temperature of the cooling liquid of 65 °C.

For the newly designed chip with 2 cm² area, this allows for handling 760 W per die, leading to a maximum current of 450 A. The 150 A /183 mm² standard die could be operated within its thermal limits carrying up to 250 A.

3. Electric Testing

Though the focus of the study was on thermal performance, the basic electrical behaviour of the setup was also tested. The results from a double-pulse test are summarized in Figure 10.

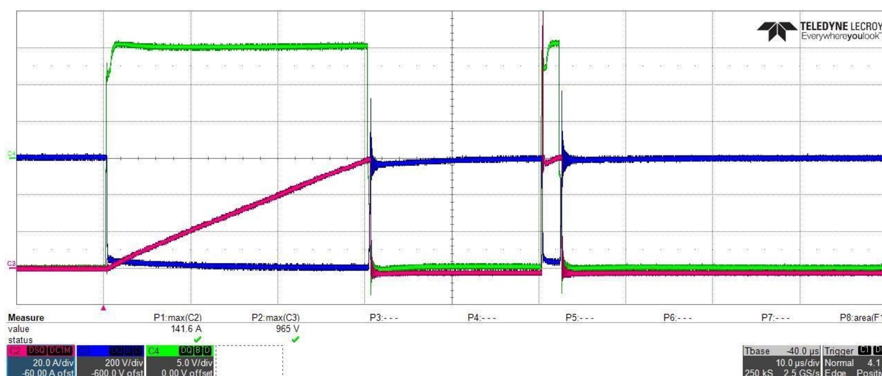

Figure 10.Results from the dynamic testing in double-pulse test equipment

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The tests revealed sufficiently clean switching behavior; however, due to the nature of the test setup, no further details were investigated. Though the layout of the devices studied was not optimized for switching, and perfect switching behaviour was not expected, the results were still promising enough to be considered for potential series-development.

4. Cyclic Load Testing

The outstanding thermal performance is a key factor in increasing the lifetime of a power electronic component. In the second design, several devices were subjected to a power cycling test (PCsec) as defined in IEC 60749 [2]. It was expected that the pad-and-clip assembly would achieve a longer lifetime than a system using bond wires, as the failure mechanisms of bond lift-off and bond heel-cracking are eliminated. However, because the pad is soldered to the chip's front side, delamination of this interface is anticipated over time.

The test was conducted with an inlet temperature of 12 °C. In a 4-second cycle with a 50% duty cycle, a chip temperature swing of 90 K was observed at a load current of 250 A.

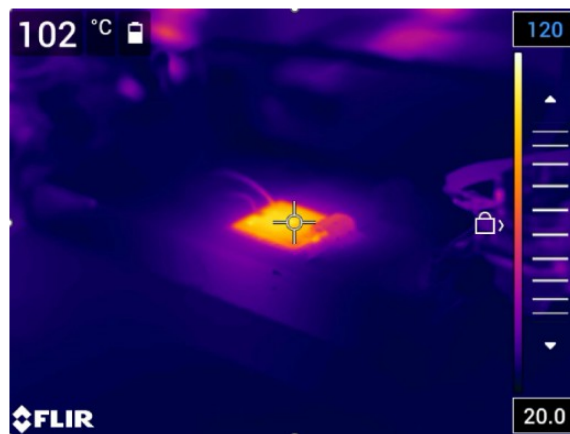

Figure 11. Thermal image of the chip during PC_{sec} – Test

Due to the limited availability of DUTs, the chips were tested in a single arrangement. Figure 11 illustrates the outstanding thermal performance achieved and the low spreading of heat within the cold plate. The results from the long-term test conducted are summarized in the graph in Figure 12.

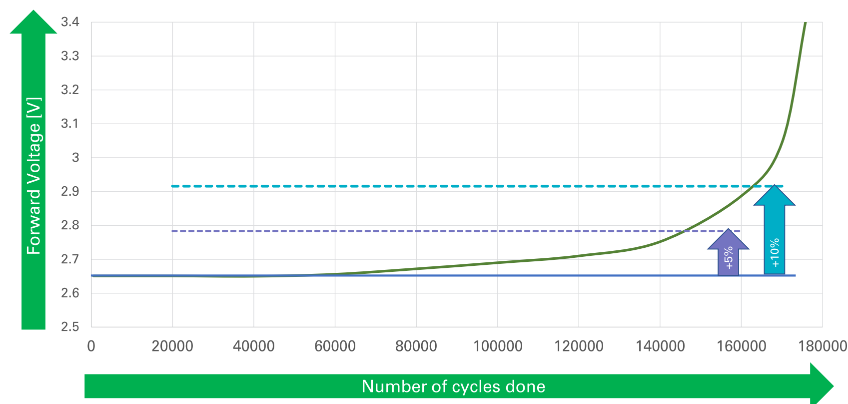

Figure 12. Results from PC_{sec} – Testing

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It is important to note that the IGBT used in this test had a rated chip current of only 150 A. Therefore, despite staying within the given thermal limits for chip temperature, the chip was operated well beyond parameters that would be used in a real-world application.

The end-of-life criterion for this test was defined as a 5% increase in forward voltage. This value was reached after approximately 145,000 cycles. In comparison, classical solder-bond technology reaches about 80,000 cycles under similar conditions. Given the potential for further improvements in chip metallization, solder alloys, and soldering processes, it seems reasonable to expect at least twice the power cycling capability compared to solder-bonded devices.

5. Applications in Focus and Resulting Benefits

From the structure chosen and power density achieved, it is obvious that such a design is meant to operate in a high-power application. In particular, applications that already feature liquid cooling and demand high power throughput can benefit from a non-insulated power semiconductor arrangement.

Primary target applications for this approach include renewable energy generation in windmills and metal melting or metal welding by induction heating in the steel industry. With the heat sink forming the connection to the IGBT's collector, the scheme is a good choice for building single switches with high current-carrying capabilities, offering a replacement for existing designs based on current power modules with similar single-switch topologies. The potential of this concept can be estimated from the rendered image in Figure 13.

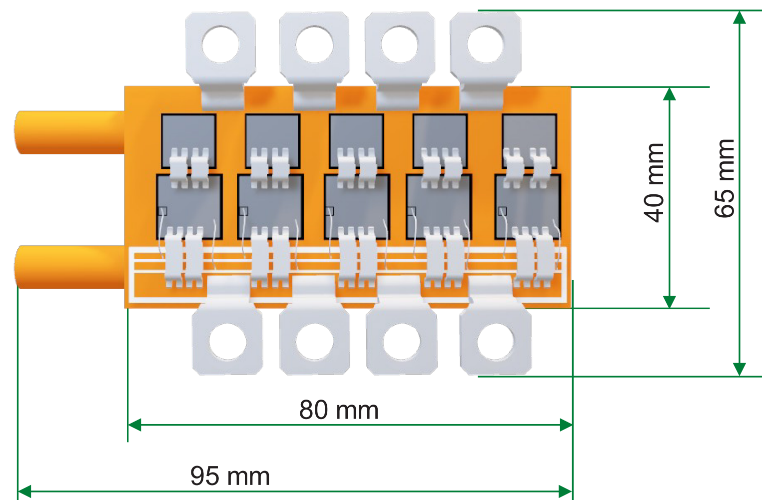

Figure 13.1200 A-device in non-isolated setup

Equipped with a 250 A-chipset, this version resembles a 1200 A single switch with an envelope of 123.5 cm³. A half-bridge consisting of two such devices consumes about 250 cm³ of space. In comparison, commonly used high-power modules today require up to 700 cm³ [3].

Beyond single switch arrangements, this setup is also well-suited for building bidirectional switches, such as those used in DC-circuit breakers in battery-charging or UPS systems, as well as AC-circuit breakers.

An additional benefit of the integrated liquid cooling is that the necessary surrounding housing is no longer burdened with the high temperatures commonly seen in power semiconductors. This opens the possibility of using lower-grade plastics, potentially even recyclable materials, which will become increasingly important in the years ahead. In contrast to the classical approach, the terminals also benefit from the intense cooling, reducing heat transfer to surrounding components such as DC-link capacitors.

In terms of resource usage, a half-bridge built from the device in Figure 13 has a mass below 0.7 kg which is less than half the weight of current designs. Sacrificing a fraction of the performance by replacing the copper heat sink using aluminum would allow for both cost and weight reduction.

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5. Summary

The omnipresent trend of increasing power density in power semiconductors, as they are built today, starts reaching physical limits due to the isolation requirement. To push these limits further, new methods to extract heat from power semiconductors more efficiently need to be identified.

One such method is direct liquid cooling, combined with suitable chip– and interconnection technologies, as presented. The shift from classical isolated assemblies to non-isolated counterparts opens the door to increasing power density by a factor of 10, compared to current solutions.

6. References

[1] Karsten Guth et. al., New assembly and interconnects beyond sintering methods PCIM 2010, Nuremberg, Germany.

[2] International Standard IEC 60749-34

[3] Elaheh Arjmand, Development of Cu-Cu Joining Technology by Laser Welding for Terminal Attach with-in Power Semiconductor Package, PCIM 2023, Nuremberg, Germany

[4] Datasheet, XA2400GV45WT, Littelfuse

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