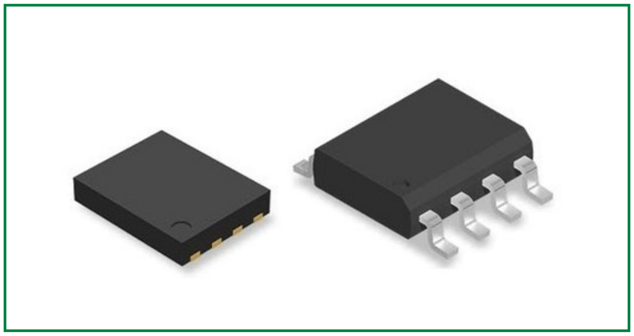
IXD704

4 A Dual Low-Side MOSFET Driver



Features

- Dual 4 A_{PK} sink/source output current (or 8 A_{PK} if paralleled)
- +14 V to +35 V supply voltage range
- TTL/CMOS compatible logic inputs
- UVLO, independent Enable inputs
- Latch-up protected to 4 A_{PK}

Applications

- Efficient power MOSFET and IGBT switching
- Switch mode power supply
- Motor control
- DC to DC converter
- Class-D switching amplifier
- Pulse transformer driver

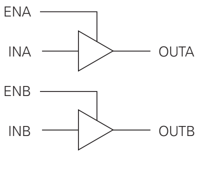
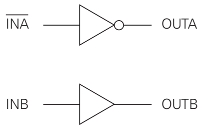
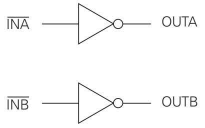
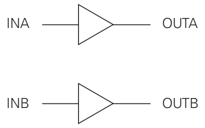
Description

The IXD704 family of dual high-speed gate drivers are especially well suited for driving the latest MOSFETs and IGBTs. Each of the two outputs can source and sink 4 A of current while producing voltage rise and fall times of less than 16 ns. The output of each driver is virtually immune to latch up, while proprietary circuitry eliminates cross conduction and current "shoot-through." Low propagation delays and fast, matched rise and fall times make the IXD704 family ideal for high frequency and high-power applications.

The IXD704 is available as a dual non-inverting driver, a dual non-inverting driver with independent enables, a dual inverting driver, and a dual driver with one inverting and one non-inverting output.

The IXD704 family is available in 8-pin narrow SOIC (N), 8-pin narrow SOIC and thermally enhanced 8-pin narrow SOIC with an exposed bottom-side pad (NE), and 8-pin DFN (M) packages.

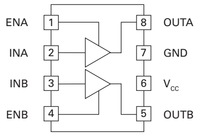
Ordering Information

	Part Number	UVLO (nominal)	Package	Packaging	Quantity
	IXD704DMTR	12V	DFN-8_EP	Tape and Reel	5000
	IXD704DAMTR	9V			
	IXD704DNETR	12V	SOIC(N)-8_EP		2000
	IXD704DANETR	9V			
	IXD704DNTR	12V	SOIC(N)-8		
	IXD704DANTR	9V			
	IXD704FNETR	12V	SOIC(N)-8_EP		
	IXD704FANETR	9V			
	IXD704FNTR	12V	SOIC(N)-8		
	IXD704FANTR	9V			
	IXD704INETR	12V	SOIC(N)-8_EP		
	IXD704IANETR	9V			
	IXD704INTR	12V	SOIC(N)-8		
	IXD704IANTR	9V			
	IXD704NNETR	12V	SOIC(N)-8_EP		
	IXD704NANETR	9V			
	IXD704NNTR	12V	SOIC(N)-8		
	IXD704NANTR	9V			

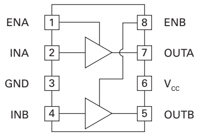
1 Specifications

1.1 Package Pinout

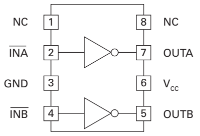
IXD704DM



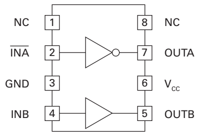
IXD704DN/DNE



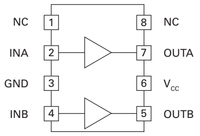
IXD704I



IXD704F



IXD704N



1.2 Pin Description

Name	Pin Type	Description
INA $\overline{\text{INA}}$	Logic Input	Channel A non-inverting Channel A inverting
INB $\overline{\text{INB}}$	Logic Input	Channel B non-inverting Channel B inverting
ENA	Logic Input	Channel A Enable: Drive pin low to force Channel A output off (Low).
ENB	Logic Input	Channel B Enable: Drive pin low to force Channel B output off (Low).
OUTA	Output	Channel A: Sources and sinks current to turn a discrete MOSFET or IGBT on and off
OUTB	Output	Channel B: Sources and sinks current to turn a discrete MOSFET or IGBT on and off
V_{CC}	Power	Supply Voltage
GND	Power	Ground
PAD	Thermal	Not shown. The exposed bottom side pad is for thermal management of the M and NE packages and should be connected to GND. The pad is not suitable for carrying current.

1.3 Absolute Maximum Ratings

Parameter	Symbol	Value		Units
		Minimum	Maximum	
Supply voltage	V_{CC}	–0.3	40	V
Output voltage (OUTA, OUTB)	V_{OUT}	–0.3	V_{CC}+0.3	
Output pulsed current (0.5 µs)	I_{OUT}	—	±5	A
Output reverse bias latch-up protection (0.5 µs)	I_{REV}	—	±4	A
Input voltage (INA, $\overline{\text{INA}}$, INB, $\overline{\text{INB}}$, ENA, ENB)	V_{IN}, V_{EN}	–5	V_{CC}+0.3	V
Junction temperature	T_J	–40	+150	°C
Storage temperature	T_{STG}	–65	+150	
Package power dissipation, DFN-8_EP	P_D	—	3.57	W
Package power dissipation, SOIC(N)-8	P_D	—	1.04	W
Package power dissipation, SOIC(N)-8_EP	P_D	—	1.47	W
ESD capability (HBM)	V_{ESD}	—	±3	kV

Absolute maximum electrical ratings are at 25 °C and voltages are referenced to the GND terminal.

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 Recommended Operating Conditions

Parameter	Symbol	Value		Units
		Minimum	Maximum	
Supply voltage	V_{CC}	14	35	V
Output voltage	V_{OUT}	GND	V_{CC}	
Input voltage	V_{IN}	GND	V_{CC}	
Input switching frequency	f	0	1	MHz
Operating ambient temperature	T_A	–40	+125	°C

1.5 Electrical Characteristics

Unless other noted, electrical characteristics are specified at: $V_{CC} = 15\,V$, $V_{INH} = 5V$, $V_{INL} = 0\,V$, $-40\,°C \le T_A \le +125\,°C$, and all voltages are referenced to the GND terminal.

Typical values are characteristic of the device at $T_A = 25\,°C$ and are the result of engineering evaluations. They are provided for informational purposes only and are not part of the manufacturing testing requirements.

1.5.1 Supply

(V_{CC})

Parameter	Conditions	Symbol	Value			Units
			Minimum	Typical	Maximum	
Supply current	$V_{OUT} = 0\,V$	I_{CCQ}	—	1.6	2	mA
	$V_{OUT} = V_{CC}$	I_{CCQ_H}	—	1.6	2	
UVLO Off threshold						V
IXD704	V_{CC} rising	V_{CCUV_r}	—	12.5	14	
IXD704xA			—	9.5	10.5	
UVLO On threshold						
IXD704	V_{CC} falling	V_{CCUV_f}	10.5	11	—	
IXD704xA			8	8.5	—	
UVLO hysteresis						
IXD704	—	V_{CCUV_hys}	1	1.5	—	
IXD704xA			0.75	1	—	

1.5.2 Logic Inputs

(INA, $\overline{\text{INA}}$, INB, $\overline{\text{INB}}$, ENA, ENB)

Parameter	Conditions	Symbol	Value			Units
			Minimum	Typical	Maximum	
Logic low voltage	—	V_{IL}	—	—	0.8	V
Logic high voltage	—	V_{IH}	2.4	—	—	
Input hysteresis	—	V_{IN_hys}	—	0.5	—	
Input pull down current (INx)	$V_{IN} = +0.8\,V$	I_{IL}	10	—	—	µA
	$V_{IN} = +5\,V$	$I_{IN(+5)}$	—	90	120	
	$V_{IN} = +15\,V$, $V_{IN} = +35\,V$	$I_{IN(+15)}$, $I_{IN(+35)}$	—	90	120	
Input pull up current ($\overline{\text{INx}}$)	$V_{\overline{IN}} = 0\,V$	$I_{IN(0)}$	—	65	100	
	$V_{\overline{IN}} = +2.4\,V$	I_{IH}	10	—	—	
Enable pull up current	$V_{EN} = 0\,V$	$I_{EN(0)}$	—	65	100	
	$V_{EN} = +2.4\,V$	I_{IH_EN}	10	—	—	
Input negative bias current	$V_{IN} = -5$	$I_{IN(-5)}$	—	−1.4	−2	mA
Input open circuit voltage	INx = ENx = Open	V_{IN_OC}	—	3.3	—	V

1.5.3 Gate Drive Outputs

(OUTA, OUTB)

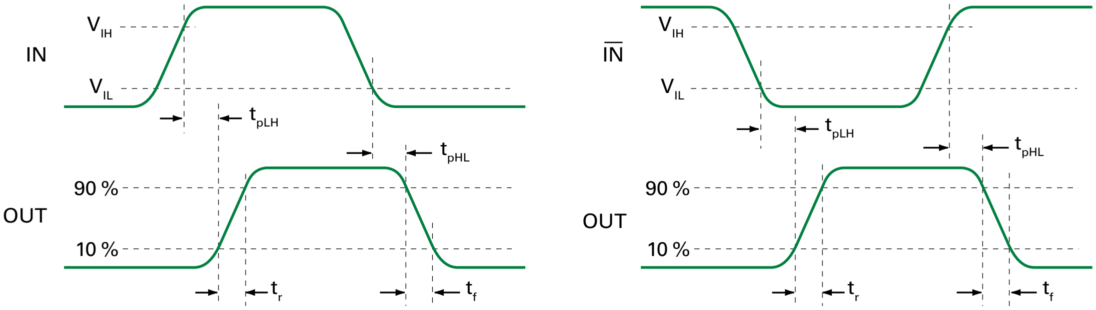
Parameter	Conditions	Symbol	Value			Units
			Minimum	Typical	Maximum	
Peak output current	$C_L = 0.47\,\mu F$, $f = 1\,kHz$	I_{OUT}	—	±4	—	A
Miller Plateau current	$V_{OUT} = 5\,V$	I_{OUT}	—	±4	—	
High level output voltage	$I_{OUT} = -100\,mA$	V_{OH}	—	$V_{CC} - 0.1$	—	V
Low level output voltage	$I_{OUT} = 100\,mA$	V_{OL}	—	0.06	—	
Output high on-resistance	$I_{OUT} = -100\,mA$	R_{OH}	—	1.3	2.5	Ω
Output low on-resistance	$I_{OUT} = 100\,mA$	R_{OL}	—	1.1	2	

1.6 Switching Characteristics

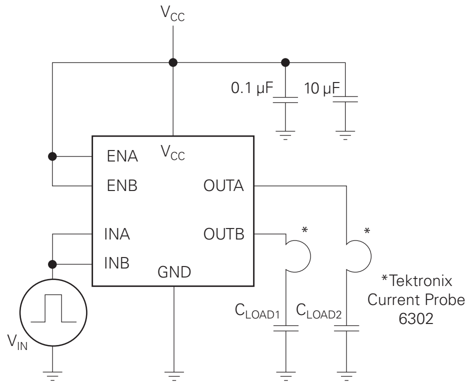
Unless other noted, timing characteristics are specified at: $V_{CC} = 15V$, $V_{INH} = 3V$, $V_{INL} = 0V$, $f_{IN} = 100\,kHz$, $D = 50\,\%$, $C_L = 1\,nF$, $-40\,°C \le T_A \le +125\,°C$, and all voltages are referenced to the GND terminal.

Parameter	Conditions	Symbol	Value			Units
			Minimum	Typical	Maximum	
Enable propagation delay	—	t_{pLH_EN}	—	35	65	ns
Disable propagation delay		t_{pHL_EN}				
Turn-on propagation delay						
Non-inverting driver	—	t_{pLH}	—	35	65	
Inverting driver				28		
Turn-off propagation delay						
Non-inverting driver	—	t_{pHL}	—	35	65	
Inverting driver				28		
Turn-on rise time	—	t_r	—	9	16	
Turn-off fall time	—	t_f	—	8	14	
Propagation delay matching (IN, EN) (IXD704D, IXD704I, IXD704N only)	$\lvert t_{pLH\_A} - t_{pLH\_B} \rvert$ $\lvert t_{pHL\_A} - t_{pHL\_B} \rvert$	t_{pM}	—	2	4	
Minimum input pulse width	—	t_{PW}	50	—	—	

1.6.1 Timing Diagrams



1.6.2 Characteristics Test Diagram

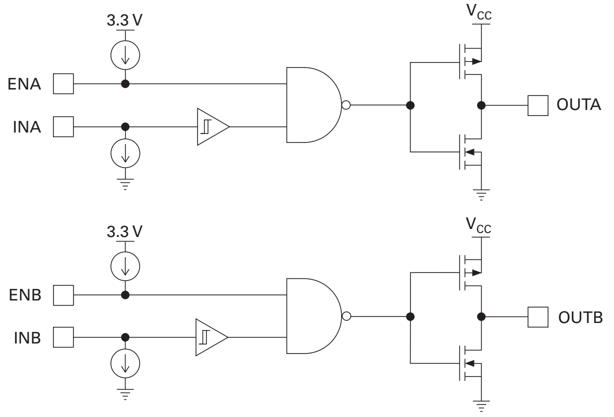


1.7 Thermal Characteristics

Parameter	Package	Symbol	Rating	Units
Thermal resistance, Junction to Ambient	M DFN-8_EP	θ_{JA}	35	K/W
	NE SOIC(N)-8_EP		85	
	N SOIC(N)-8		120	
Thermal resistance, Junction to Case	M DFN-8_EP	θ_{JC}	4.96	
	NE SOIC(N)-8_EP		10	

2 Block Diagrams and Logic Tables

2.1 IXD704D: Dual Non-Inverting with Enables

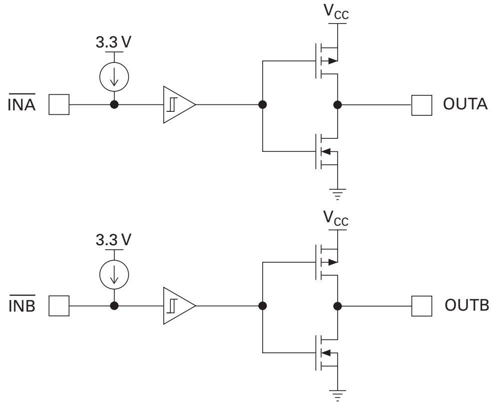


Logic Table

IN#	EN#	UVLO[2]	OUT#
0[1]	1[1]	0	0
1			1
X	0		0
X	X	1	0

Notes:
 # = A or B. Drivers are independent, inputs of one driver do not affect the output of the other driver.
[1] *Or floating (open)*
[2] *UVLO = 0: Device active*
UVLO = 1: Device disabled

2.2 IXD704I: Dual Inverting

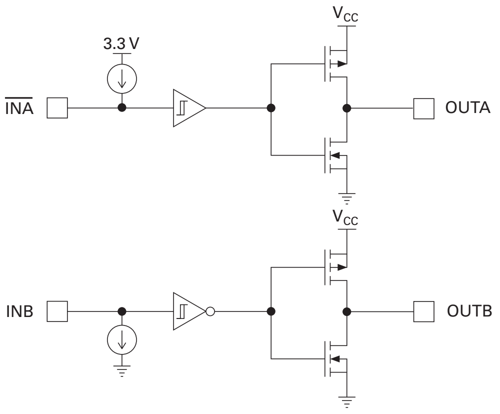


Logic Table

$\overline{\text{IN}}$#	UVLO[2]	OUT#
0	0	1
1[1]		0
X	1	0

Notes:
 # = A or B. Drivers are independent, inputs of one driver do not affect the output of the other driver.
[1] *Or floating (open)*
[2] *UVLO = 0: Device active*
UVLO = 1: Device disabled

2.3 IXD704F: A Inverting, B Non-Inverting



Channel A Logic Table

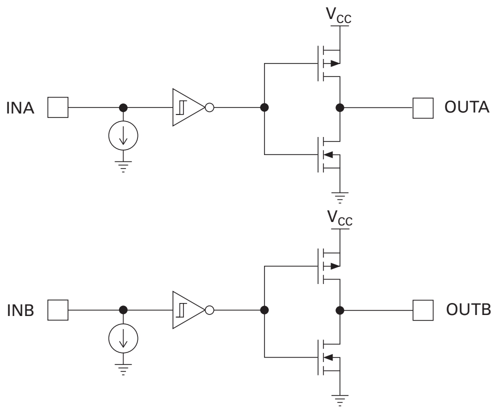
$\overline{\text{INA}}$	UVLO[2]	OUTA
0	0	1
1[1]		0
X	1	0

Channel B Logic Table

INB	UVLO[2]	OUTB
0[1]	0	0
1		1
X	1	0

Notes:
[1] Or floating (open)
[2] UVLO = 0: Device active
UVLO = 1: Device disabled

2.4 IXD704N: Dual Non-Inverting



Logic Table

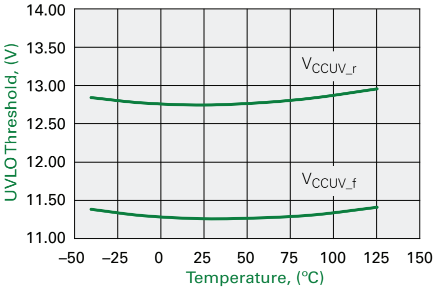
IN#	UVLO[2]	OUT#
0[1]	0	0
1		1
X	1	0

Notes:
 # = A or B. Drivers are independent, inputs of one driver do not affect the output of the other driver.
[1] Or floating (open)
[2] UVLO = 0: Device active
UVLO = 1: Device disabled

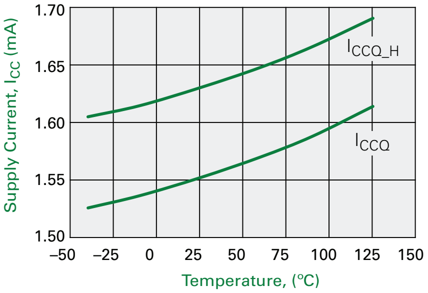
3 Performance Data

Unless otherwise noted V_{CC} = 15 V, T_A=25 °C, and values are typical.

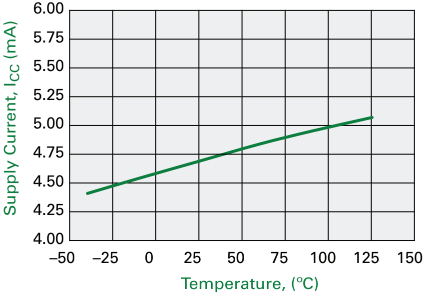
V_{CC} Under Voltage Lockout vs. Temperature



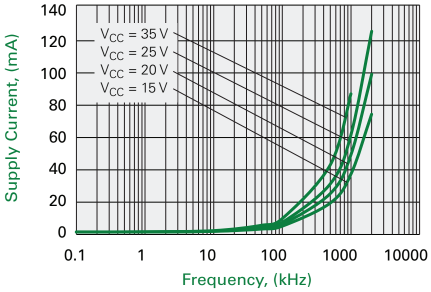
Supply Current vs. Temperature
Outputs in DC ON/OFF Conditions
(ENA = ENB = V_{CC} = 15 V)



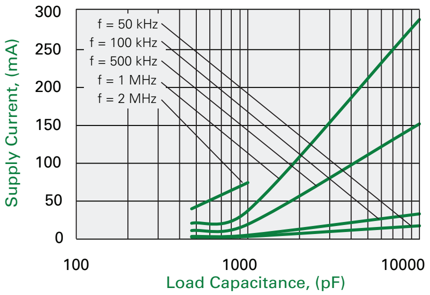
Operating Supply Current vs. Temperature
(Outputs Switching)
(V_{CC} = 15 V, f = 100 kHz, C_L = 1 nF)



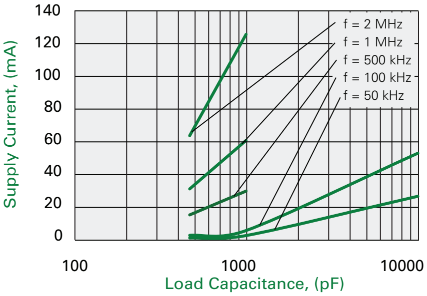
Operating Supply Current vs. Frequency
(C_L = 1 nF, Both Channels Switching)



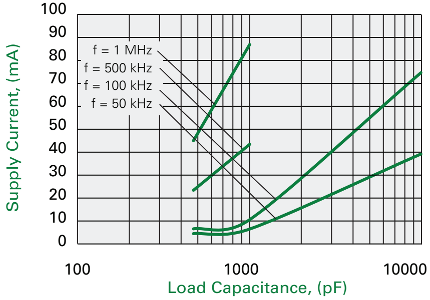
Supply Current vs. Load Capacitance
Both Outputs Active (V_{CC} = 15 V)



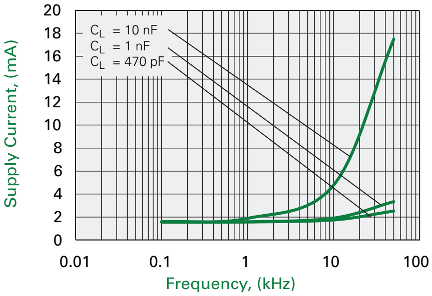
Supply Current vs. Load Capacitance
Both Outputs Active (V_{CC} = 25 V)



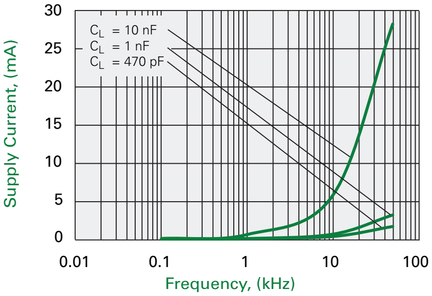
Supply Current vs. Load Capacitance
Both Outputs Active (V_{CC} = 35 V)



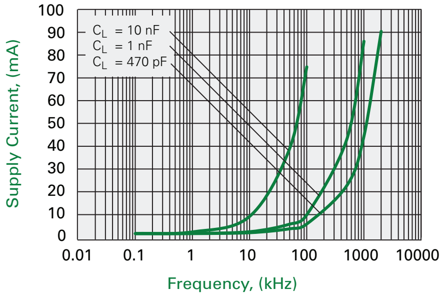
Supply Current vs. Frequancy
Both Outputs Active (V_{CC} = 15 V)



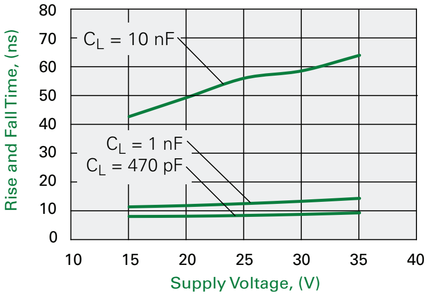
Supply Current vs. Frequancy
Both Outputs Active (V_{CC} = 25 V)



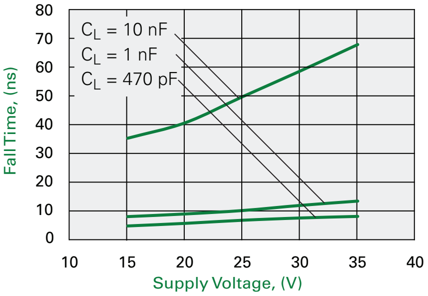
Supply Current vs. Frequancy
Both Outputs Active (V_{CC} = 35 V)



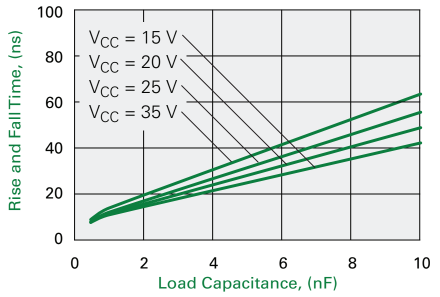
Rise Times vs. Supply Voltage Channel A&B
(Input = 0 – 5 V, f = 100 kHz, T = 25 °C)



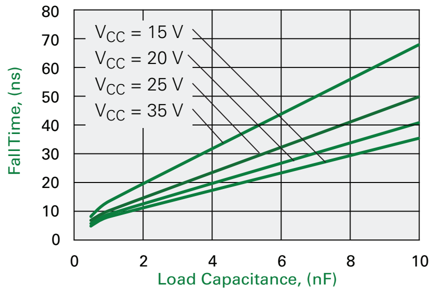
Fall Times vs. Supply Voltage, Channel A&B
(Input = 0 – 3 V, f = 100 kHz, T_A = 25 °C)



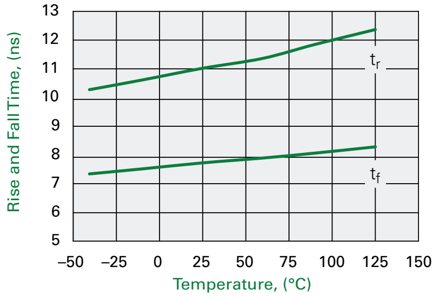
Rise Time vs. Load Capacitance at Various V_{CC} levels Channel A&B
(Input = 0 – 5 V, f = 100 kHz, T_A = 25 °C)



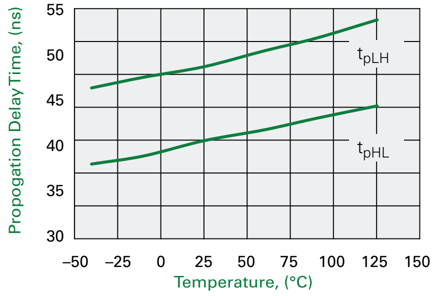
Fall Time vs. Load Capacitance at Various V_{CC} levels, Channel A&B
(Input = 0 - 5 V, f = 100 kHz, T_A = 25 °C)



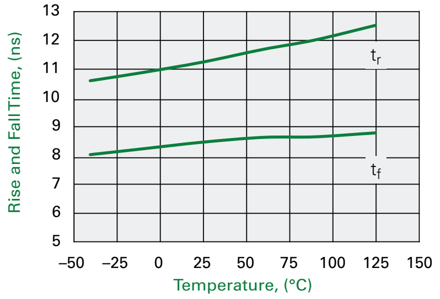
Rise and Fall Times vs. Temperature Channel A
(Input = 0 – 3 V, f = 100 kHz, V_{CC} = 15 V, C_L = 1 nF)



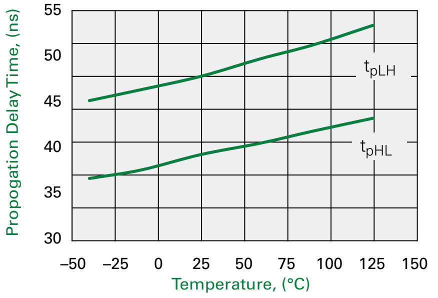
Propagation Delay vs. Temperature Channel A
(Input = 0 – 3 V, f = 100 kHz, V_{CC} = 15 V, C_L = 1 nF)



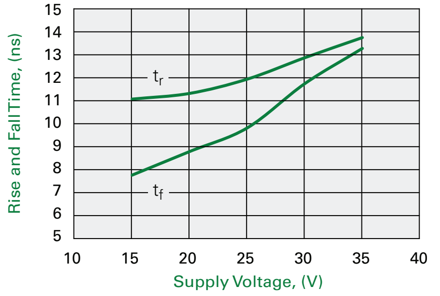
Rise and Fall Times vs. Temperature Channel B
(Input = 0 – 3 V, f = 100 kHz, V_{CC} = 15 V, C_L = 1 nF)



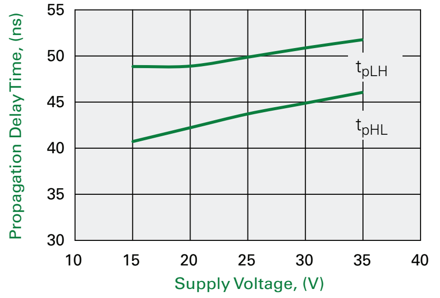
Propagation Delay vs. Temperature Channel B
(Input = 0 – 3 V, f = 100 kHz, V_{CC} = 15 V, C_L = 1 nF)



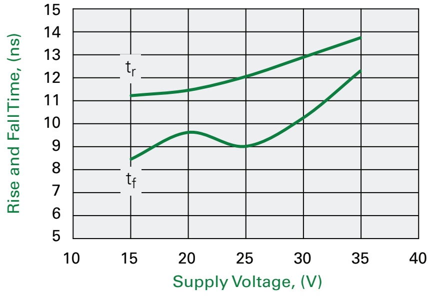
Rise / Fall Time vs. Supply Voltage Channel A
(Input = 0 – 3 V, f = 100 kHz, C_L = 1 nF)



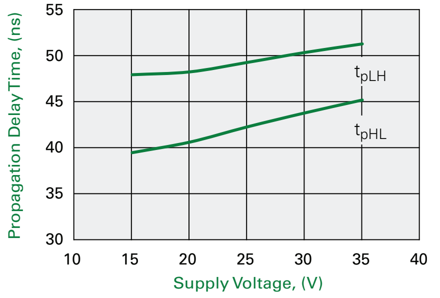
Propagation Delay vs. Supply Voltage Channel A
(Input = 0 – 3 V, f = 100 kHz, C_L = 1 nF)



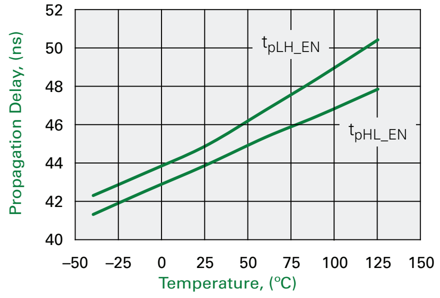
Rise / Fall Time vs. Supply Voltage Channel B
(Input = 0 – 3 V, f = 100 kHz, C_L = 1 nF)



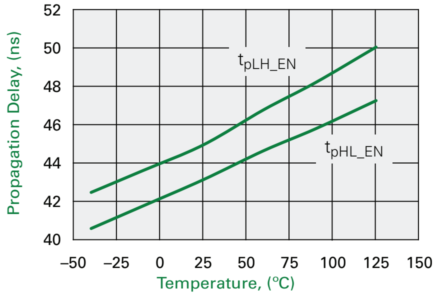
Propagation Delay vs. Supply Voltage Channel B
(Input = 0 – 3 V, f = 100 kHz, C_L = 1 nF)



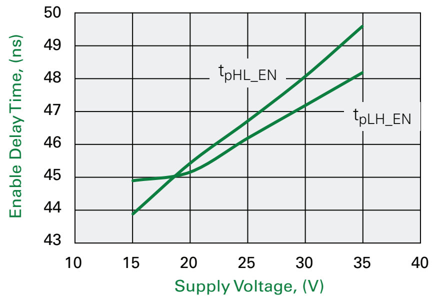
Enable to Output Propagation Delay vs. Temperature Channel A
(Input = 0 – 3 V, f = 100 kHz, V_{CC} = 15 V, C_L = 1 nF)



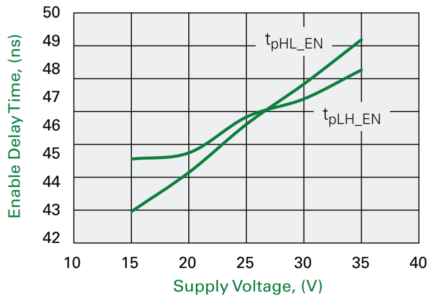
Enable to Output Propagation Delay vs. Temperature Channel B
(Input = 0 – 3 V, f = 100 kHz, V_{CC} = 15 V, C_L = 1 nF)



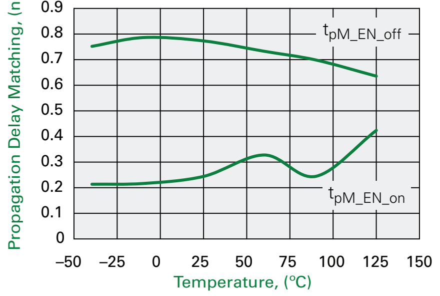
Propagation Delay (Enable) vs. Supply Voltage Channel A (Input = 0 – 3 V, f = 100 kHz, C_L = 1 nF)



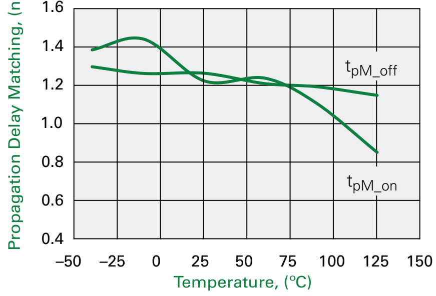
Propagation Delay (Enable) vs. Supply Voltage Channel B (Input = 0 – 3 V, f = 100 kHz, C_L = 1 nF)



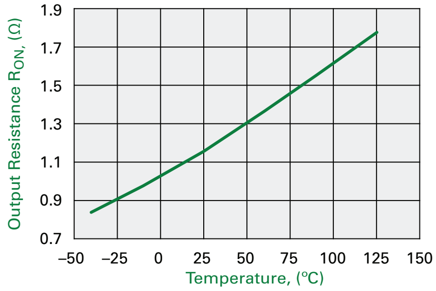
Propagation Delay Matching (Enable) vs. Temperature (Input = 0 – 3 V, f = 100 kHz, V_{CC} = 15 V, C_L = 1 nF)



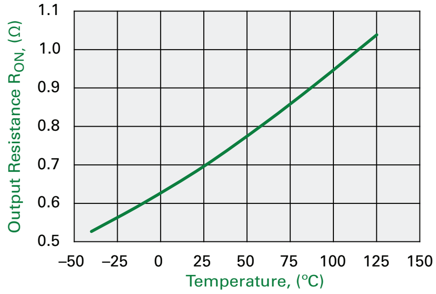
Propagation Delay Matching vs. Temperature (Input = 0 – 3 V, f = 100 kHz, V_{CC} = 15 V, C_L = 1 nF)



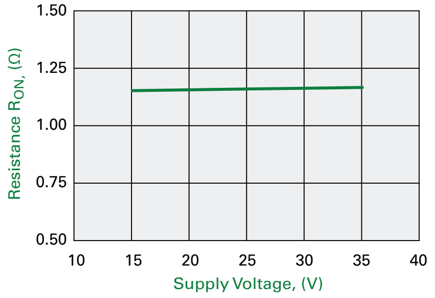
Output Pull-Up Resistance vs. Temperature (V_{CC} = 15 V, I_{OUT} = –100 mA)



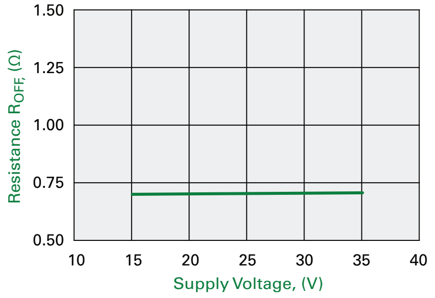
Output Pull-Down Resistance vs. Temperature (V_{CC} = 15 V, I_{OUT} = 100 mA)



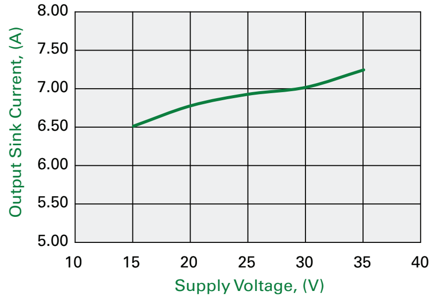
High State Output Resistance vs. Supply Voltage (I_{OUT} = –100 mA)



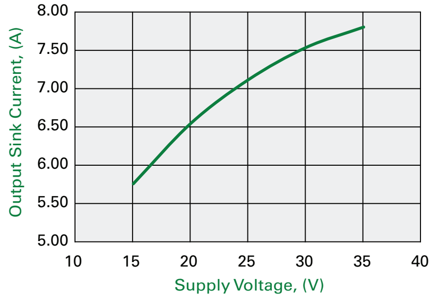
Low State Output Resistance vs. Supply Voltage (I_{OUT} = 100 mA)



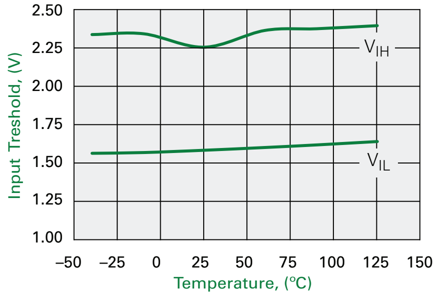
Outpuit Sink Current vs. Supply Voltage (V_{IN} = 0 - 5 V, C_L = 0.47 uF, f = 1 kHz)



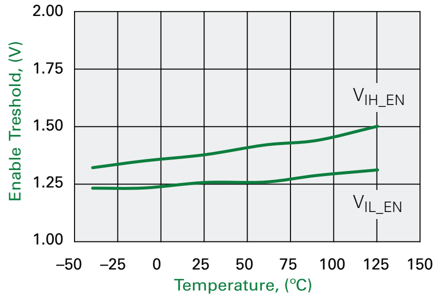
Output Source Current vs. Supply Voltage (V_{IN} = 0 - 5 V, C_L = 0.47 uF, f = 1 kHz)



Input Threshold vs. Temperature (V_{CC} = 15 V)



Enable Threshold vs. Temeprature (V_{CC} = 15 V)



4 Manufacturing Information

4.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. Littelfuse classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a Moisture Sensitivity Level (MSL) classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
IXD704, all versions	MSL 1

4.2 ESD Sensitivity

This product is ESD Sensitive, and should be handled according to the industry standard **JESD-625**.

4.3 Soldering Profile

Provided in the table below is the **IPC/JEDEC J-STD-020** Classification Temperature (T_C) and the maximum total dwell time (T_C – 5 °C). The device's body temperature must not exceed the Classification Temperature at any time during reflow soldering processes.

Device	Classification Temperature (T_C)	Dwell Time (t_P)	Max Reflow Cycles
IXD704, all versions	260°C	30 seconds	3

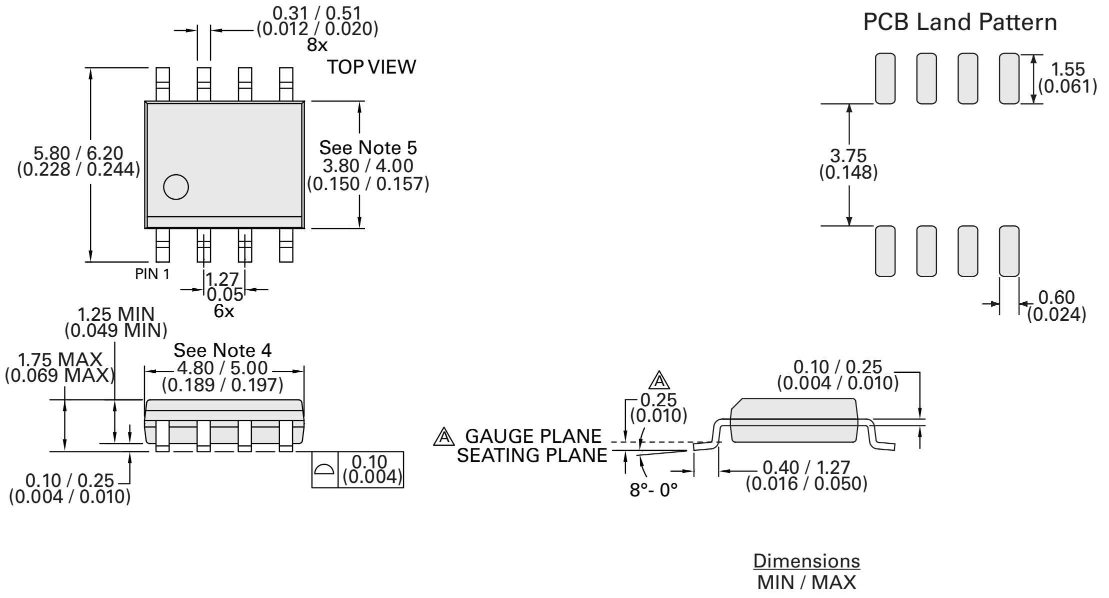
4.4 Board Wash

Littelfuse recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: Using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to halide flux or solvents.

Pb RoHS e3

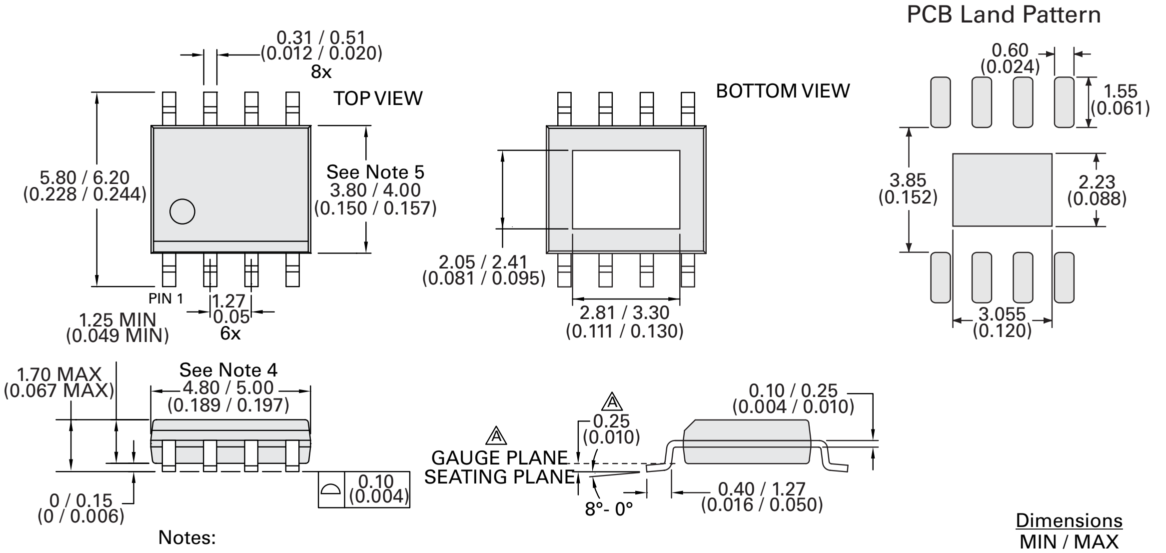
4.5 Mechanical Dimensions

4.5.1 N Package: SOIC(N)-8



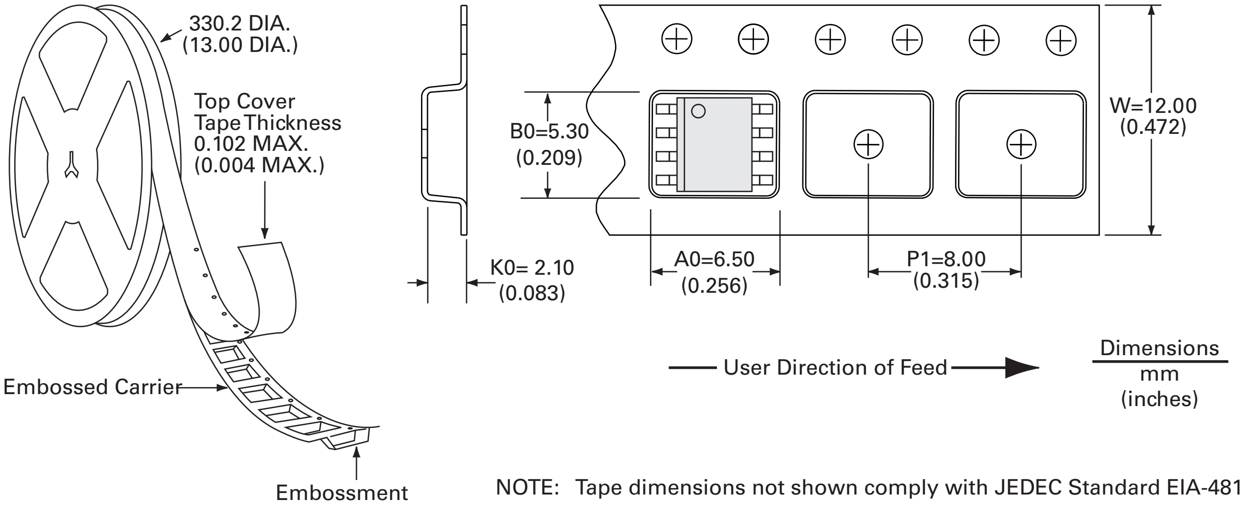
Notes:
1. Controlling dimension: millimeters.
2. All dimensions are in mm (inches).
3. This package conforms to JEDEC Standard MS-012, variation AA, Rev. F.
4. Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per end.
5. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 mm per side.
6. Lead thickness includes plating.

4.5.2 NE Package: SOIC(N)-8_EP



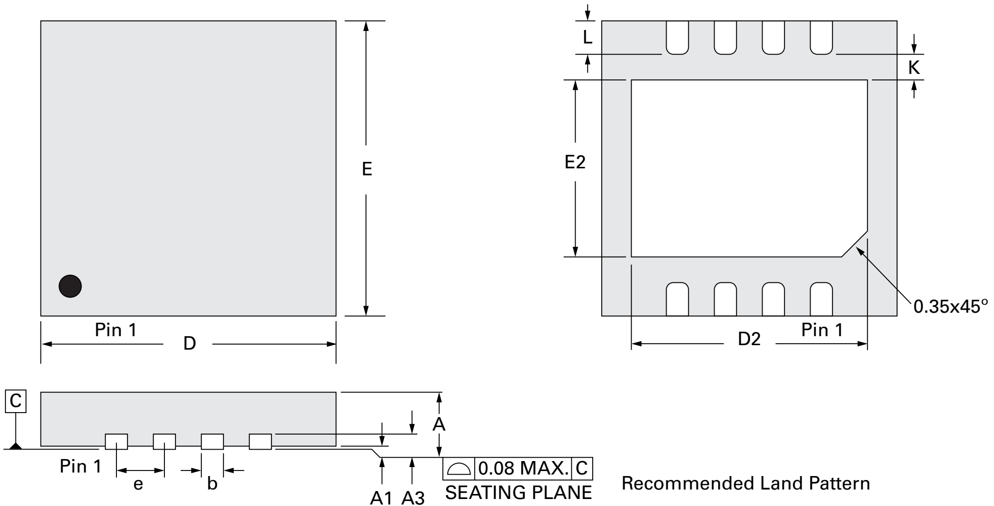
Notes:
1. Controlling dimension: millimeters.
2. All dimensions are in mm (inches).
3. This package conforms to JEDEC Standard MS-012, variation BA, Rev. F.
4. Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per end.
5. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 mm per side.
6. The exposed metal pad on the back of the package should be connected to GND. It is not suitable for carrying current.
7. Lead thickness includes plating.

4.5.3 Tape and Reel Information for N and NE Packages



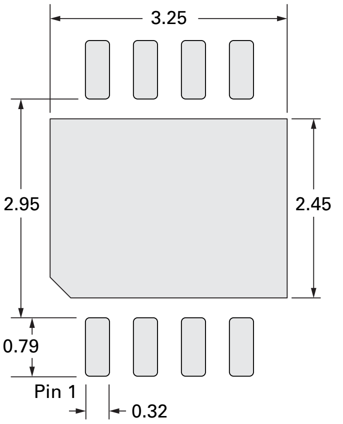
NOTE: Tape dimensions not shown comply with JEDEC Standard EIA-481-2

4.5.4 M Package (DFN-8_EP)



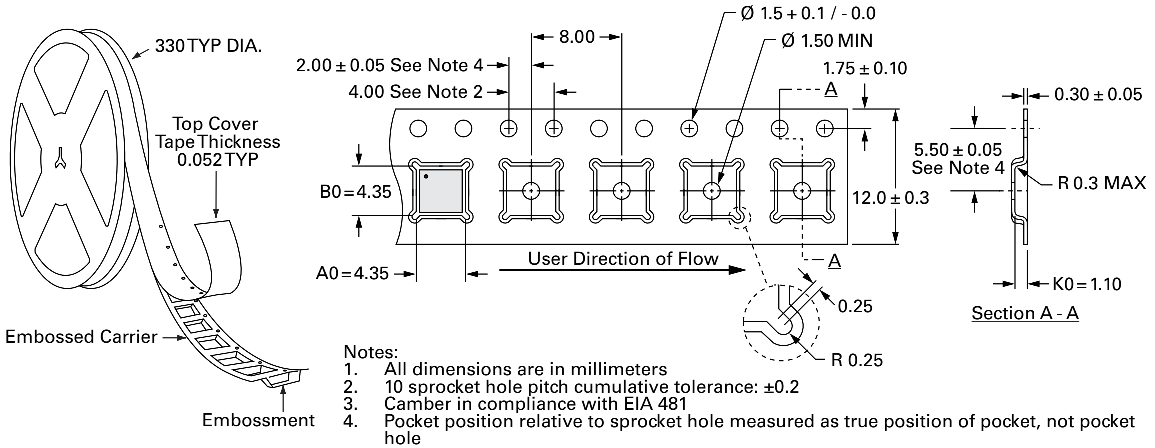
SYMBOL	VALUE MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.25	0.30	0.35
D	3.90	4.00	4.10
D2	3.15	3.20	3.25
E	3.90	4.00	4.10
E2	2.35	2.40	2.45
e	0.65 BSC		
L	0.40	0.45	0.50
K	0.20	-	-

Recommended Land Pattern



Notes:
1. All dimensions are in millimeters.
2. Dimension"b" applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip.
3. Coplanarity applies to the exposed heat sink pad as well as the terminals.

4.5.5 Tape and Reel Information for M Package



Notes:
1. All dimensions are in millimeters
2. 10 sprocket hole pitch cumulative tolerance: ±0.2
3. Camber in compliance with EIA 481
4. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole
5. Tolerances, unless otherwise noted:
   1 Place: ± 0.2
   2 Places: ± 0.10