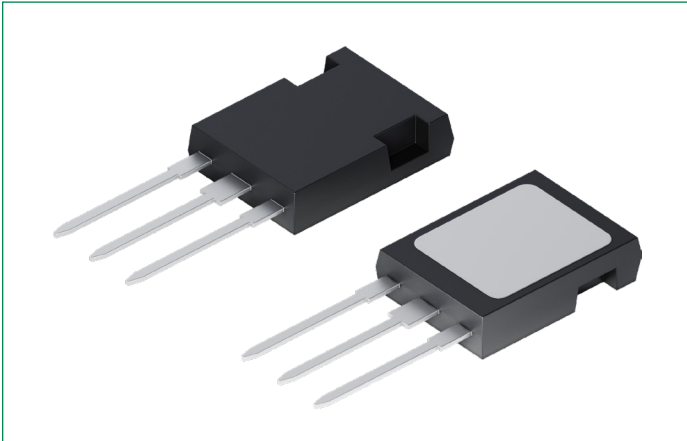


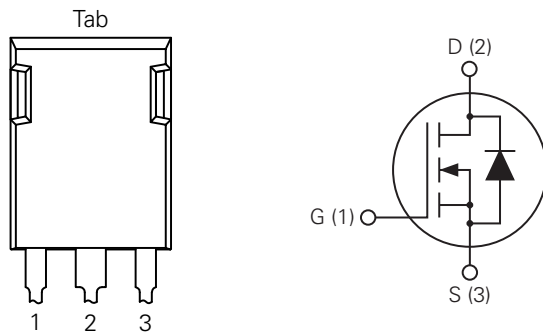
IXTR400N20X4

200 V, 3.90 mΩ, 210 A X4-Class Power MOSFET

N-Channel Enhancement Mode, Avalanche Rated



Pinout Diagram ISOPLUS-247-3L (IXTR)



1: Gate; **2:** Drain; **3:** Source, **Tab:** Isolated

Features

- Low on-state resistance
- High nominal current rating
- Low gate charge
- Low thermal resistance

Benefits

- Low conduction losses, improved efficiency
- Minimized parallel connection effort with decreased part count
- Simplified driver design
- Simplified thermal design

ISOPLUS247 Package

- Direct Bonded Copper (DBC) based isolated PLUS247 package improves thermal resistance and power handling capability
- Isolation voltage 2500 V AC (RMS), 1 minute
- Isolated discrete package with electrically isolated tab simplifies assembly
- Pin compatibility with standard TO-247 package

Applications

- DC load switch
- Battery protection
- Battery OR-ing
- Battery energy storage systems
- DC/DC buck-boost converters

Product Summary

Characteristic	Value	Unit
V_{DSS}	200	V
I_D @ 25°C (chip limit)	210	A
I_D @ 25°C (package terminal limit)	160	A
$R_{DS(on)}$	≤ 3.9	mΩ

Maximum Ratings ($T_{vj} = 25\text{ °C}$ unless otherwise specified)

Symbol	Characteristic	Conditions	Value	Unit
V_{DSS}	Drain-source voltage	$T_{vj} = 25\text{ °C}$ to 175 °C	200	V
V_{GSS}	Gate-source voltage	Continuous	± 20	V
V_{GSM}		Transient	± 30	V
I_{D25}	Drain current ¹	$T_c = 25\text{ °C}$	210	A
I_{tRMS}	Terminal RMS current	–	160	A
I_{DM}	Peak drain current	$T_c = 25\text{ °C}$, pulse width limited by $T_{vj(max)}$	900	A
I_{AS}	Single pulse avalanche current	$T_c = 25\text{ °C}$	200	A
E_{AS}	Single pulse avalanche energy	$T_c = 25\text{ °C}$	4	J
dv/dt	Reverse diode dv/dt	$I_S \leq I_{DM}$, $V_{DD} \leq V_{DSS}$, $T_{vj} \leq 150\text{ °C}$	50	V/ns
P_{tot}	Power dissipation	$T_c = 25\text{ °C}$	417	W
T_{vj}	Virtual junction temperature range	–	–55 to +175	°C
$T_{vj(max)}$	Maximum virtual junction temperature range	–	175	°C
T_{stg}	Storage temperature range	–	–55 to +175	°C
T_{sold}	Soldering temperature	1.6 mm (0.062 in.) from case for 10 s	300	°C
V_{isol}	Isolation withstand voltage	50/60 Hz, t = 1 min	2500	V~
F_C	Mounting force	–	20..120/4.5..27	N/lb
W	Package weight	–	5	g

Note 1: Terminal current limit to be taken into account

Thermal Characteristics

Symbol	Characteristic	Value			Unit
		Min.	Typ.	Max.	
$R_{th(j-c)}$	Thermal resistance junction to case	–	–	0.36	K/W
$R_{th(c-s)}$	Thermal resistance case to heat sink (thermal grease commonly utilized)	–	0.05	–	K/W

Electrical Characteristics – Static ($T_{vj} = 25\text{ °C}$ unless otherwise specified)

Symbol	Characteristic	Conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	200	–	–	V
$V_{GS(th)}$	Gate threshold voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = V_{DS}$	2.5	–	4.5	V
I_{GSS}	Gate-source leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$	–	–	± 200	nA
I_{DSS}	Drain-source leakage current	$V_{DS} = V_{DSS}$, $V_{GS} = 0\text{ V}$	–	–	25	μA
		$V_{DS} = V_{DSS}$, $V_{GS} = 0\text{ V}$, $T_{vj} = 150\text{ °C}$	–	–	3	mA
$R_{DS(on)}$	Drain-source on-resistance ²	$V_{GS} = 10\text{ V}$, $I_D = 100\text{ A}$	–	–	3.90	m Ω

Note 2: Pulse test, $t \leq 300\text{ }\mu\text{s}$, duty cycle, $d \leq 2\%$

Electrical Characteristics – Dynamic $(T_{vj} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Symbol	Characteristic	Conditions	Value			Unit
			Min.	Typ.	Max.	
g_{fs}	Transconductance ²	$V_{DS} = 10\text{ V}, I_D = 60\text{ A}$	125	170	–	S
$R_{g(int)}$	Gate input resistance	–	–	1.26	–	Ω
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$	–	27.7	–	nF
C_{oss}	Output capacitance		–	3.1	–	nF
C_{rss}	Reverse transfer capacitance		–	15	–	pF
$C_{o(er)}$	Effective output capacitance – energy related	$V_{GS} = 0\text{ V}, V_{DS} = 0.8 \times V_{DSS}$	–	1.78	–	nF
$C_{o(tr)}$	Effective output capacitance – time related		–	7.47	–	nF
Q_G	Total gate charge	$V_{GS} = 10\text{ V}, V_{DS} = 0.5 \times V_{DSS},$ $I_D = 200\text{ A}$	–	348	–	nC
Q_{GS}	Gate-source charge		–	118	–	
Q_{GD}	Gate-drain charge		–	80	–	
$t_{d(on)}$	Turn-on delay time	Resistive Switching $V_{GS} = 10\text{ V}, V_{DS} = 0.5 \times V_{DSS},$ $I_D = 200\text{ A}, R_{G(ext)} = 10\text{ }\Omega$	–	150	–	ns
t_r	Rise time		–	480	–	
$t_{d(off)}$	Turn-off delay time		–	430	–	
t_f	Fall time		–	370	–	

Note 2: Pulse test, $t \leq 300\text{ }\mu\text{s}$, duty cycle, $d \leq 2\%$

Source-Drain Diode Characteristics $(T_{vj} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Symbol	Characteristic	Conditions	Value			Unit
			Min.	Typ.	Max.	
I_S	Continuous diode forward current	$V_{GS} = 0\text{ V}$	–	–	400	A
I_{SM}	Diode pulse current	Repetitive, pulse width limited by $T_{vj(max)}$	–	–	1600	A
V_{SD}	Diode forward voltage ²	$I_F = 100\text{ A}, V_{GS} = 0\text{ V}$	–	–	1.4	V
t_{rr}	Reverse recovery time	$I_F = 100\text{ A}, -di/dt = 300\text{ A}/\mu\text{s},$ $V_R = 100\text{ V}, V_{GS} = 0\text{ V}$	–	270	–	ns
Q_{rr}	Reverse recovery charge		–	1.75	–	μC
I_{rrm}	Peak reverse recovery current		–	35	–	A

Note 2: Pulse test, $t \leq 300\text{ }\mu\text{s}$, duty cycle, $d \leq 2\%$

Characteristic Curves

Fig. 1. Output Characteristics @ $T_{vj} = 25\text{ }^\circ\text{C}$

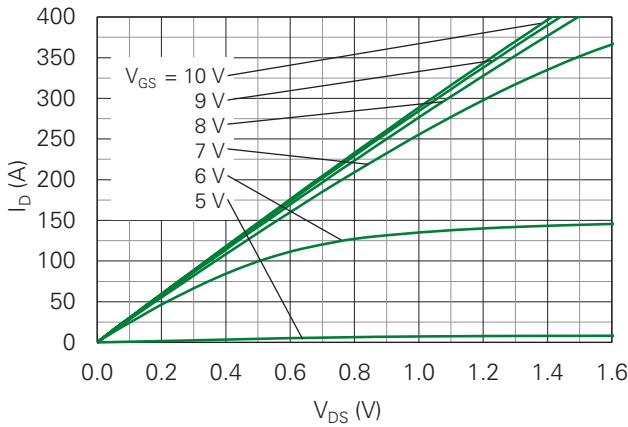


Fig. 2. Extended Output Characteristics @ $T_{vj} = 25\text{ }^\circ\text{C}$

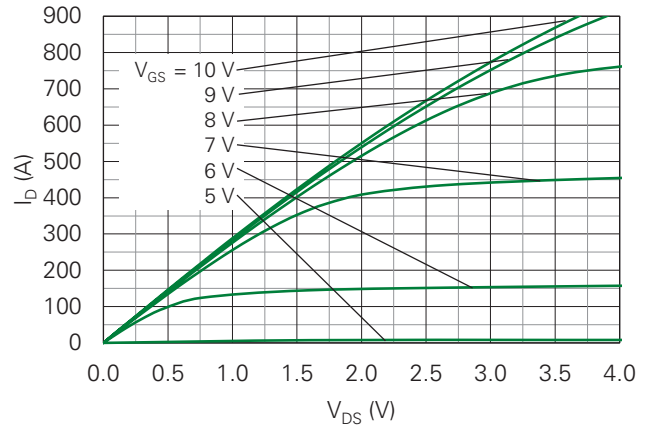


Fig. 3. Output Characteristics @ $T_{vj} = 150\text{ }^\circ\text{C}$

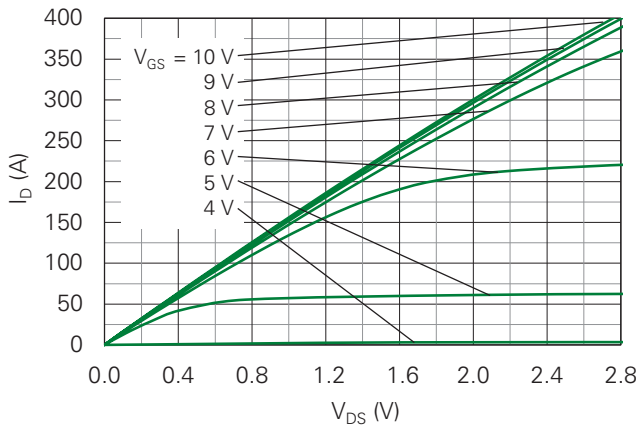


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 200\text{ A}$ Value vs. Junction Temperature

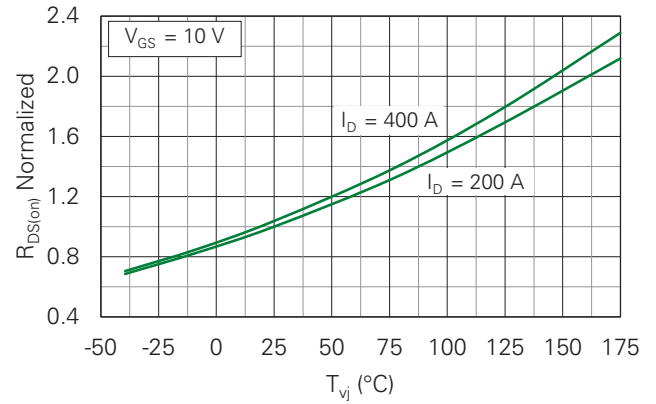


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 200\text{ A}$ vs. Drain Current

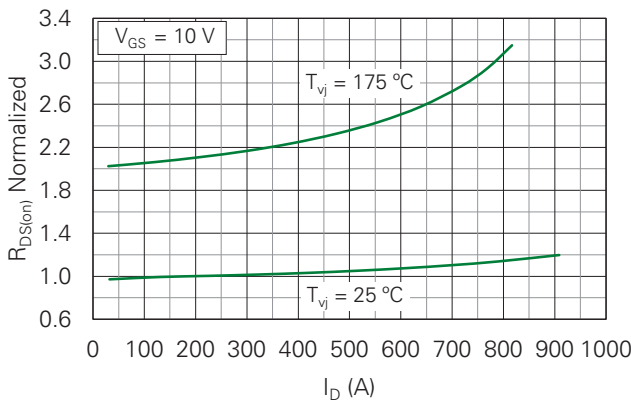


Fig. 6. Normalized Breakdown & Threshold Voltages vs. Junction Temperature

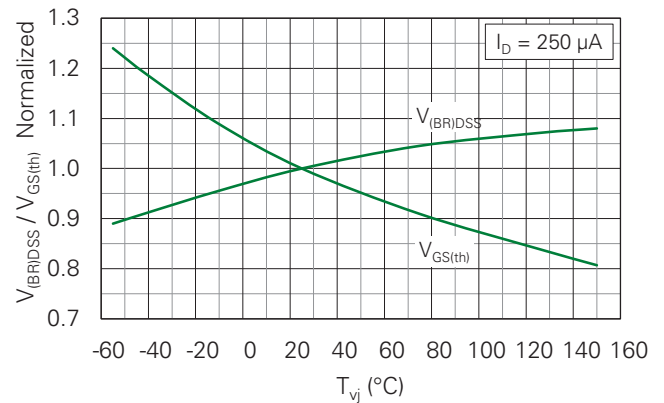


Fig. 7. Drain Current vs. Case Temperature

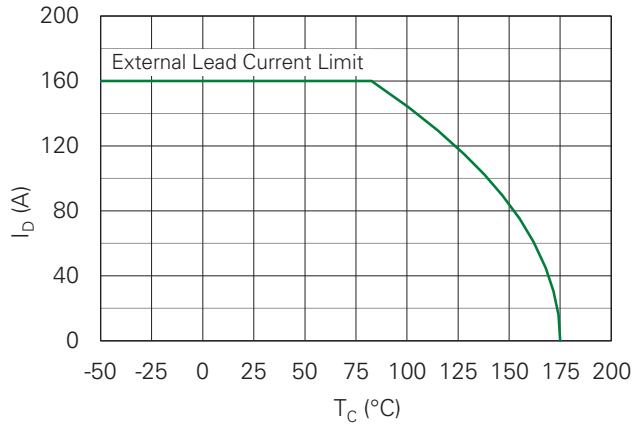


Fig. 8. Input Admittance

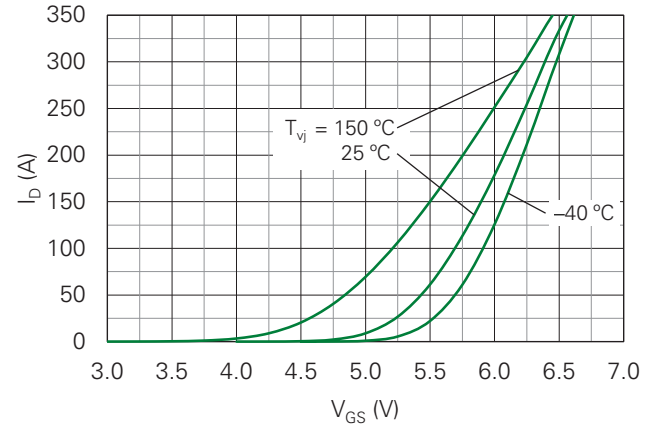


Fig. 9. Transconductance

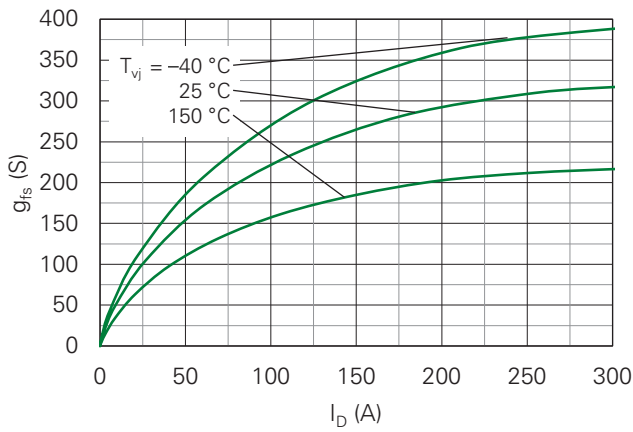


Fig. 10. Forward Voltage Drop of Intrinsic Diode

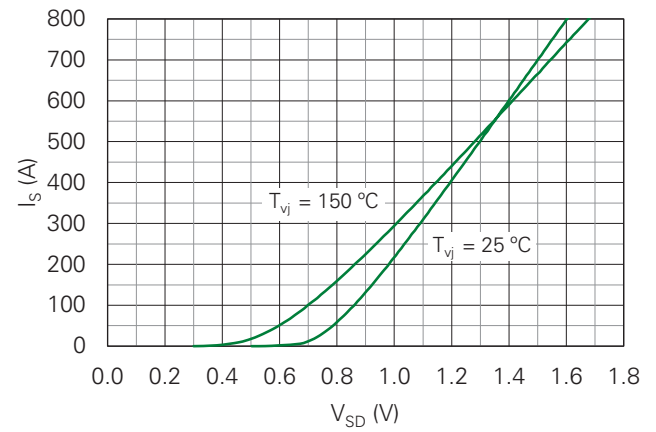


Fig. 11. Gate Charge

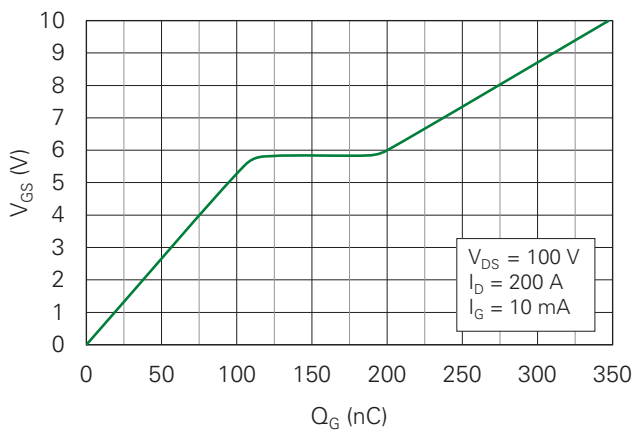


Fig. 12. Capacitance

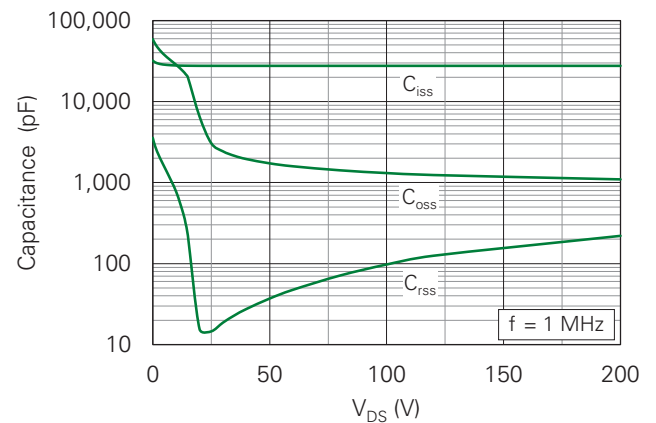


Fig. 13. Output Capacitance Stored Energy

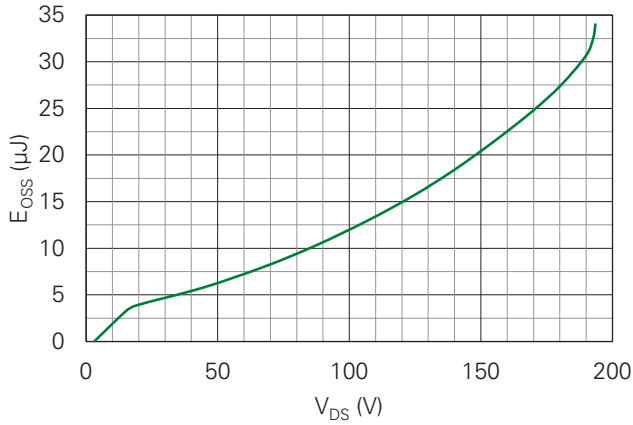


Fig. 14. Forward-Bias Safe Operating Area

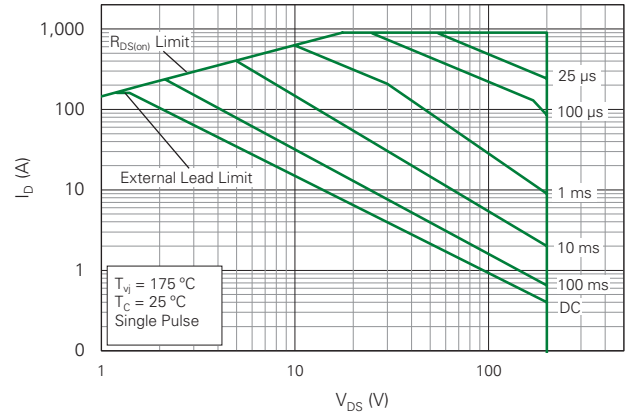


Fig. 15. Resistive Switching Times vs. Gate Resistance @ $I_D = 100\text{A}$

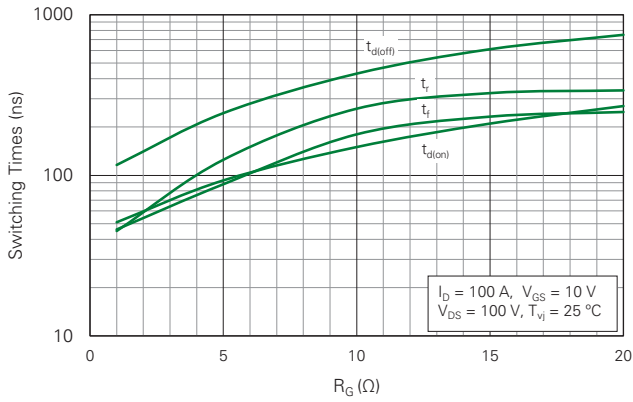


Fig. 16. Resistive Switching Times vs. Gate Resistance @ $I_D = 200\text{A}$

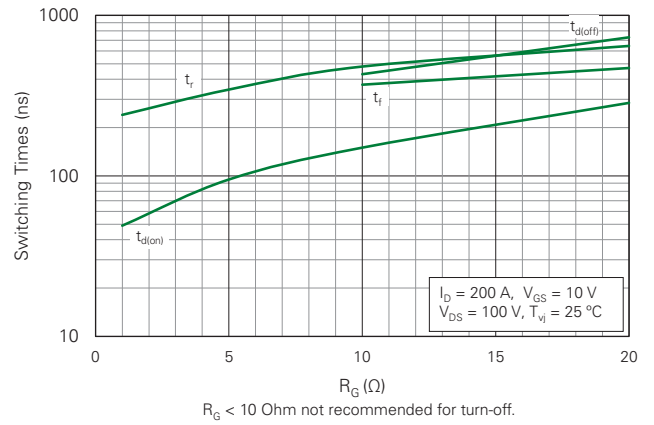


Fig. 17. Resistive Switching Times vs. Drain Current

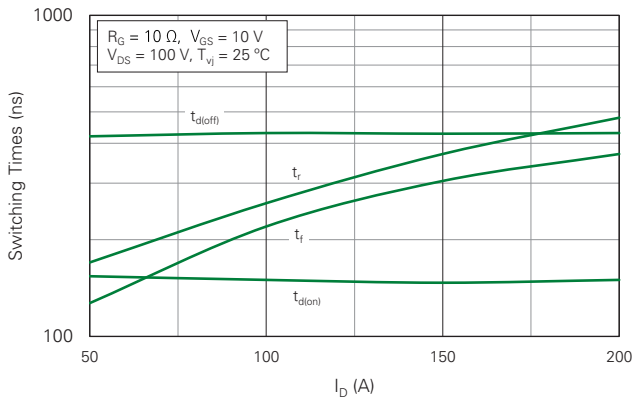
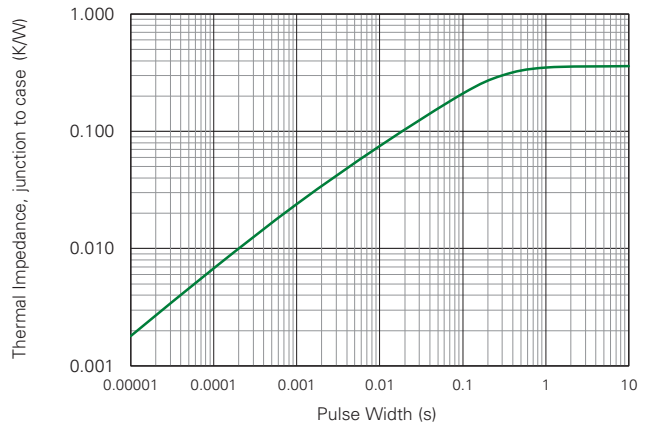
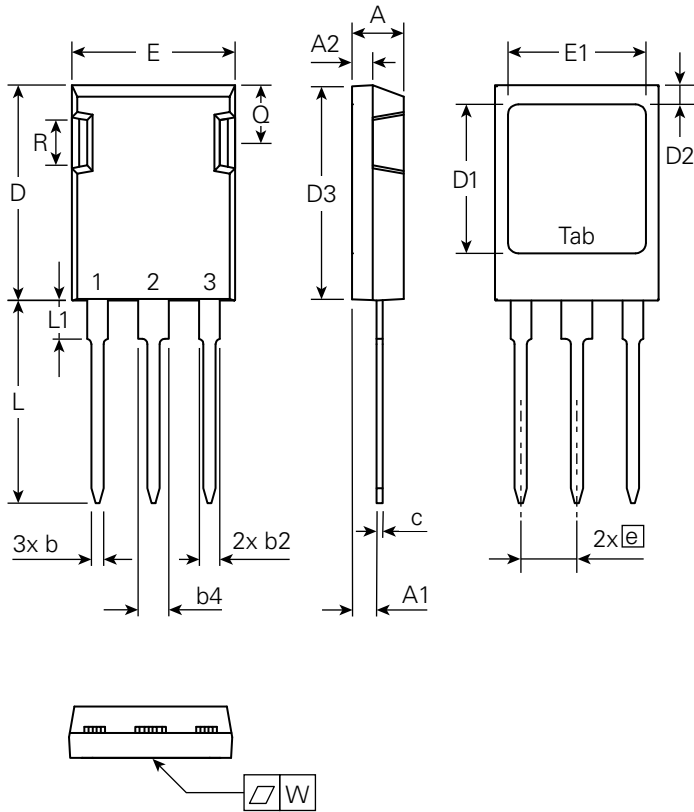


Fig. 18. Maximum Transient Thermal Impedance



Part Outline Drawing ISOPLUS-247-3L (IXTR)



Symbol	Inches			Millimeters		
	Min.	Typical	Max.	Min.	Typical	Max
A	0.190	–	0.205	4.83	–	5.21
A1	0.090	–	0.100	2.29	–	2.54
A2	0.075	–	0.085	1.91	–	2.16
b	0.045	–	0.055	1.14	–	1.40
b2	0.075	–	0.087	1.91	–	2.20
b4	0.115	–	0.128	2.92	–	3.24
c	0.024	–	0.033	0.61	–	0.83
D	0.819	–	0.840	20.80	–	21.34
D1	0.620	–	0.640	15.75	–	16.26
D2	0.065	–	0.085	1.65	–	2.15
D3	0.799	–	0.815	20.30	–	20.70
E	0.620	–	0.635	15.75	–	16.13
E1	0.520	–	0.540	13.21	–	13.72
e	0.215 BSC			5.45 BSC		
L	0.780	–	0.811	19.81	–	20.60
L1	0.150	–	0.172	3.81	–	4.38
Q	0.220	–	0.244	5.59	–	6.20
R	0.167	–	0.217	4.25	–	5.50
W	–	–	0.004	–	–	0.10

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