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LF2136B

3-Phase Half Bridge Gate Driver

Features

- Three floating high-side drivers in bootstrap operation to 600V
- 200mA source / 350mA sink output current capability
- Outputs tolerant to negative transients, dV/dt immune
- Wide VCC operating range: 10V to 20V
- Logic input 3.3V capability
- Internal deadtime of 290ns to protect MOSFETs
- Matched propagation delay for all channels
- Outputs out of phase with inputs
- Schmitt triggered logic inputs
- Cross conduction prevention logic
- Under Voltage Lockout (UVLO) for all channels
- Overcurrent protection shuts down drivers

Description

LF2136B is a three-phase gate driver IC designed for high voltage, high speed applications, driving N-channel MOSFETs and IGBTs in a half-bridge configuration. The high voltage process enables the LF2136B high sides to switch up to 600V in a bootstrap operation.

LF2136B logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with controlling devices and are enabled low to better function in high noise environments. The driver outputs feature high pulse current buffers designed for minimum driver cross conduction.

LF2136B offers numerous protection functions. A shoot-through protection logic prevents both outputs being high with both inputs low (fault state), an under-voltage lockout (UVLO) for V_{CC} shuts down all drivers through an internal fault control, while a UVLO for V_{BS} shuts down the respective high side output. Additionally an overcurrent protection will terminate all six outputs. Both the V_{CC} UVLO and the overcurrent protection activate an automatic fault clear with a timing that is adjustable with an external capacitor.

LF2136B is offered in an SOIC-28 package and operates over an extended temperature range of -40 °C to +125 °C .

Applications

- 3-Phase Motor Inverter Driver
- White Goods - Air Conditioner, Washing Machine, Refrigerator
- Industrial Motor Inverter - Power Tools, Robotics
- General Purpose 3-Phase Inverter

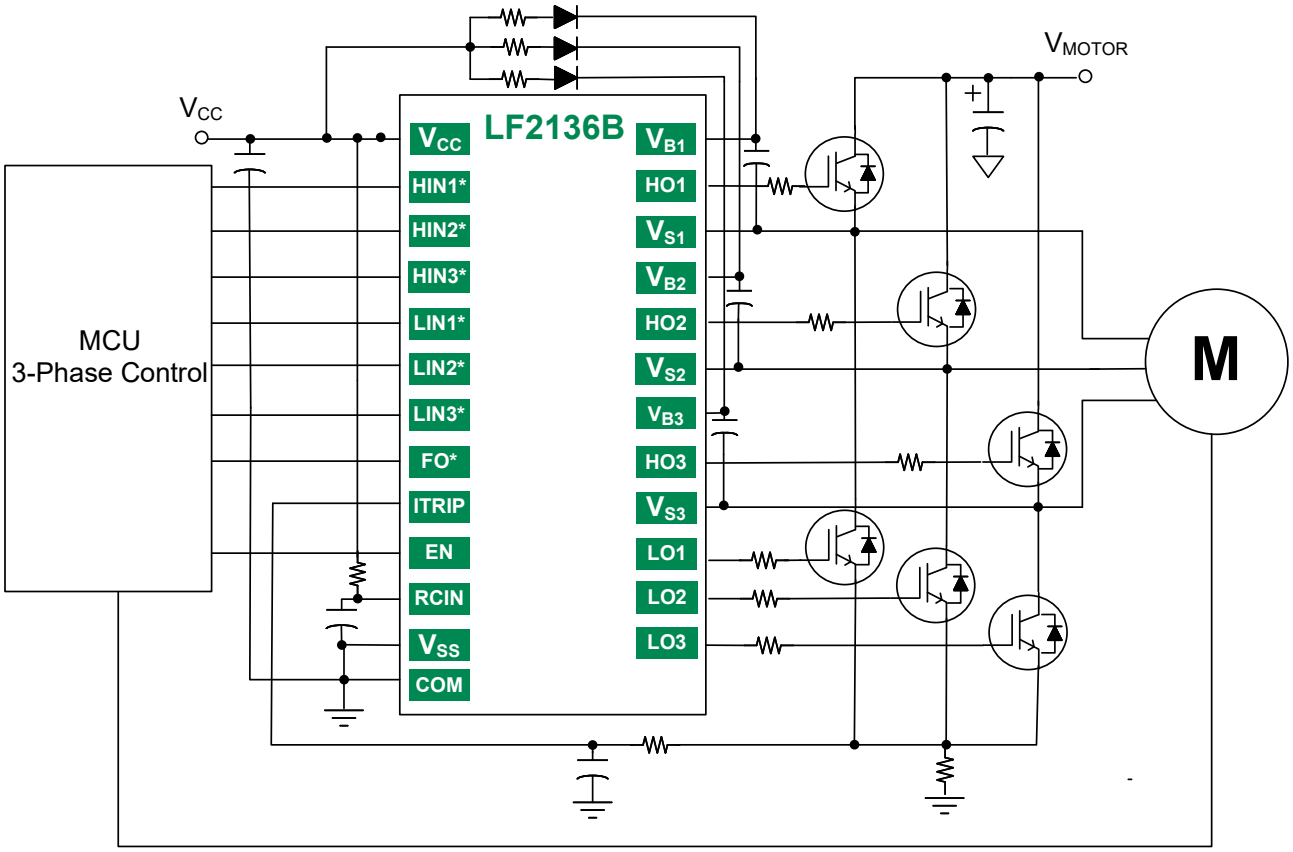
SOIC-28

Ordering Information

Year Year Week Week

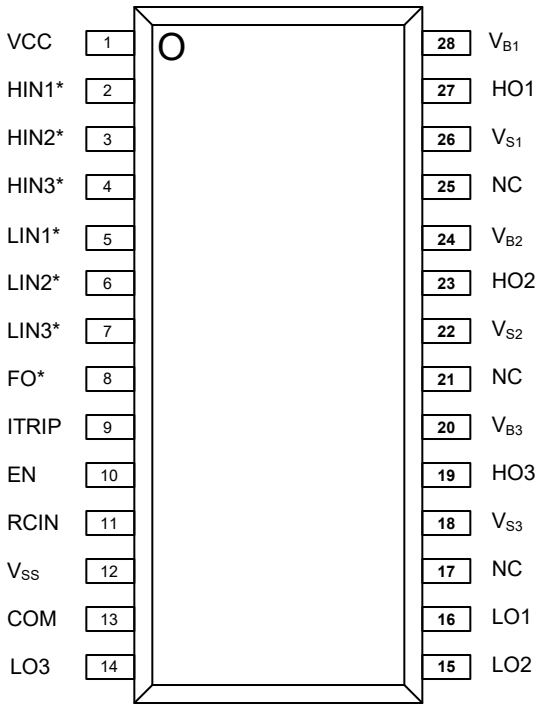
Part#	Package	Pack / Qty	MARK
LF2136BTR	SOIC-28	T&R / 1500	YYWW LF2136B LOT ID

Typical Application



1 Specifications

1.1 Pin Diagrams



Top View: SOIC-28

1.2 Pin Descriptions

Pin#	Pin Name	Pin Type	Pin Description
1	V_{CC}	Power	Low-side and logic fixed supply
2, 3, 4	HIN1*, HIN2*, HIN3*	Input	Logic input for high-side gate driver output, out of phase with HO.
5, 6, 7	LIN1*, LIN2*, LIN3*	Input	Logic input for low-side gate driver output, out of phase with LO.
8	FO*	Output	Fault active low with open drain output (fault with over-current and V_{CC} UVLO)
9	I_{TRIP}	Input	Analog input for over-current shutdown
10	EN	Input	Logic input for functionality, I/O logic functions when EN is high.
11	RCIN	Input	An external RC network input used to define FAULT CLEAR delay
12	V_{SS}	Power	Logic ground
13	COM	Power	Low-side driver return
14, 15, 16	LO3, LO2, LO1	Output	Low-side gate driver output
17, 21, 25	NC	No Connect	Not Connected internally
18, 22, 26	V_{S3},V_{S2},V_{S1}	Power	High-side floating supply return
19, 23, 27	HO3, HO2, HO1	Output	High-side gate driver output
20, 24, 28	V_{B3},V_{B2},V_{B1}	Power	High-side floating supply

1.3 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
High-side floating supply voltage	V_B	-0.3	+624	V
High-side floating supply offset voltage	V_S	V_B-24	V_B+0.3	V
High- side floating output voltage	V_{HO}	V_S-0.3	V_B+0.3	V
Low-side output voltage	V_{LO}	-0.3	V_{CC}+0.3	V
Offset supply voltage transient	dV_S/dt	--	50	V/ns
Low-side fixed supply voltage	V_{CC}	-0.3	+24	V
Input voltage (HIN*, LIN*, ITRIP , EN)	V_{IN}	V_{SS}-0.3	V_{SS}+5.5	V
Fault output voltage	V_{FO*}	V_{SS}-0.3	V_{CC}+0.3	V
Logic Ground	V_{SS}	-5	5	V
Package power dissipation	P_D	--	1.6	W
Junction Operating Temperature	T_J	--	+150	° C
Storage Temperature	T_{STG}	-55	+150	° C

Unless otherwise specified all voltages are referenced to COM . All electrical ratings are at T_A = 25 °C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1.4 Thermal Characteristics

Parameter	Symbol	Rating	Unit
Junction to ambient	$\emptyset_{JA}$	78	°C/W

Thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

1.5 Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Unit
High side floating supply voltage	V_B	V_S + 10	V_S + 20	V
High side floating supply offset voltage	V_S	**NOTE1**	600	V
High side floating output voltage	V_{HO}	V_S	V_B	V
Low side and logic fixed supply voltage	V_{CC}	10	20	V
Low side output voltage	V_{LO}	COM	V_{CC}	V
Input voltage (HIN*, LIN*, ITRIP, EN)	V_{IN}	V_{SS}	V_{SS}+5	V
Fault output Voltage	V_{FO*}	V_{SS}	V_{CC}	V
RCIN input voltage	V_{RCIN}	V_{SS}	V_{CC}	V
Logic Ground	V_{SS}	-5	5	V

Unless otherwise specified all voltages are referenced to COM

NOTE1 *High-side driver remains operational for V_S transients down to -5V*

1.6 DC Electrical Characteristics

V_{CC}= V_{BS} = 15V, T_A = 25 °C and V_{SS}= V_{COM} = 0V , unless otherwise specified.

The V_{IN} and I_{IN} parameters are applicable to all six channels (HIN1,2,3 and LIN1,2,3*). The V_O and I_O parameters are applicable to the outputs (HO1,2,3 and LO1,2,3) and are referenced to COM.*

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Logic "1" input voltage	V_{IH}	**NOTE2**	2.4	--	--	V
Logic "0" input voltage	V_{IL}		--	--	0.8	
Logic input voltage hysteresis	$V_{IN(HYS)}$		--	0.7	--	
High level output voltage, V_{BIAS} - V_O	V_{OH}	I_O = 0mA	--	--	0.1	
Low level output voltage, V_O	V_{OL}	I_O = 0mA	--	--	0.1	
Offset supply leakage current	I_{LK}	V_B = VS = 600V	--	--	10	µA
Quiescent V_{BS} supply current	I_{BSQ}	V_{IN} = 0V or 5V, EN=0V	10	85	130	
Quiescent V_{CC} supply current	I_{CCQ}	V_{IN} = 0V or 5V, EN=0V	--	1.1	1.6	mA
Driver logic "0" input bias current	I_{IN+}	V_{IN} = 0V	--	130	200	µA
Driver logic "1" input bias current	I_{IN-}	V_{IN} = 5V	--	3.0	20	
Enable logic "1" input bias current	I_{EN+}	V_{EN} = 5V	--	33	80	µA
Enable logic "0" input bias current	I_{EN-}	V_{EN} = 0V	--	--	2	µA
V_{BS} and V_{CC} UVLO off positive going threshold	V_{BSUV+}, V_{CCUV+}	--	7.6	8.9	9.9	V
V_{BS} and V_{CC} UVLO enable negative going threshold	V_{BSUV-} V_{CCUV-}	--	7.1	8.3	9.4	
V_{BS} and V_{CC} UVLO hysteresis	$V_{BSUV(HYS)}$, $V_{CCUV(HYS)}$	--	--	0.65	--	
Output high short circuit pulsed current	I_{O+}	V_O = 0V, t ≤ 10 µs	120	200	--	mA
Output low short circuit pulsed current	I_{O-}	V_O = 15V, t ≤ 10 µs	250	350	--	
Overcurrent detect positive threshold	V_{ITRIP+}	--	400	500	600	mV
Overcurrent detect negative threshold	$V_{I TRIP-}$	--	340	420	500	mV
ITRIP input bias current	I_{ITRIP}	V_{ITRIP}=1V	--	11	16	µA
RCIN Positive going threshold voltage	V_{RCIN+}	--	7.0	8.4	9.8	V
RCIN Negative going threshold voltage	V_{RCIN-}	--	--	5	--	V
FO* logic low output voltage	V_{FO*L}	V_{ITRIP}=1V, I_{FO*}=1.5mA	--	0.2	0.5	V
RCIN On resistance	$R_{ON(RCIN)}$	I_{RCIN}=1.5mA	40	75	110	Ω
FO* logic low output on-resistance	$R_{ON(FO*)}$	I_{FO*}=1.5mA	80	130	180	Ω

NOTE2 *For optimal operation, it is highly recommended that the input pulse (HIN1,2,3* and LIN1,2,3*) should have a minimum amplitude of 2.4V with a minimum pulse width of 600ns .*

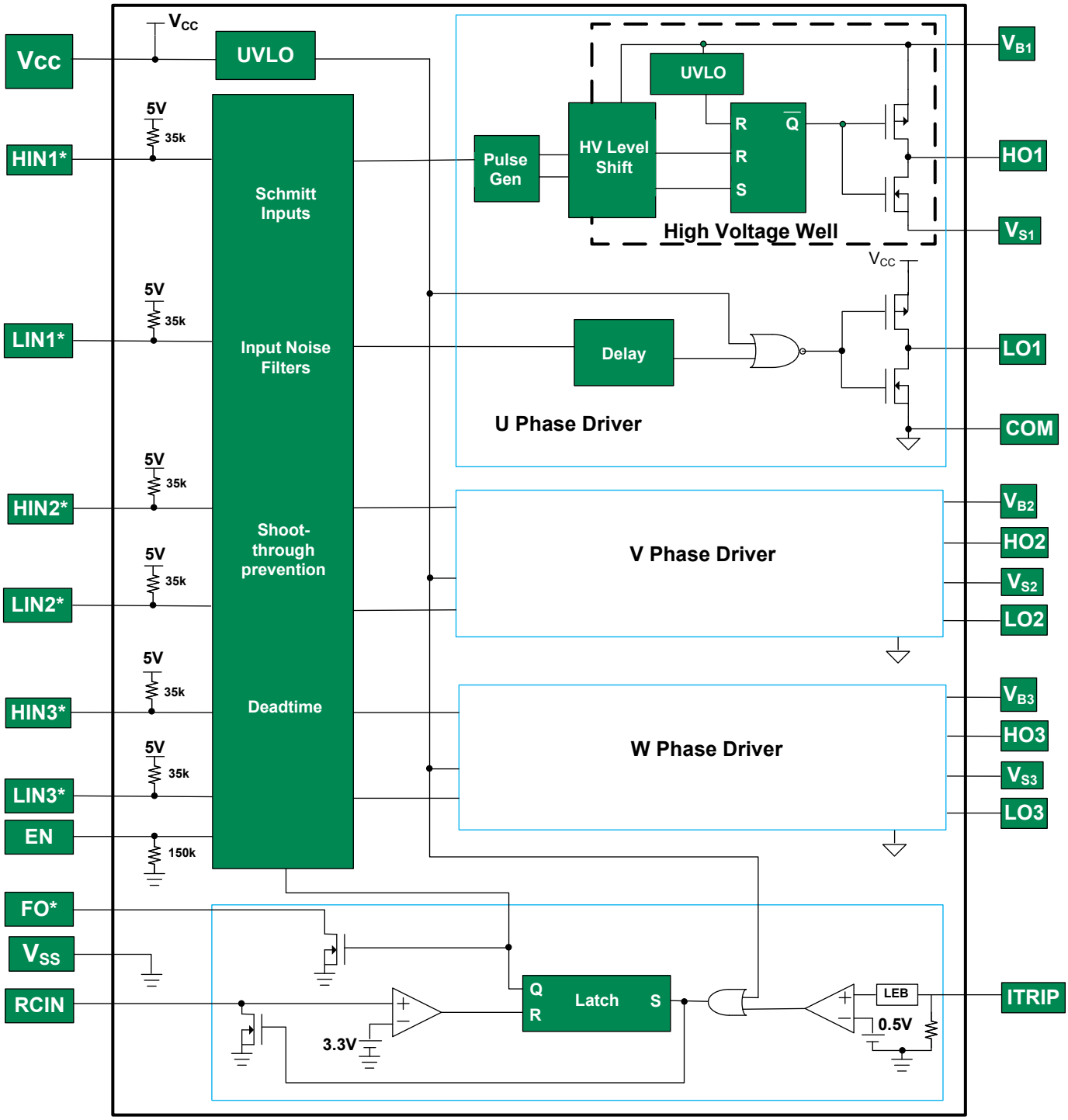
1.7 AC Electrical Characteristics

V_{CC}= V_{BS}=15V, T_A = 25 °C, C_L=1000pF, and V_{SS} = V_{COM} = 0V unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typical	Max	Unit
Turn-on propogation delay	t_{on}	V_S = 0V	200	330	460	ns
Turn-off propogation delay	t_{off}	V_S = 0V	200	330	460	
Turn-on rise time	t_r	V_S = 0V	--	90	150	
Turn-off fall time	t_f		--	35	60	
Propogation delay matching	t_{DM}	--	--	--	50	ns
Enable low to output shutdown delay	t_{EN}	--	225	330	425	ns
ITRIP Pin leading-edge blanking time	t_{BLT}	--	200	300	400	ns
ITRIP to FO* propagation delay	t_{FLT}	V_{ITRIP}= 1V	320	550	760	ns
ITRIP all gate outputs off propagation delay	t_{ITRIP}	V_{ITRIP}= 1V All outputs	380	615	820	ns
Input filtering time (HIN*, LIN*, EN)	t_{FLTIN}		--	250	--	ns
Fault clear delay	t_{FLTCLR}	C_{RCIN} = 1nF, R_{RCIN} = 2MΩ	--	1.6	--	ms
Deadtime	t_{DT}	--	200	290	420	ns
Deadtime matching	t_{DTM}	--	--	--	50	ns
Output pulse width matching t_{PM} = $\lvert t_{IN} - t_{OUT} \rvert$	t_{PM}	t_{IN} > 1µs	--	50	75	ns

2 Functional Specifications

2.1 Functional Block Diagram



2.2 Timing Waveforms

Figure 1. Input-to-Output Delay Timing Diagram

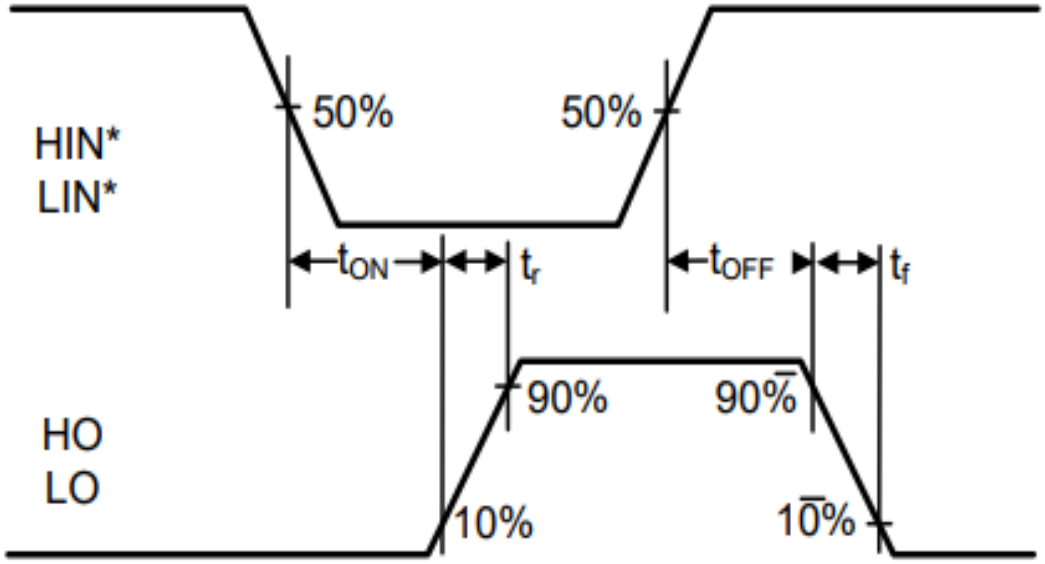
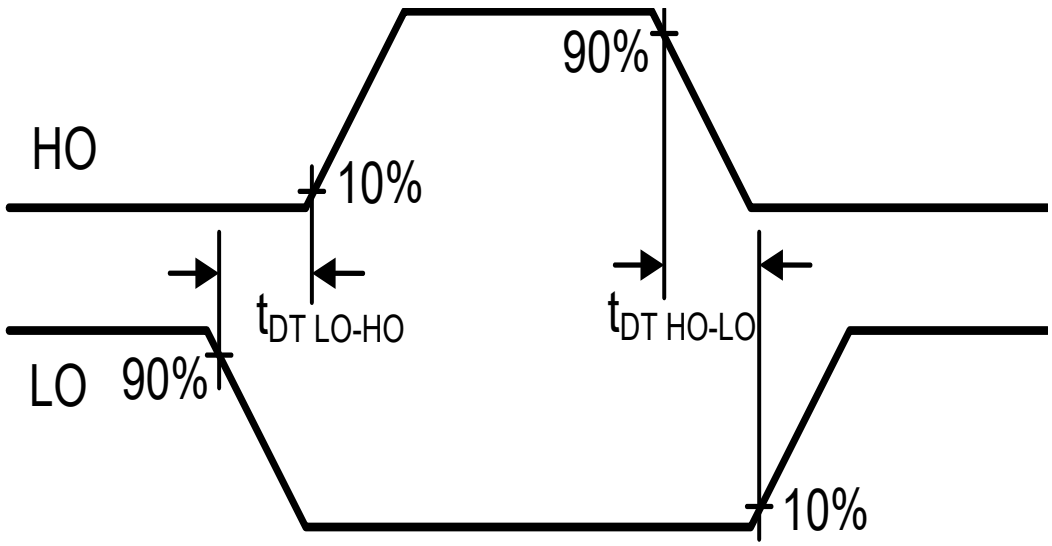


Figure 2. Deadtime Waveform Diagram



$$t_{DTM} = |t_{DT\ LO\text{-}HO} - t_{DT\ HO\text{-}LO}|$$

Figure 3. Input to Output Logic Diagram

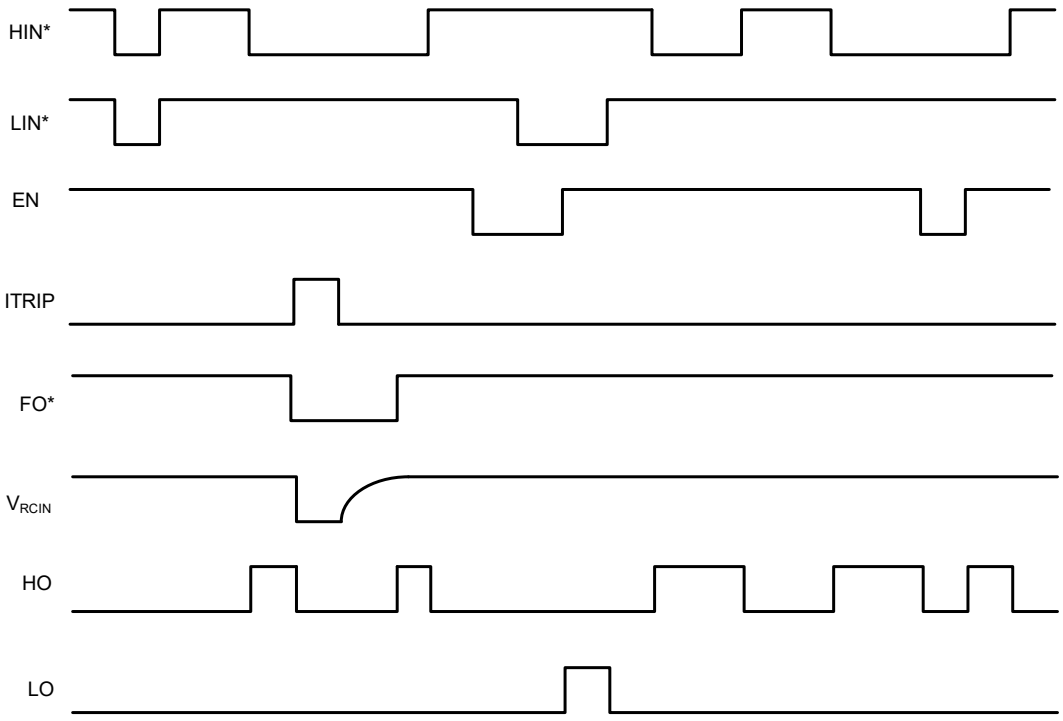
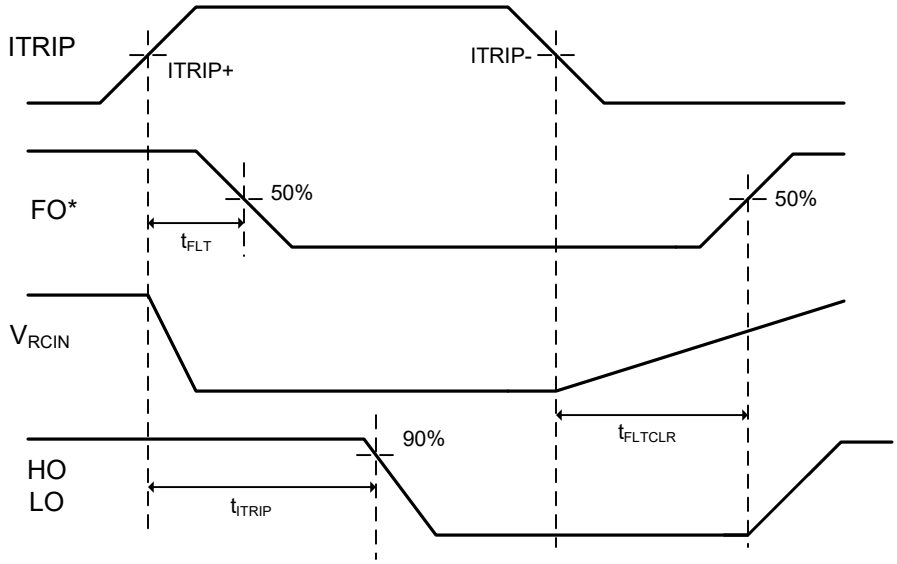


Figure 4. Overcurrent Timing Diagram



2.3 Application Information

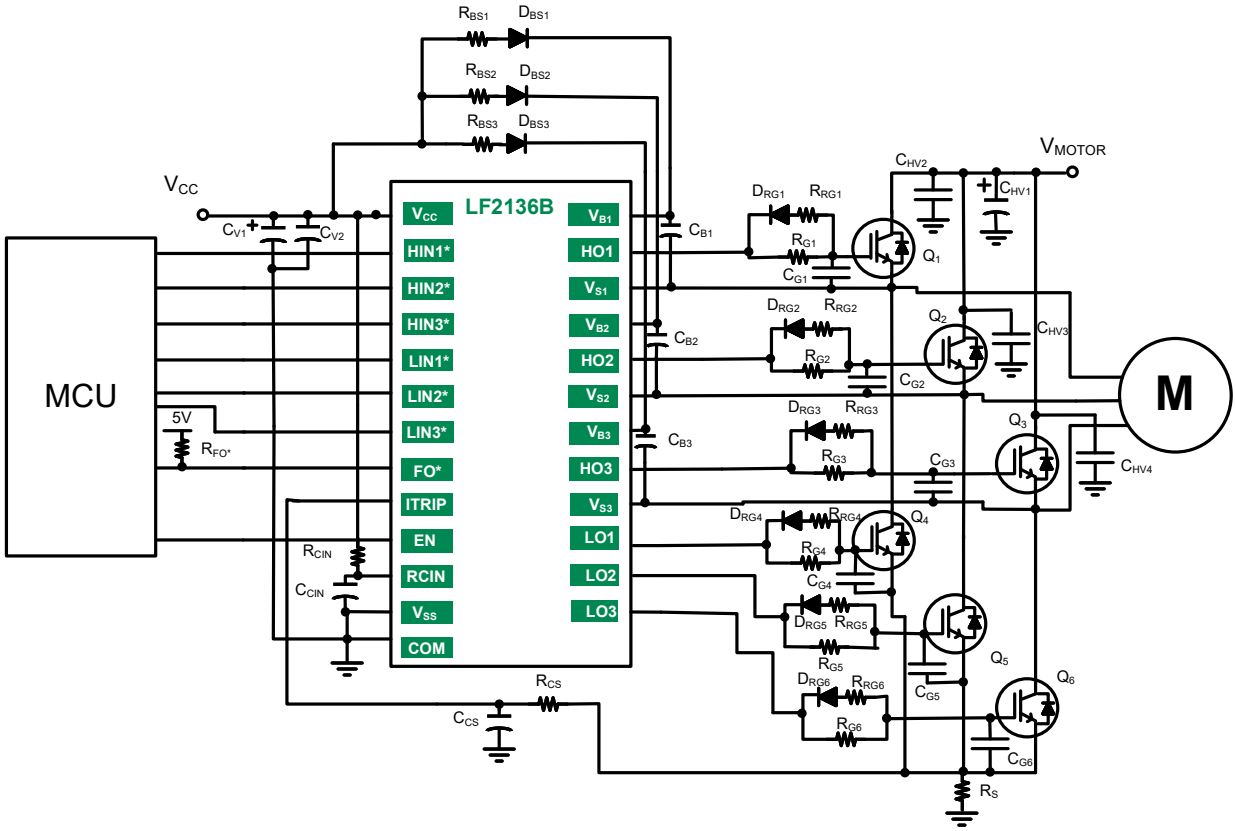


Figure 5. LF2136B in a 3 phase motor drive application.

- RRG1 - RRG6 values are typically between 0Ω and 10Ω, exact value decided by MOSFET junction capacitance and drive current of gate driver; 10Ω is used in this example.

- It is **highly recommended** that the input pulse (to HINx* and LINx*) should have minimum amplitude of 2.4V with a minimum pulse width of 600ns.

- RG1 - RG6 values are typically between 20Ω and 100Ω, exact value decided by MOSFET junction capacitance and drive current of gate driver; 50Ω is used in this example.

- RBS1 - RBS3 values are typically between 3Ω and 20Ω, exact value depending on bootstrap capacitor value and amount of current limiting required for bootstrap capacitor charging; 10Ω is used in this example. Also DB1 - DB3 should be an ultra fast diode of 1A rating minimum and voltage rating greater than system operating voltage.

3 Manufacturing Information

3.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. Littelfuse Integrated Circuits Division classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** rating as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033.**

Device	Moisture Sensitivity Level (MSL) Classification
LF2136B	MSL3

3.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

3.3 Reflow Profile

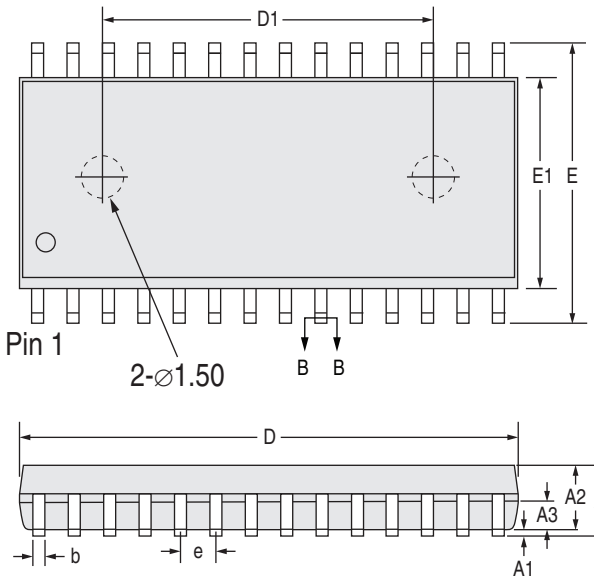
Provided in the table below is the IPC/JEDEC J-STD-020 Classification Temperature (T_C) and the maximum dwell time the body temperature of these surface mount devices may be (T_C - 5)°C or greater. The Classification Temperature sets the Maximum Body Temperature allowed for these devices during reflow soldering processes.

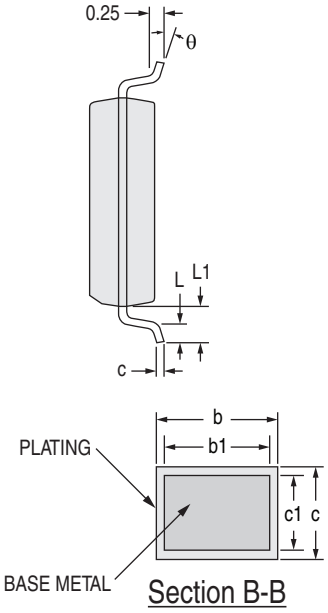
Device	Classification Temperature(Tc)	Dwell Time (tp)	Max Reflow Cycles
LF2136B	260°C	30 seconds	3

3.4 Board Wash

Littelfuse recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to halide flux or solvents.

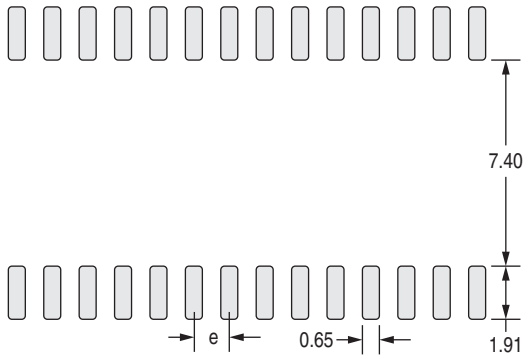
4 Package Dimensions: SOIC-28





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	2.65
A1	0.10	-	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.39	-	0.48
b1	0.38	0.41	0.43
c	0.25	-	0.31
c1	0.24	0.25	0.26
D	17.80	18.00	18.20
D1	11.90	12.00	12.10
E	10.10	10.30	10.50
E1	7.30	7.50	7.70
e	1.27 BSC		
L	0.70	-	1.00
L1	1.40 BSC		
θ	0°	-	8°

PCB Land Pattern



Important Notice

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