

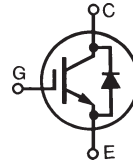
### BiMOSFET™ Monolithic Bipolar MOS Transistor

### IXBK75N170 IXBX75N170

$$V_{CES} = 1700V$$

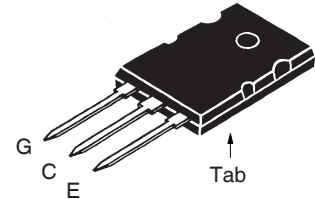
$$I_{C110} = 75A$$

$$V_{CE(sat)} \leq 3.1V$$

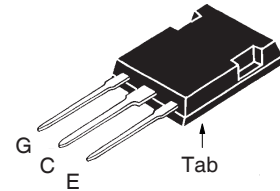


Symbol	Test Conditions	Maximum Ratings	
$V_{CES}$	$T_J = 25^\circ C$ to $150^\circ C$	1700	V
$V_{CGR}$	$T_J = 25^\circ C$ to $150^\circ C$ , $R_{GE} = 1M\Omega$	1700	V
$V_{GES}$	Continuous	$\pm 20$	V
$V_{GEM}$	Transient	$\pm 30$	V
$I_{C25}$	$T_C = 25^\circ C$ (Chip Capability)	200	A
$I_{LRMS}$	$T_C = 25^\circ C$ (Lead RMS Limit)	160	A
$I_{C110}$	$T_C = 110^\circ C$	75	A
$I_{CM}$	$T_C = 25^\circ C$ , 1ms	580	A
<b>SSOA</b>	$V_{GE} = 15V$ , $T_{VJ} = 125^\circ C$ , $R_G = 1\Omega$	$I_{CM} = 150$	A
<b>(RBSOA)</b>	Clamped Inductive Load	$V_{CE} \leq 0.8 \cdot V_{CES}$	
$P_C$	$T_C = 25^\circ C$	1040	W
$T_J$		-55 ... +150	$^\circ C$
$T_{JM}$		150	$^\circ C$
$T_{stg}$		-55 ... +150	$^\circ C$
$T_L$	Maximum Lead Temperature for Soldering	300	$^\circ C$
$T_{SOLD}$	1.6 mm (0.062 in.) from Case for 10	260	$^\circ C$
$M_d$	Mounting Torque (TO-264)	1.13/10	Nm/lb.in.
$F_c$	Mounting Force (PLUS247)	20..120/4.5..27	N/lb.
<b>Weight</b>	TO-264	10	g
	PLUS247	6	g

#### TO-264 (IXBK)



#### PLUS247™ (IXBX)



G = Gate                      C = Collector  
E = Emitter                  Tab = Collector

#### Features

- International Standard Packages
- High Blocking Voltage
- High Current Handling Capability
- Anti-Parallel Diode

#### Advantages

- High Power Density
- Low Gate Drive Requirement
- Intergrated Diode Can Be Used for Protection

#### Applications

- Capacitor Discharge
- AC Switches
- Switch-Mode and Resonant-Mode Power Supplies
- UPS
- AC Motor Drives

Symbol	Test Conditions ( $T_J = 25^\circ C$ , Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$BV_{CES}$	$I_C = 250\mu A$ , $V_{GE} = 0V$	1700		V
$V_{GE(th)}$	$I_C = 1.5mA$ , $V_{CE} = V_{GE}$	2.5		5.5 V
$I_{CES}$	$V_{CE} = 0.8 \cdot V_{CES}$ , $V_{GE} = 0V$ $T_J = 125^\circ C$			25 $\mu A$ 2 mA
$I_{GES}$	$V_{CE} = 0V$ , $V_{GE} = \pm 20V$			$\pm 100$ nA
$V_{CE(sat)}$	$I_C = I_{C110}$ , $V_{GE} = 15V$ , Note 1 $T_J = 125^\circ C$	2.6 3.1	3.1	V V

### Symbol Test Conditions

( $T_J = 25^\circ\text{C}$  Unless Otherwise Specified)

### Characteristic Values

		Min.	Typ.	Max.		
$g_{fs}$	$I_C = I_{C110}, V_{CE} = 10V, \text{Note 1}$	34	56		S	
$C_{ies}$	$V_{CE} = 25V, V_{GE} = 0V, f = 1\text{MHz}$		6930		pF	
$C_{oes}$			400		pF	
$C_{res}$			150		pF	
$Q_g$	$I_C = I_{C110}, V_{GE} = 15V, V_{CE} = 0.5 \cdot V_{CES}$		350		nC	
$Q_{ge}$			50		nC	
$Q_{gc}$			160		nC	
$t_{d(on)}$	<b>Resistive load, <math>T_J = 25^\circ\text{C}</math></b> $I_C = I_{C110}, V_{GE} = 15V$		46		ns	
$t_r$			160		ns	
$t_{d(off)}$		$R_G = 1\Omega, V_{CE} = 0.5 \cdot V_{CES}$		260		ns
$t_f$				440		ns
$t_{d(on)}$	<b>Resistive load, <math>T_J = 125^\circ\text{C}</math></b> $I_C = I_{C110}, V_{GE} = 15V$		47		ns	
$t_r$			230		ns	
$t_{d(off)}$		$R_G = 1\Omega, V_{CE} = 0.5 \cdot V_{CES}$		260		ns
$t_f$				580		ns
$R_{thJC}$				0.12	$^\circ\text{C/W}$	
$R_{thCS}$		0.15			$^\circ\text{C/W}$	

### Reverse Diode

### Symbol Test Conditions

( $T_J = 25^\circ\text{C}$  Unless Otherwise Specified)

### Characteristic Values

		Min.	Typ.	Max	
$V_F$	$I_F = I_{C110}, V_{GE} = 0V, \text{Note 1}$			3.0	V
$t_{rr}$	$I_F = 37A, V_{GE} = 0V, -di_F/dt = 100A/\mu\text{s}$		1.5		$\mu\text{s}$
$I_{RM}$			50		A
$Q_{RM}$		$V_R = 100V, V_{GE} = 0V$		38.2	

### Note

1. Pulse test,  $t \leq 300\mu\text{s}$ , duty cycle,  $d \leq 2\%$ .

Additional provisions for lead-to-lead isolation are required at  $V_{CE} > 1200V$ .

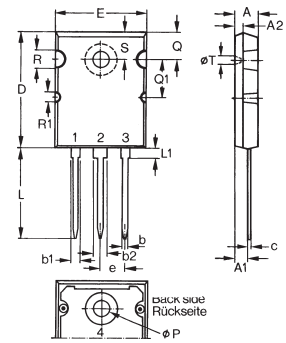
### PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

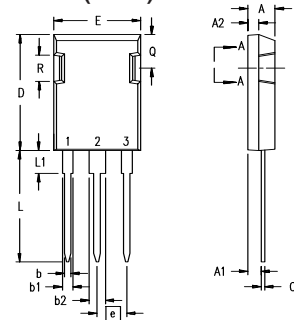
IXYS MOSFETs and IGBTs are covered 4,835,592 4,931,844 5,049,961 5,237,481 6,162,665 6,404,065 B1 6,683,344 6,727,585 7,005,734 B2 7,157,338 B2  
by one or more of the following U.S. patents: 4,850,072 5,017,508 5,063,307 5,381,025 6,259,123 B1 6,534,343 6,710,405 B2 6,759,692 7,063,975 B2  
4,881,106 5,034,796 5,187,117 5,486,715 6,306,728 B1 6,583,505 6,710,463 6,771,478 B2 7,071,537

### TO-264 AA ( IXBK) Outline



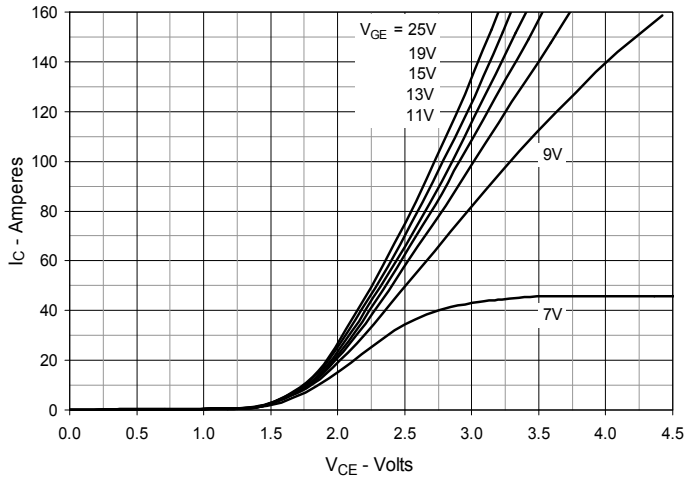
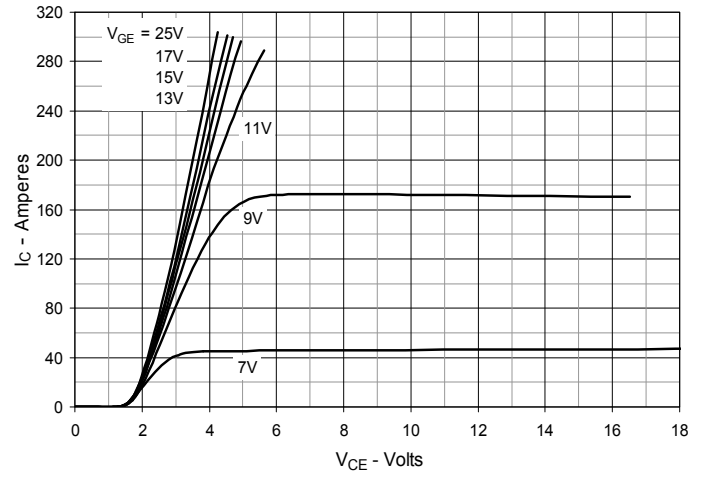
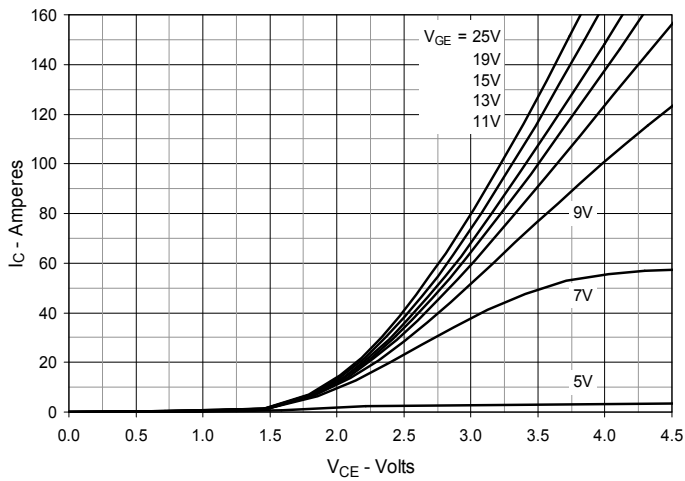
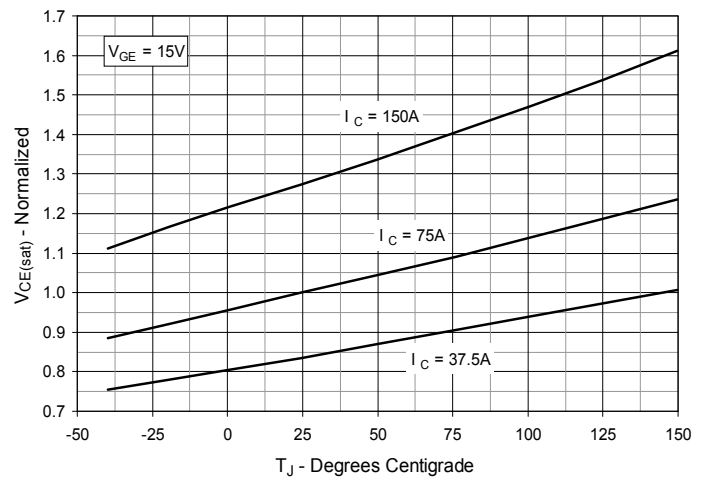
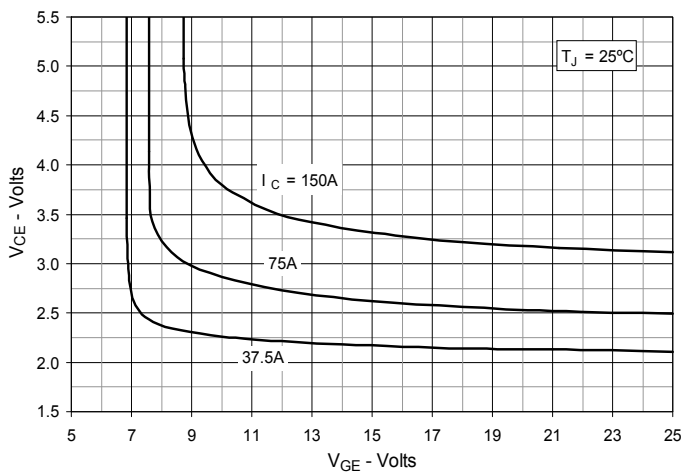
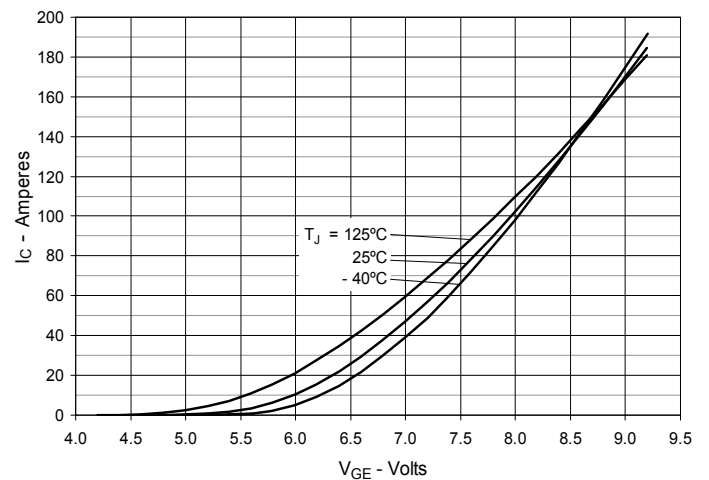
Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	4.82	5.13	.190	.202
A1	2.54	2.89	.100	.114
A2	2.00	2.10	.079	.083
b	1.12	1.42	.044	.056
b1	2.39	2.69	.094	.106
b2	2.90	3.09	.114	.122
c	0.53	0.83	.021	.033
D	25.91	26.16	1.020	1.030
E	19.81	19.96	.780	.786
e	5.46 BSC		.215 BSC	
J	0.00	0.25	.000	.010
K	0.00	0.25	.000	.010
L	20.32	20.83	.800	.820
L1	2.29	2.59	.090	.102
P	3.17	3.66	.125	.144
Q	6.07	6.27	.239	.247
Q1	8.38	8.69	.330	.342
R	3.81	4.32	.150	.170
R1	1.78	2.29	.070	.090
S	6.04	6.30	.238	.248
T	1.57	1.83	.062	.072

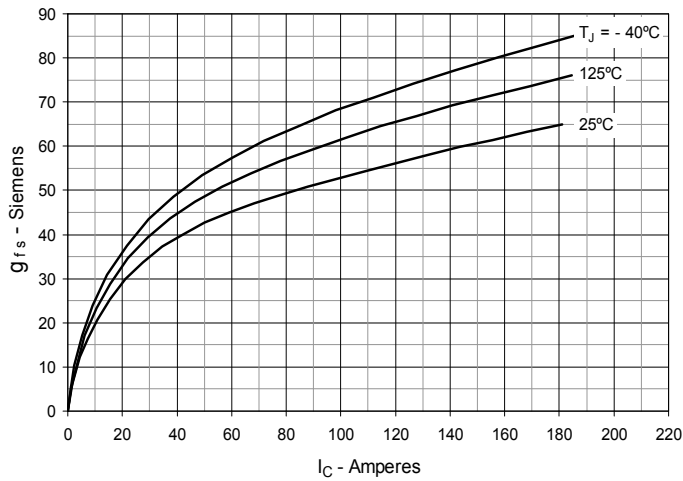
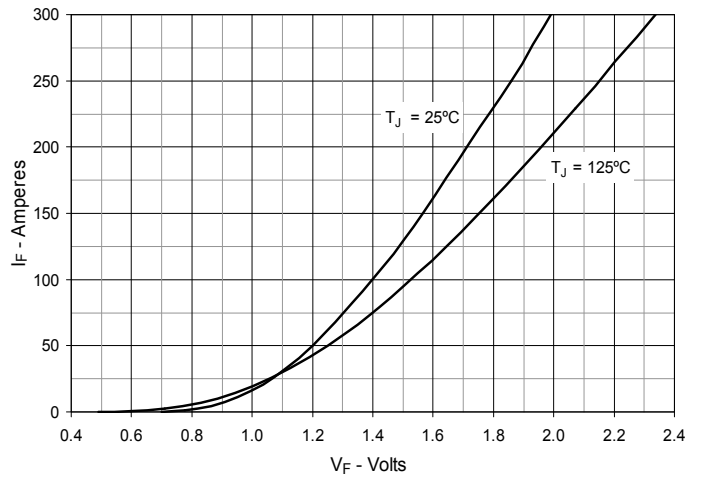
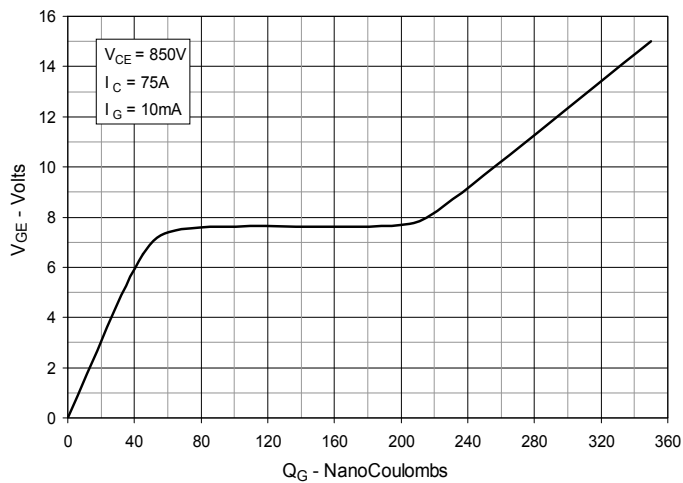
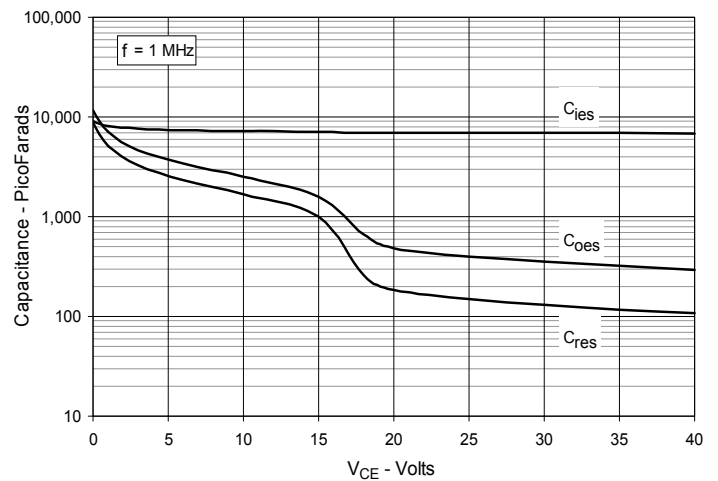
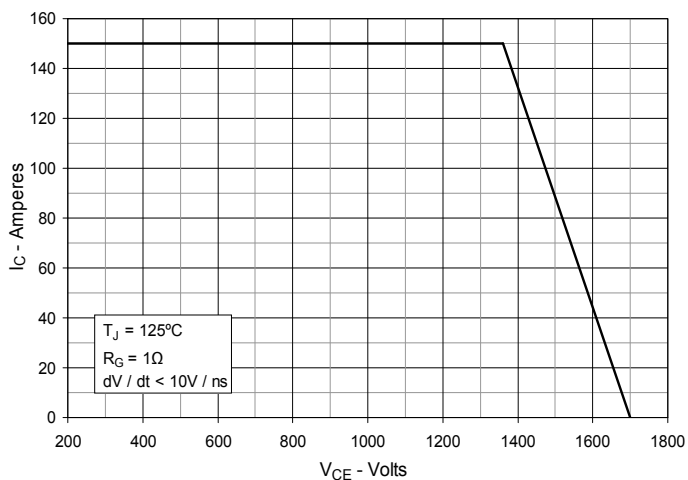
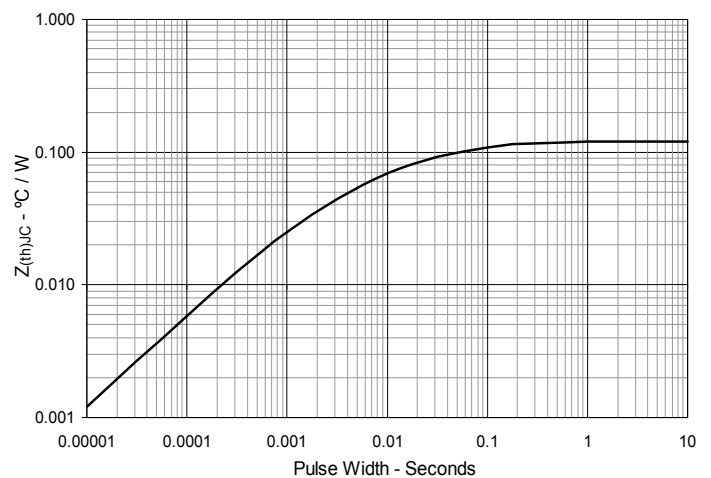
### PLUS247™ (IXBX) Outline



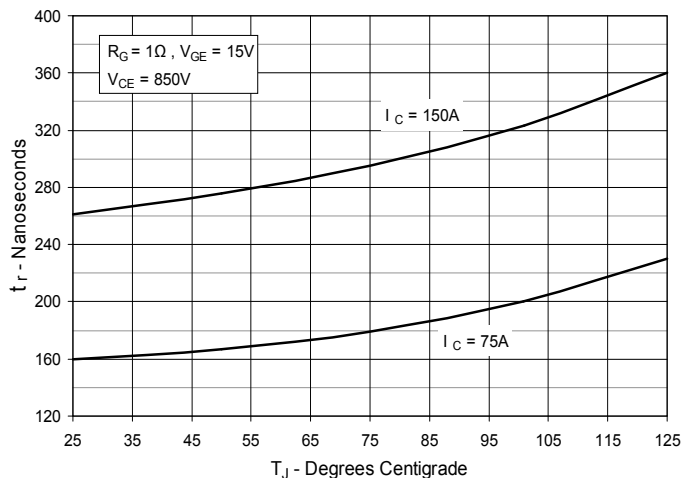
Terminals: 1 - Gate  
2 - Drain (Collector)  
3 - Source (Emitter)

Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	4.83	5.21	.190	.205
A <sub>1</sub>	2.29	2.54	.090	.100
A <sub>2</sub>	1.91	2.16	.075	.085
b	1.14	1.40	.045	.055
b <sub>1</sub>	1.91	2.13	.075	.084
b <sub>2</sub>	2.92	3.12	.115	.123
C	0.61	0.80	.024	.031
D	20.80	21.34	.819	.840
E	15.75	16.13	.620	.635
e	5.45 BSC		.215 BSC	
L	19.81	20.32	.780	.800
L1	3.81	4.32	.150	.170
Q	5.59	6.20	.220	0.244
R	4.32	4.83	.170	.190

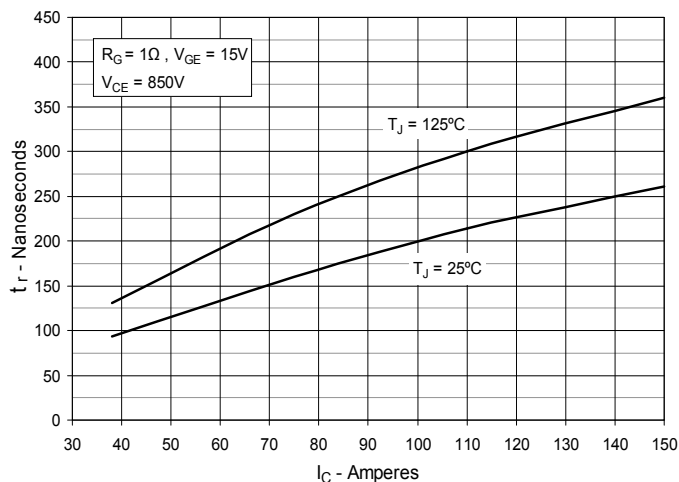
**Fig. 1. Output Characteristics  
@ 25°C**

**Fig. 2. Extended Output Characteristics  
@ 25°C**

**Fig. 3. Output Characteristics  
@ 125°C**

**Fig. 4. Dependence of  $V_{CE(sat)}$  on  
Junction Temperature**

**Fig. 5. Collector-to-Emitter Voltage  
vs. Gate-to-Emitter Voltage**

**Fig. 6. Input Admittance**


**Fig. 7. Transconductance**

**Fig. 8. Forward Voltage Drop of Intrinsic Diode**

**Fig. 9. Gate Charge**

**Fig. 10. Capacitance**

**Fig. 11. Reverse-Bias Safe Operating Area**

**Fig. 12. Maximum Transient Thermal Impedance**


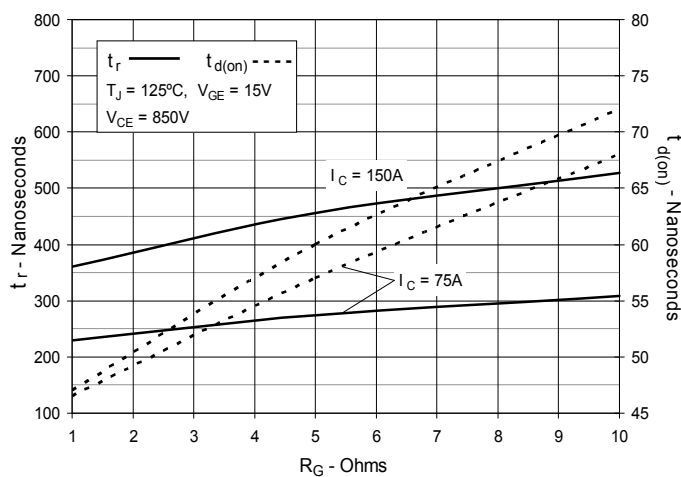
**Fig. 13. Resistive Turn-on  
Rise Time vs. Junction Temperature**



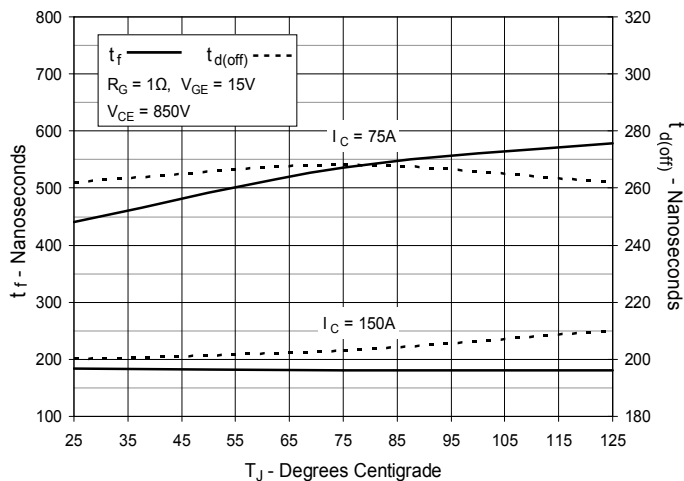
**Fig. 14. Resistive Turn-on  
Rise Time vs. Collector Current**



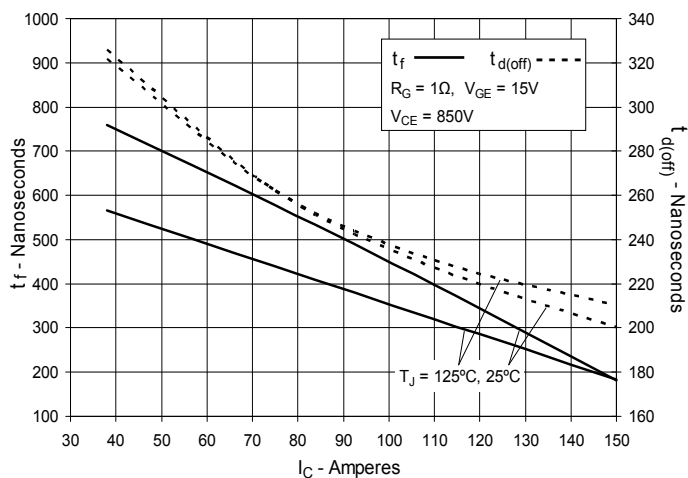
**Fig. 15. Resistive Turn-on  
Switching Times vs. Gate Resistance**



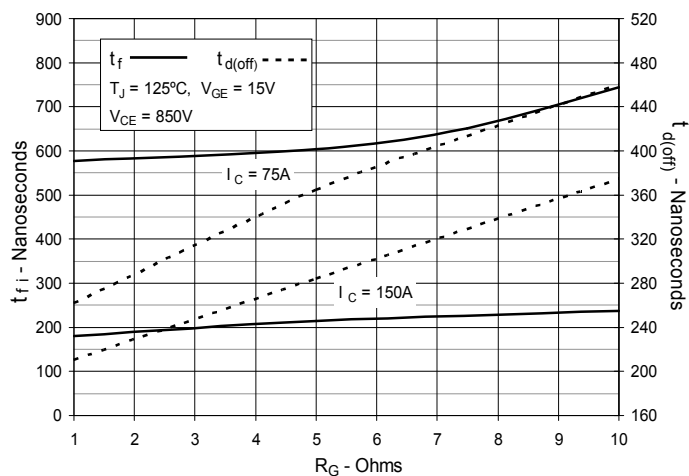
**Fig. 16. Resistive Turn-off  
Switching Times vs. Junction Temperature**



**Fig. 17. Resistive Turn-off  
Switching Times vs. Collector Current**



**Fig. 18. Resistive Turn-off  
Switching Times vs. Gate Resistance**





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