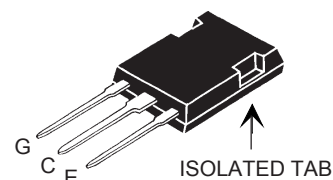


IXGR48N60C3D1

$$\begin{aligned} V_{CES} &= 600V \\ I_{C25} &= 56A \\ V_{CE(sat)} &\leq 2.7V \\ t_{fi(typ)} &= 38ns \end{aligned}$$

ISOPLUS 247™



G = Gate C = Collector
E = Emitter

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
 - UL Recognized Package
 - Isolated Mounting Surface
 - 2500V Electrical Isolation
- Avalanche Rated
- Square RBSOA
- Anti-Parallel Ultra Fast Diode
- Fast Switching
- International Standard Package

Advantages

- High Power Density
- Low Gate Drive Requirement

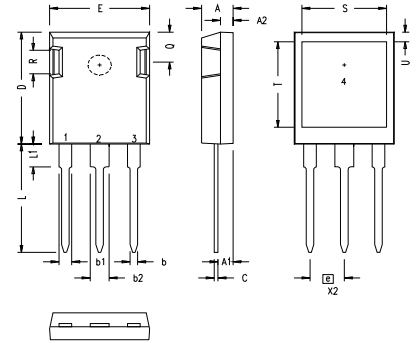
Applications

- High Frequency Power Inverters
- UPS
- Motor Drives
- SMPS
- PFC Circuits
- Battery Chargers
- Welding Machines
- Lamp Ballasts

Symbol	Test Conditions	Characteristic Values (T _J = 25°C, Unless Otherwise Specified)		
		Min.	Typ.	Max.
V _{GE(th)}	I _C = 250μA, V _{CE} = V _{GE}	3.0		5.5 V
I _{CES}	V _{CE} = V _{CES} V _{GE} = 0V T _J = 125°C			300 μA 1.75 mA
I _{GES}	V _{CE} = 0V, V _{GE} = ±20V			±100 nA
V _{CE(sat)}	I _C = 30A, V _{GE} = 15V, Note 1 T _J = 125°C		2.3 1.8	2.7 V V

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)		
		Min.	Typ.	Max.
g_{fs}	$I_C = 30\text{A}$, $V_{CE} = 10\text{V}$, Note 1	20	30	S
C_{ies}	$V_{CE} = 25\text{V}$, $V_{GE} = 0\text{V}$, $f = 1\text{MHz}$		1960	pF
C_{oes}			220	pF
C_{res}			66	pF
Q_g	$I_C = 30\text{A}$, $V_{GE} = 15\text{V}$, $V_{CE} = 0.5 \cdot V_{CES}$		77	nC
Q_{ge}			16	nC
Q_{gc}			32	nC
$t_{d(on)}$	Inductive Load, $T_J = 25^\circ\text{C}$ $I_C = 30\text{A}$, $V_{GE} = 15\text{V}$ $V_{CE} = 400\text{V}$, $R_G = 3\Omega$		19	ns
t_{ri}			26	ns
E_{on}			0.41	mJ
$t_{d(off)}$			60	ns
t_{fi}			38	ns
E_{off}			0.23	0.55 mJ
$t_{d(on)}$	Inductive Load, $T_J = 125^\circ\text{C}$ $I_C = 30\text{A}$, $V_{GE} = 15\text{V}$ $V_{CE} = 400\text{V}$, $R_G = 3\Omega$		19	ns
t_{ri}			26	ns
E_{on}			0.65	mJ
$t_{d(off)}$			92	ns
t_{fi}			95	ns
E_{off}			0.57	mJ
R_{thJC}				1.0 $^\circ\text{C/W}$
R_{thCS}			0.15	$^\circ\text{C/W}$

ISOPLUS247 (IXGR) Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b1	.075	.084	1.91	2.13
b2	.115	.123	2.92	3.12
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
E	.620	.635	15.75	16.13
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.520	.540	13.21	13.72
T	.620	.640	15.75	16.26
U	.065	.080	1.65	2.03

- 1 - GATE
2 - DRAIN (COLLECTOR)
3 - SOURCE (EMITTER)
4 - NO CONNECTION

NOTE: This drawing will meet all dimensions requirement of JEDEC outline TO-247AD except screw hole.

Reverse Diode (FRED)

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)		
		Min.	Typ.	Max.
V_F	$I_F = 30\text{A}$, $V_{GE} = 0\text{V}$, Note 1	$T_J = 25^\circ\text{C}$		2.7 V
I_{RM}	$I_F = 30\text{A}$, $V_{GE} = 0\text{V}$, $-di_F/dt = 100\text{A}/\mu\text{s}$, $V_R = 100\text{V}$	$T_J = 100^\circ\text{C}$		4 A
t_{rr}	$I_F = 1\text{A}$, $-di_F/dt = 100\text{A}/\mu\text{s}$; $V_R = 30\text{V}$	$T_J = 100^\circ\text{C}$	100 25	ns ns
R_{thJC}				1.5 $^\circ\text{C/W}$

Note 1: Pulse test, $t \leq 300\mu\text{s}$, Duty cycle, $d \leq 2\%$.

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338 B2
4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

Fig. 1. Output Characteristics
@ 25°C

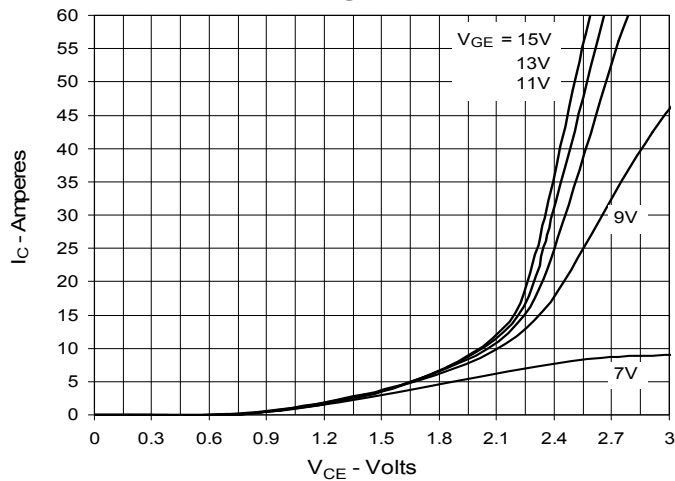


Fig. 2. Extended Output Characteristics
@ 25°C

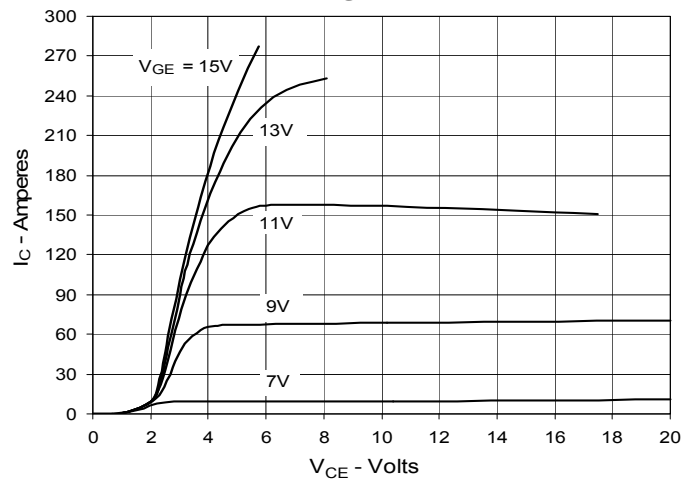


Fig. 3. Output Characteristics
@ 125°C

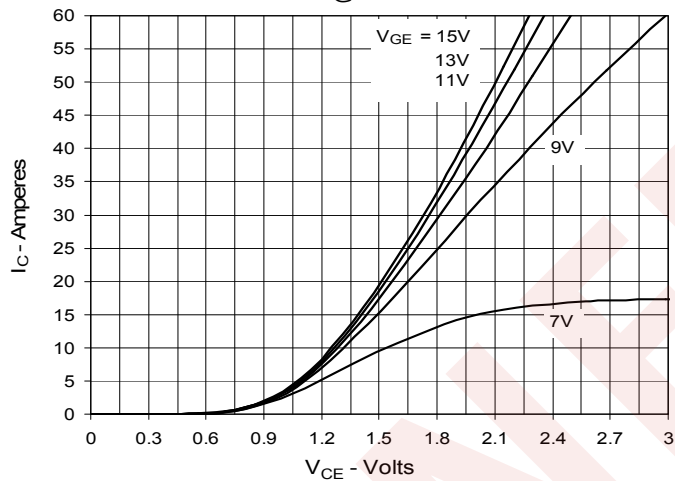


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

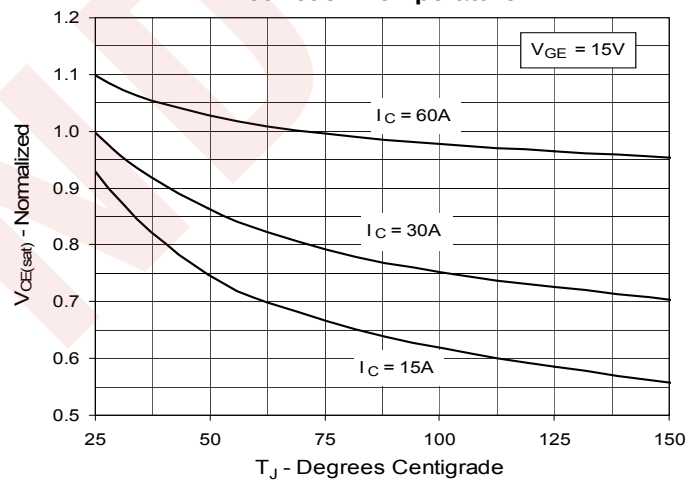


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

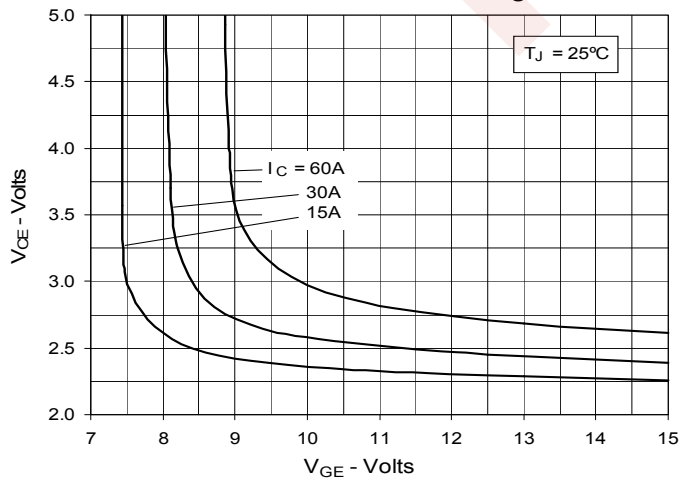


Fig. 6. Input Admittance

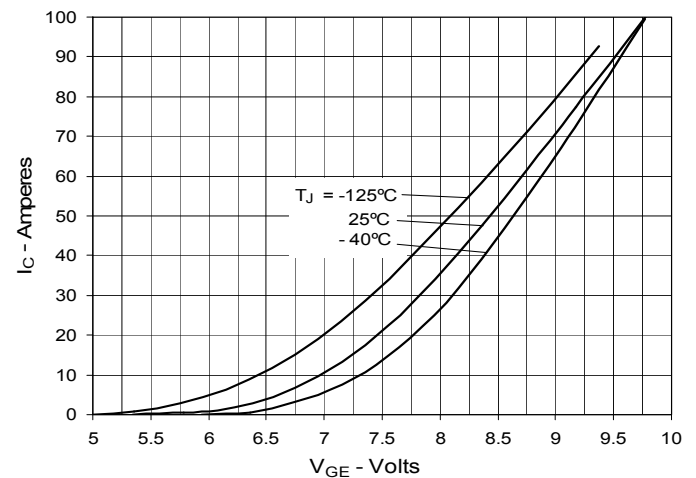


Fig. 7. Transconductance

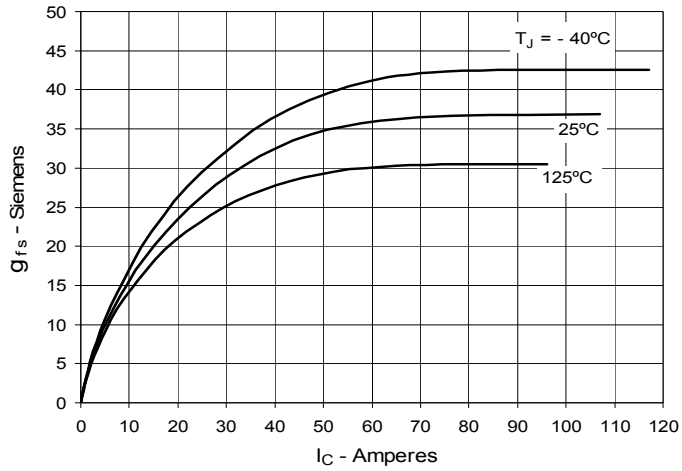


Fig. 8. Gate Charge

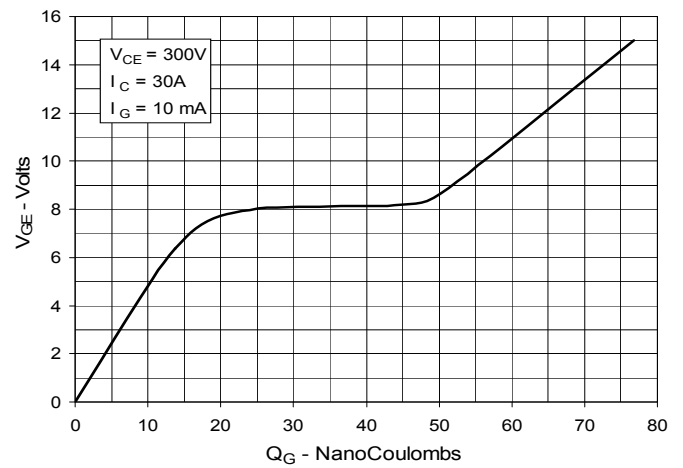


Fig. 9. Capacitance

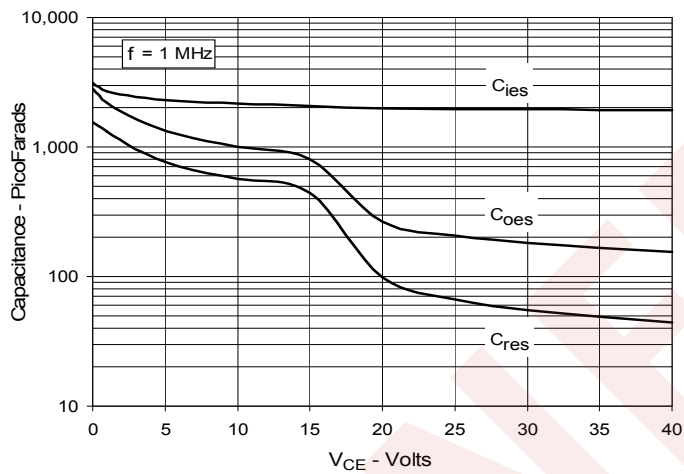


Fig. 10. Reverse-Bias Safe Operating Area

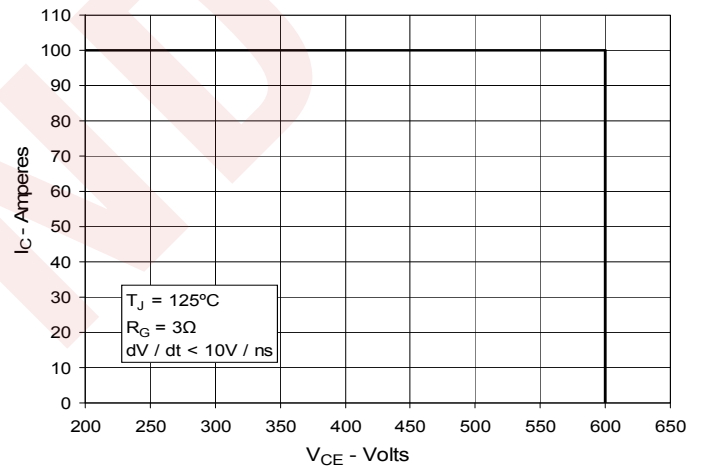
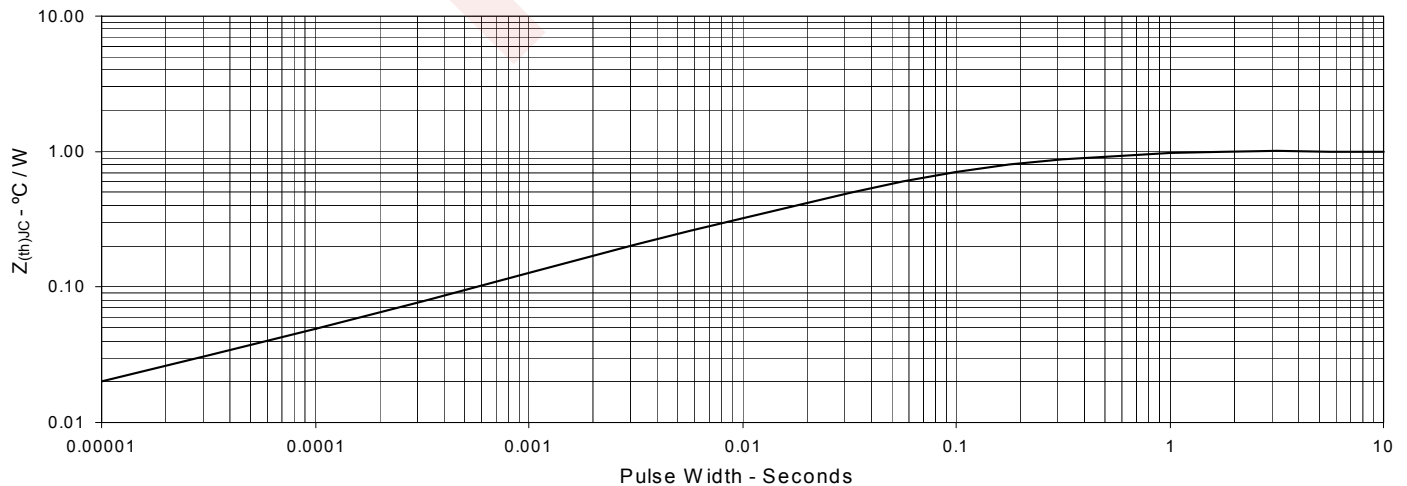
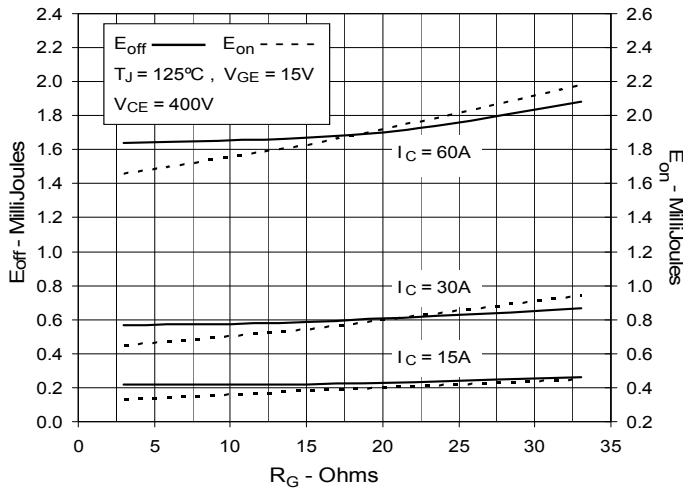


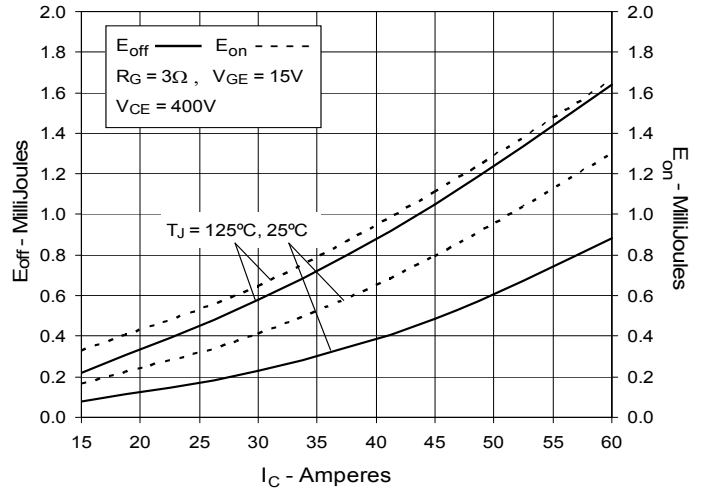
Fig. 11. Maximum Transient Thermal Impedance



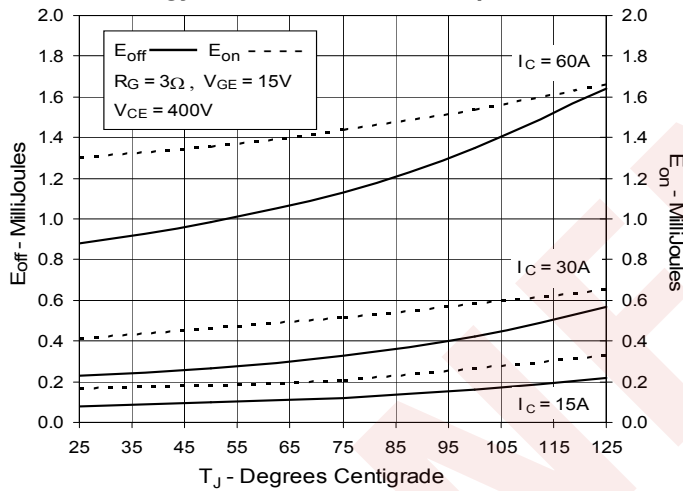
**Fig. 12. Inductive Switching
Energy Loss vs. Gate Resistance**



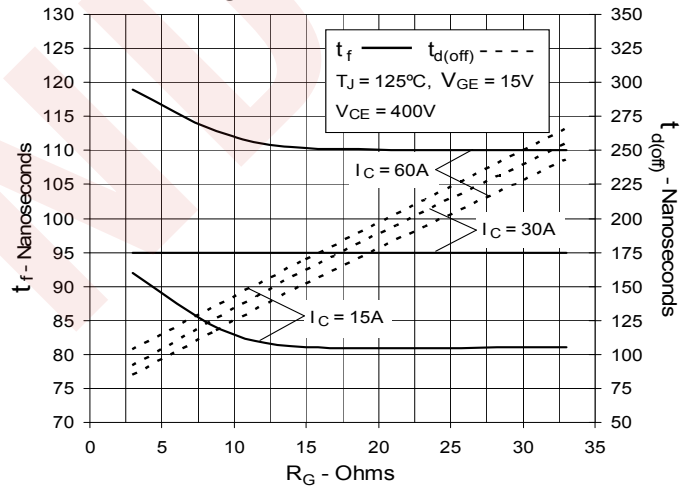
**Fig. 13. Inductive Switching
Energy Loss vs. Collector Current**



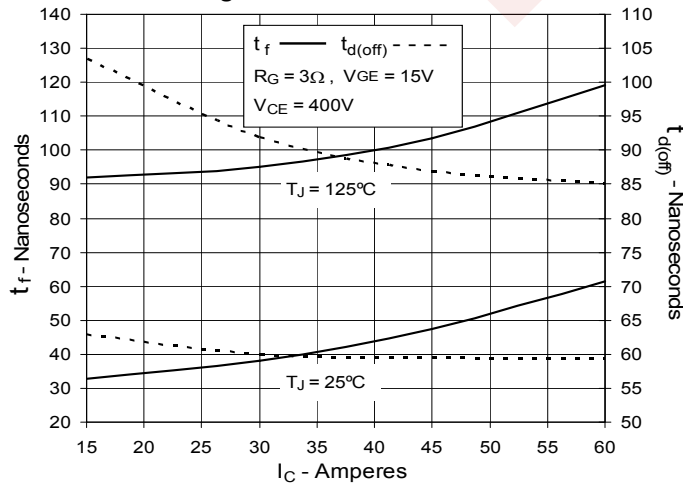
**Fig. 14. Inductive Switching
Energy Loss vs. Junction Temperature**



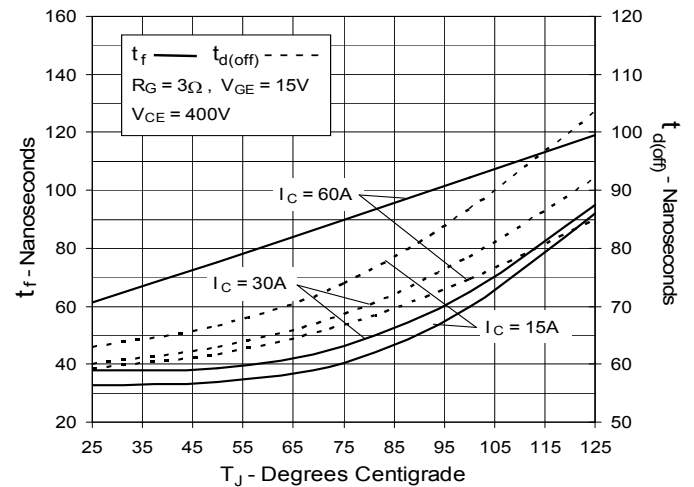
**Fig. 15. Inductive Turn-off
Switching Times vs. Gate Resistance**



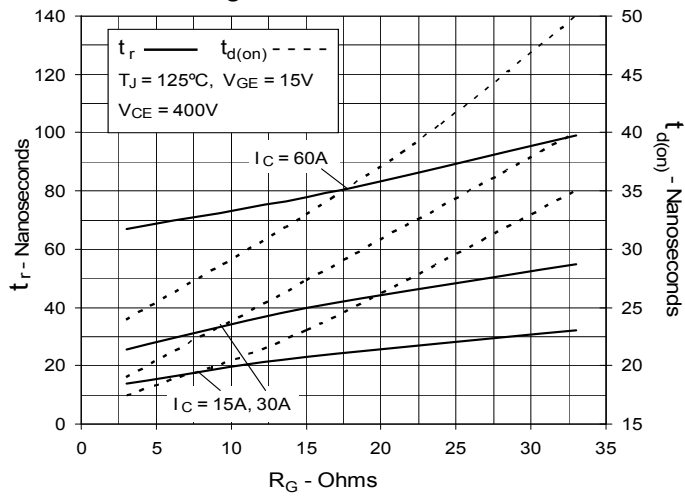
**Fig. 16. Inductive Turn-off
Switching Times vs. Collector Current**



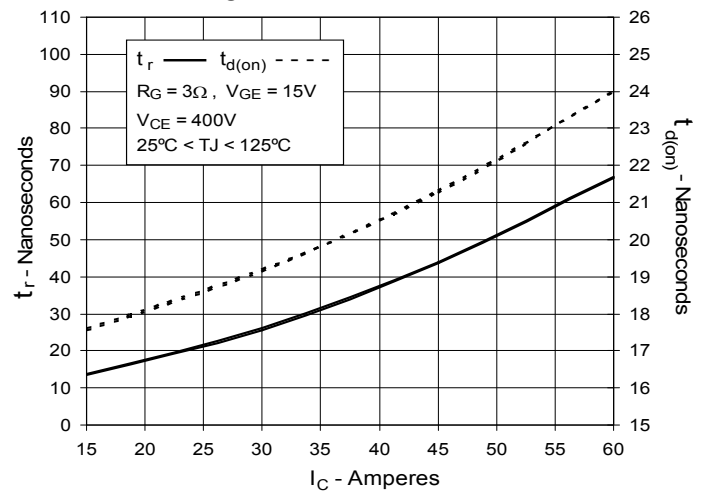
**Fig. 17. Inductive Turn-off
Switching Times vs. Junction Temperature**



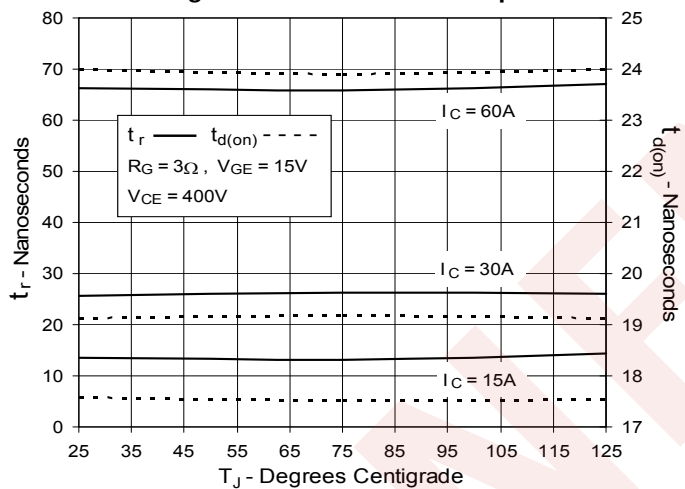
**Fig. 18. Inductive Turn-on
Switching Times vs. Gate Resistance**



**Fig. 19. Inductive Turn-on
Switching Times vs. Collector Current**



**Fig. 20. Inductive Turn-on
Switching Times vs. Junction Temperature**



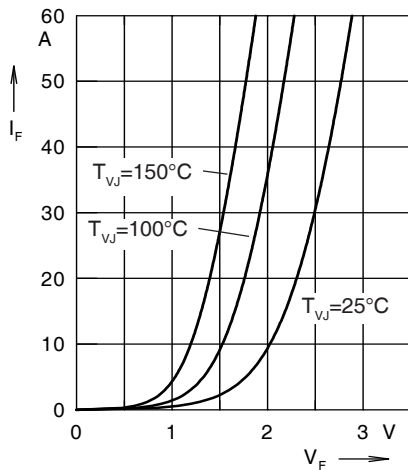
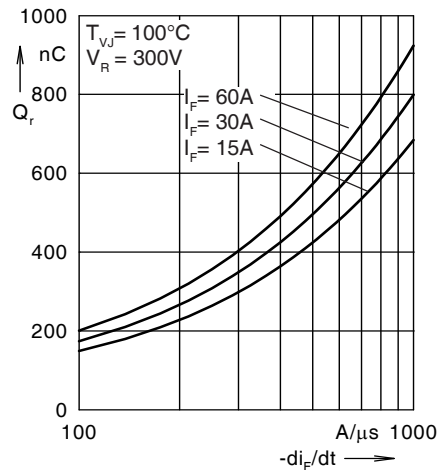
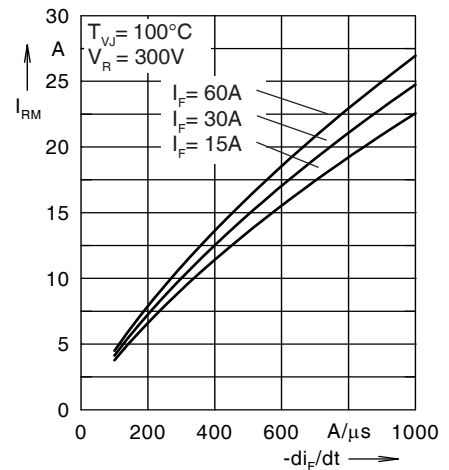
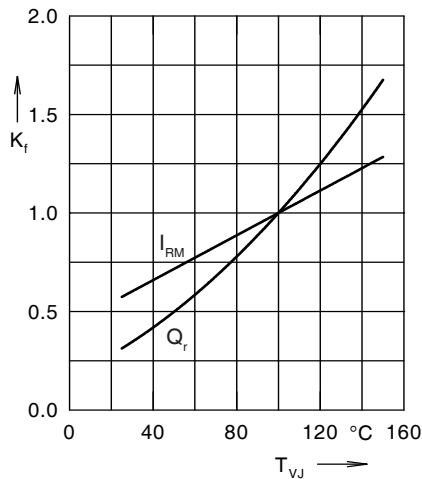
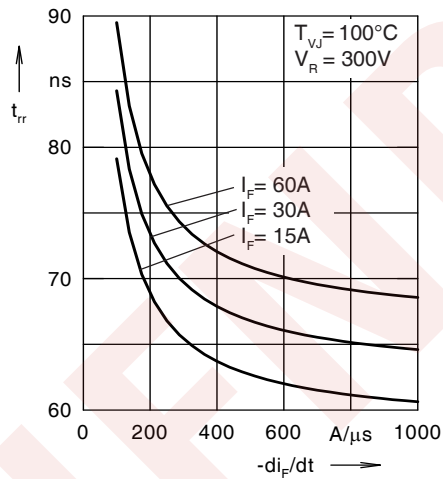
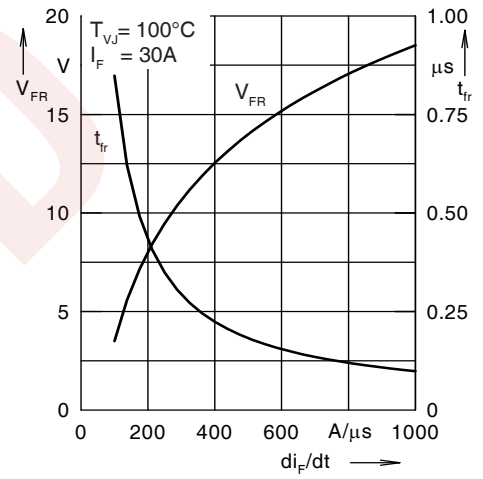
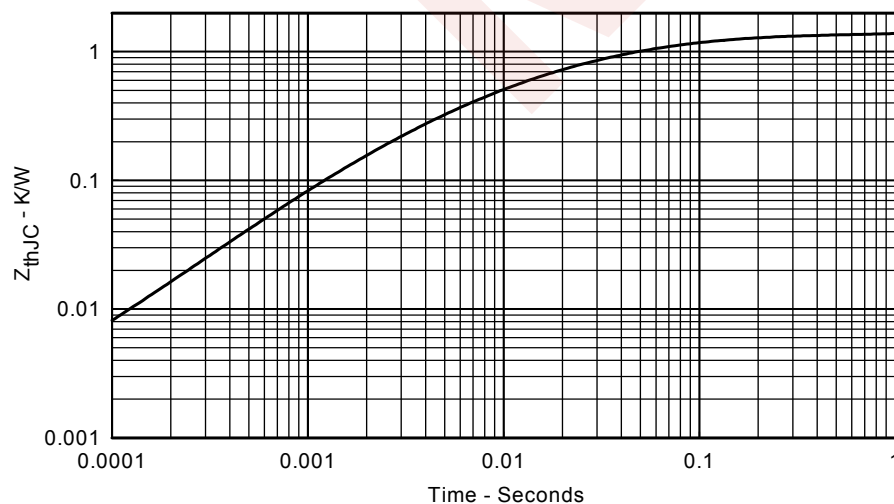
Fig. 21. Forward current I_F versus V_F Fig. 22. Reverse recovery charge Q_r versus $-di_F/dt$ Fig. 23. Peak reverse current I_{RM} versus $-di_F/dt$ Fig. 24. Dynamic parameters Q_r , I_{RM} versus T_{VJ} Fig. 25. Recovery time t_{rr} versus $-di_F/dt$ Fig. 26. Peak forward voltage V_{FR} and t_{fr} versus di_F/dt 

Fig. 27. Transient thermal resistance junction to case

NOT FOR NEW DESIGN

NEW



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