

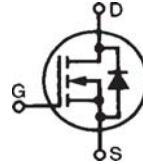
Polar3™ High Voltage Power MOSFET

IXTF6N200P3

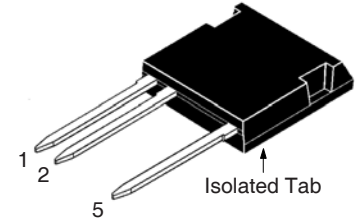
$$\begin{aligned} V_{DSS} &= 2000V \\ I_{D25} &= 4A \\ R_{DS(on)} &\leq 4.2\Omega \end{aligned}$$

(Electrically Isolated Tab)

N-Channel Enhancement Mode



ISOPLUS i4-Pak™



1 = Gate 5 = Drain
2 = Source

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C to } 150^\circ\text{C}$	2000	V
V_{DGR}	$T_J = 25^\circ\text{C to } 150^\circ\text{C}, R_{GS} = 1M\Omega$	2000	V
V_{GSS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_C = 25^\circ\text{C}$	4.0	A
I_{D110}	$T_C = 110^\circ\text{C}$	2.3	A
I_{DM}	$T_C = 25^\circ\text{C}$, Pulse Width Limited by T_{JM}	18.0	A
P_D	$T_C = 25^\circ\text{C}$	215	W
T_J		- 55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		- 55 ... +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ\text{C}$
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	$^\circ\text{C}$
F_C	Mounting Force	20..120 / 4.5..27	N/lb
V_{ISOL}	50/60Hz, 1 Minute	2500	V~
Weight		6	g

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 2500V~ Electrical Isolation
- High Blocking Voltage
- High Voltage Package

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- High Voltage Power Supplies
- Capacitor Discharge Applications
- Pulse Circuits
- Laser and X-Ray Generation Systems

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	2000		V
$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	3.0		5.0 V
I_{GSS}	$V_{GS} = \pm 20V, V_{DS} = 0V$			± 100 nA
I_{DSS}	$V_{DS} = 0.8 \cdot V_{DSS}, V_{GS} = 0V$ Note 2, $T_J = 100^\circ\text{C}$		150	25 μA
$R_{DS(on)}$	$V_{GS} = 10V, I_D = 3A$, Note 1			4.2 Ω

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 30\text{V}$, $I_D = 3\text{A}$, Note 1	4.5	7.5	S
C_{iss}	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$		3700	pF
C_{oss}			236	pF
C_{rss}			104	pF
R_{Gi}	Gate Input Resistance		2.5	Ω
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10\text{V}$, $V_{DS} = 500\text{V}$, $I_D = 3\text{A}$ $R_G = 2\Omega$ (External)		28	ns
t_r			22	ns
$t_{d(off)}$			80	ns
t_f			46	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 3\text{A}$		143	nC
Q_{gs}			21	nC
Q_{gd}			70	nC
R_{thJC}				0.58 $^\circ\text{C/W}$
R_{thCS}			0.15	$^\circ\text{C/W}$

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
I_S	$V_{GS} = 0\text{V}$			6 A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			24 A
V_{SD}	$I_F = I_S$, $V_{GS} = 0\text{V}$, Note 1			1.5 V
t_{rr}	$I_F = 3\text{A}$, $-di/dt = 100\text{A}/\mu\text{s}$ $V_R = 100\text{V}$, $V_{GS} = 0\text{V}$		520	ns
Q_{RM}			580	nC
I_{RM}			2.2	A

Notes:

1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.
2. Device must be heatsunk for high-temperature leakage current measurements to avoid thermal runaway.

ADVANCE TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

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IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338 B2
4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

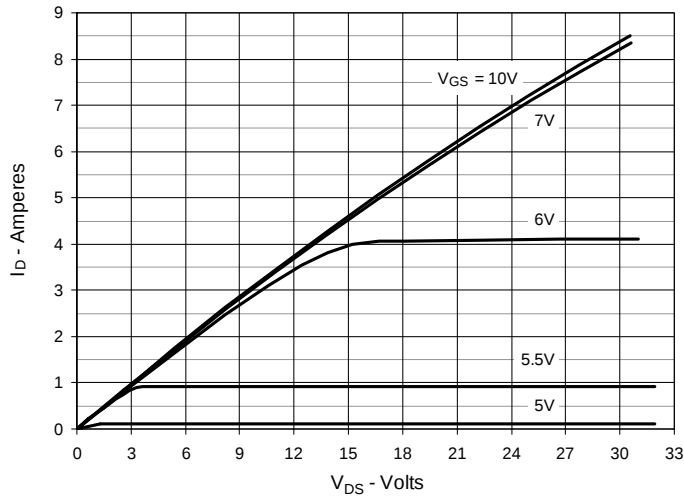
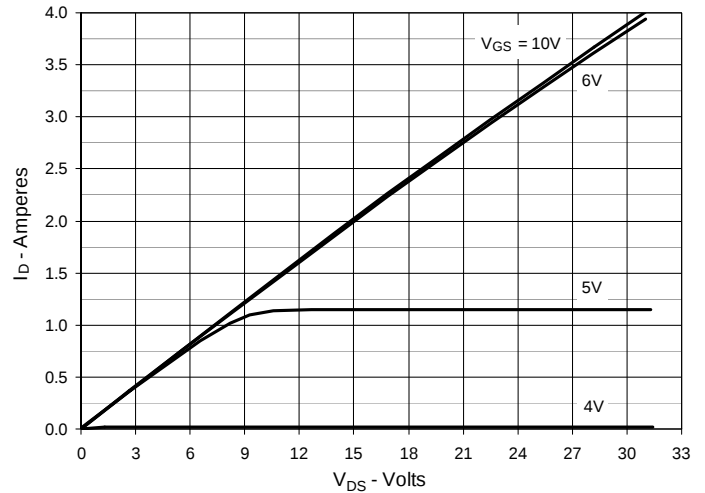
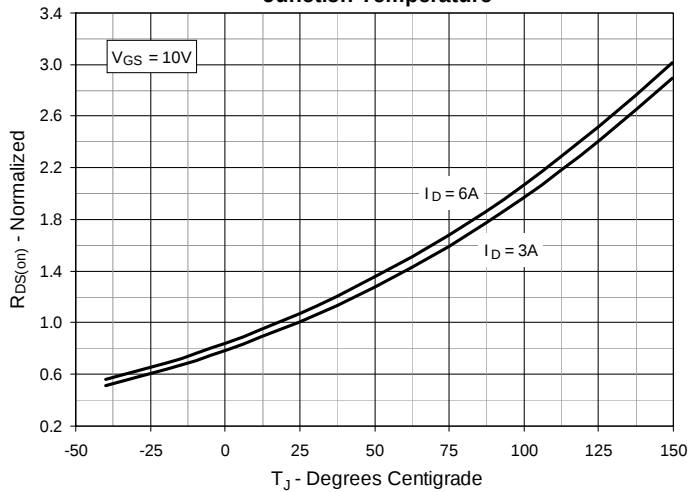
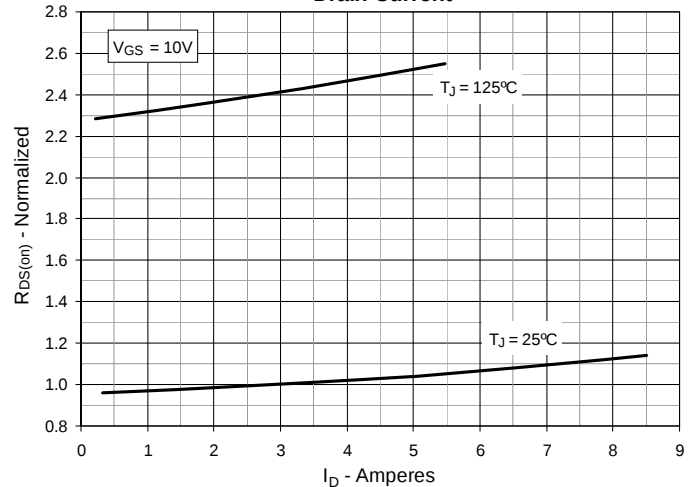
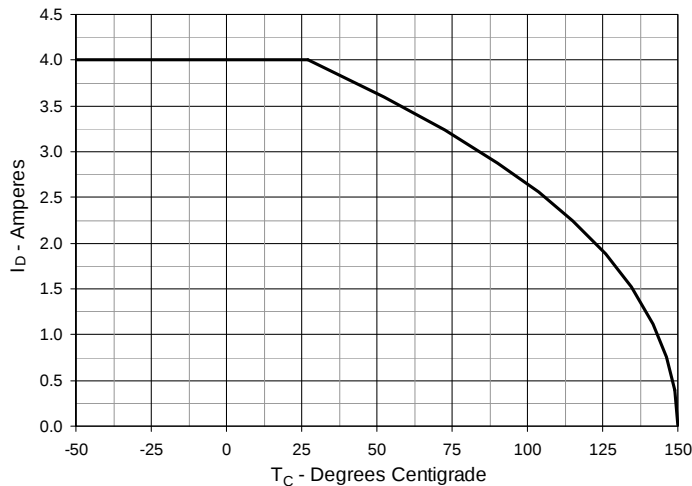
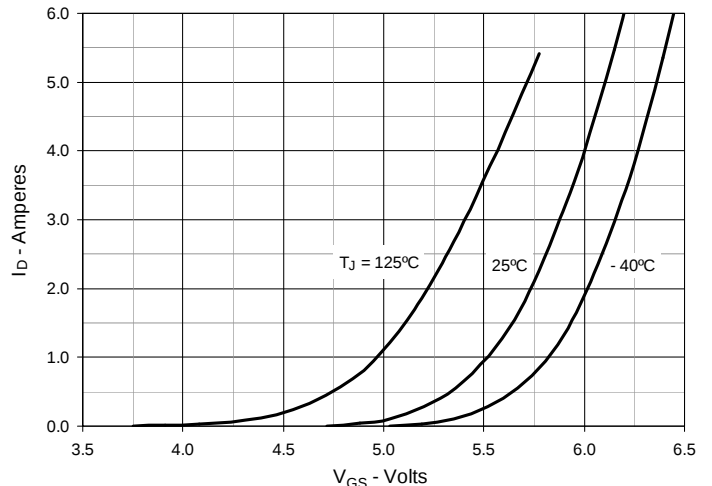
Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 2. Output Characteristics @ $T_J = 125^\circ\text{C}$

Fig. 3. $R_{DS(on)}$ Normalized to $I_D = 3\text{A}$ Value vs. Junction Temperature

Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 3\text{A}$ Value vs. Drain Current

Fig. 5. Maximum Drain Current vs. Case Temperature

Fig. 6. Input Admittance


Fig. 7. Transconductance

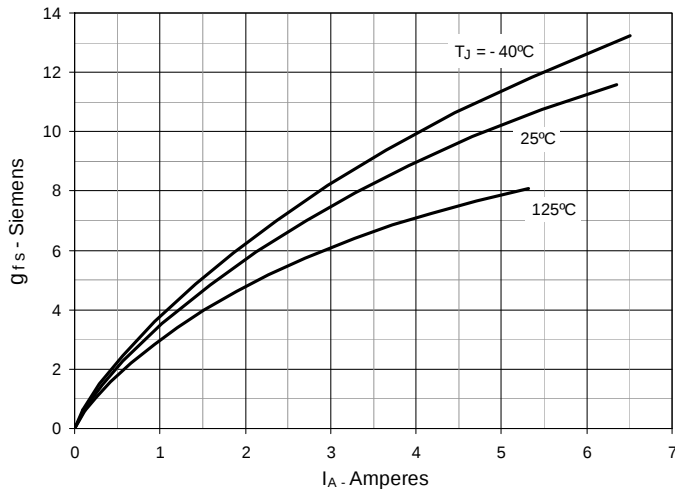


Fig. 8. Forward Voltage Drop of Intrinsic Diode

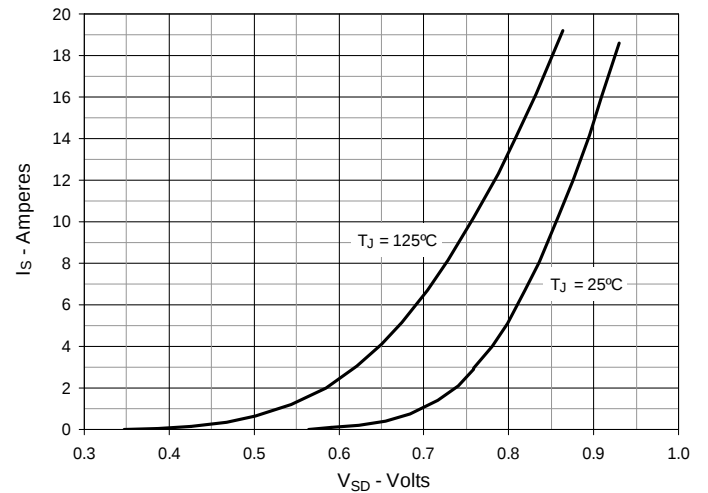


Fig. 9. Gate Charge

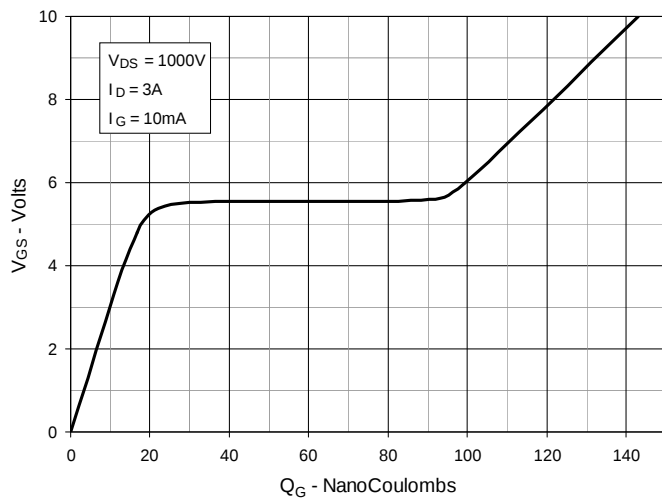


Fig. 10. Capacitance

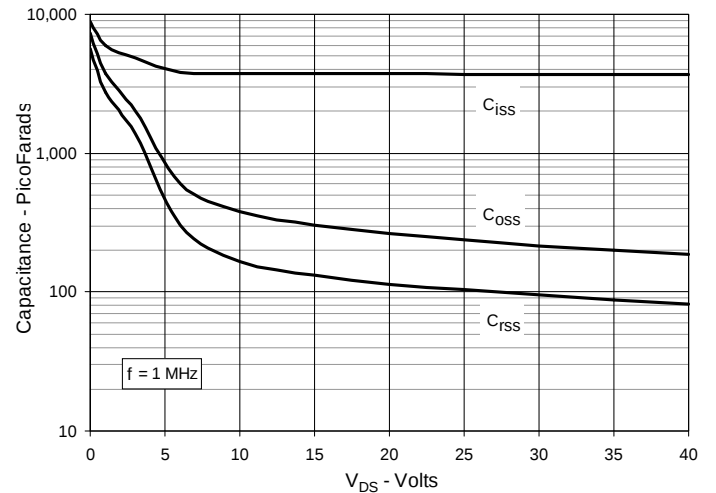


Fig. 11. Forward-Bias Safe Operating Area

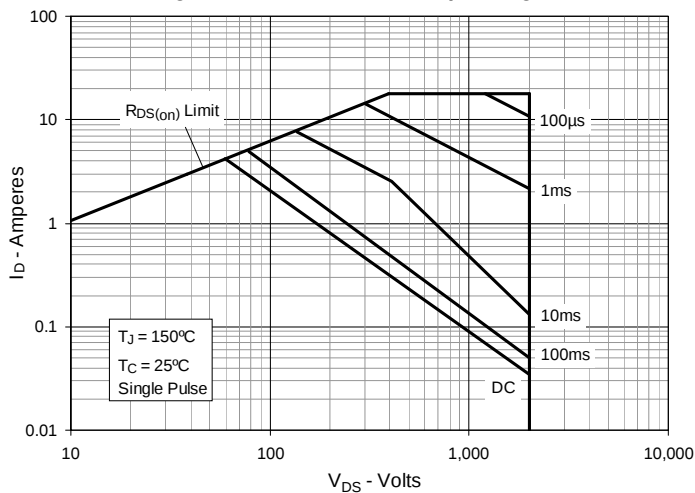
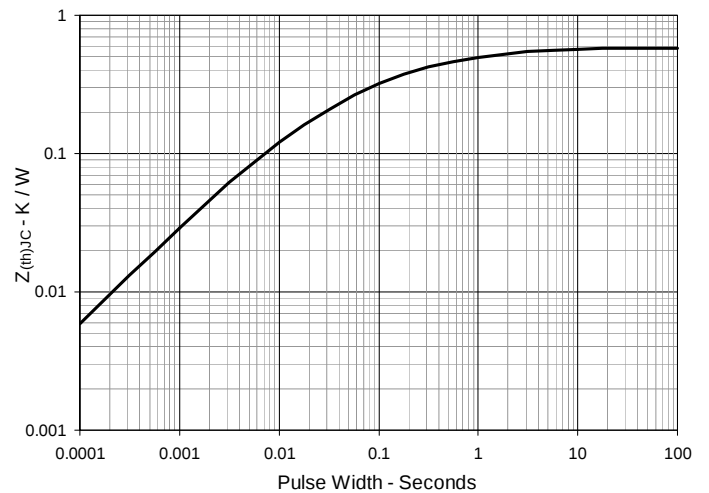
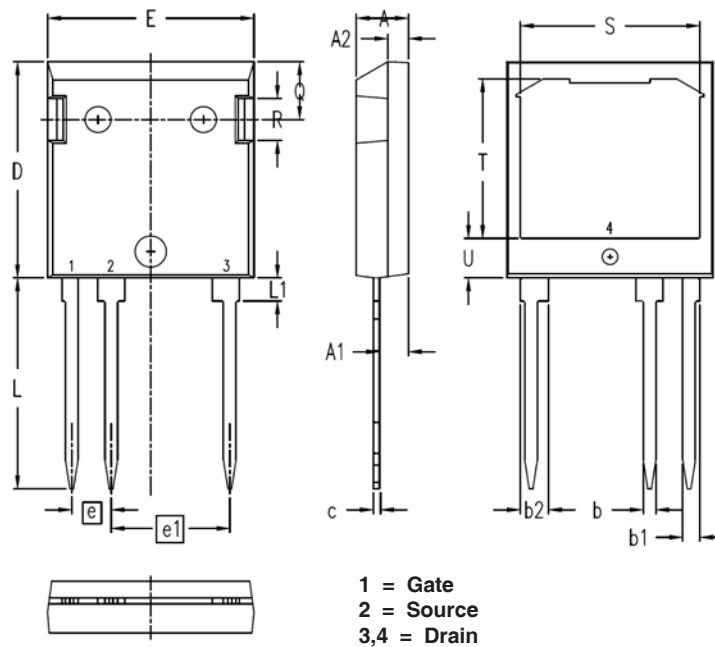


Fig. 12. Maximum Transient Thermal Impedance



ISOPLUS i4-Pak Outline


SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.193	.201	4.90	5.10
A1	.106	.114	2.70	2.90
A2	.075	.083	1.90	2.10
b	.047	.055	1.20	1.40
b1	.061	.069	1.55	1.75
b2	.087	.094	2.20	2.40
c	.020	.029	0.51	0.74
D	.819	.846	20.80	21.50
E	.768	.799	19.50	20.30
e	.150 BSC		3.81 BSC	
e1	.450 BSC		11.43 BSC	
L	.780	.838	19.80	21.30
L1	.083	.094	2.10	2.40
Q	.213	.236	5.40	6.00
R	.157	.169	4.00	4.30
S	.673	.685	17.10	17.40
T	.602	.614	15.30	15.60
U	.142	.154	3.60	3.90



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