

High Voltage Power MOSFET

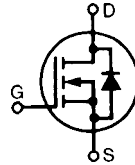
IXTQ3N150M

$$V_{DSS} = 1500V$$

$$I_{D25} = 3A$$

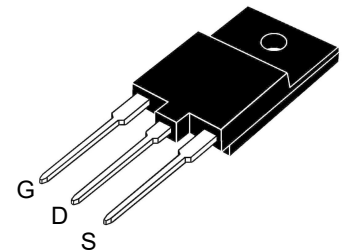
$$R_{DS(on)} \leq 7.3\Omega$$

N-Channel Enhancement Mode
Avalanche Rated
Fast Intrinsic Diode



**OVERMOLDED
(IXTQ...M)**

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C to } 150^\circ\text{C}$	1500	V
V_{DGR}	$T_J = 25^\circ\text{C to } 150^\circ\text{C}, R_{GS} = 1\text{ M}\Omega$	1500	V
V_{GSS}	Continuous	± 30	V
V_{GSM}	Transient	± 40	V
I_{D25}	$T_C = 25^\circ\text{C}, \text{ Limited by } T_{JM}$	3	A
I_{DM}	$T_C = 25^\circ\text{C}, \text{ Pulse Width Limited by } T_{JM}$	9	A
I_A	$T_C = 25^\circ\text{C}$	3	A
E_{AS}	$T_C = 25^\circ\text{C}$	250	mJ
dv/dt	$I_S \leq I_{DM}, V_{DD} \leq V_{DSS}, T_J = 150^\circ\text{C}$	5	V/ns
P_D	$T_C = 25^\circ\text{C}$	73	W
T_J		- 55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		- 55 ... +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering 1.6 mm (0.062 in.) from Case for 10s	300	$^\circ\text{C}$
M_d	Mounting Torque	1.13/10	Nm/lb.in.
Weight		6	g



G = Gate D = Drain
S = Source

Features

- Plastic Overmolded Tab for Electrical Isolation
- Avalanche Rated
- Fast Intrinsic Diode
- Low Package Inductance

Advantages

- High Power Density
- Easy to Mount
- Space Savings

Applications

- High Voltage Power Supplies
- Capacitor Discharge Applications
- Pulse Circuits

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu\text{A}$	1500		V
$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	2.5		5.0 V
I_{GSS}	$V_{GS} = \pm 30V, V_{DS} = 0V$			± 100 nA
I_{DSS}	$V_{DS} = V_{DSS}, V_{GS} = 0V$ $T_J = 125^\circ\text{C}$			10 μA 250 μA
$R_{DS(on)}$	$V_{GS} = 10V, I_D = 1.5A, \text{ Note 1}$			7.3 Ω

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 20\text{V}$, $I_D = 1.5\text{A}$, Note 1	2.2	3.6	S
C_{iss}	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$		1375	pF
C_{oss}			90	pF
C_{rss}			30	pF
R_{GI}	Gate Input Resistance		3.0	Ω
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 1.5\text{A}$ $R_G = 5\Omega$ (External)		19	ns
t_r			21	ns
$t_{d(off)}$			42	ns
t_f			25	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 1.5\text{A}$		38.6	nC
Q_{gs}			6.5	nC
Q_{gd}			19.0	nC
R_{thJC}				1.7 $^\circ\text{C/W}$
R_{thCS}		0.21		$^\circ\text{C/W}$

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
I_S	$V_{GS} = 0\text{V}$, Note 1			3 A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			12 A
V_{SD}	$I_F = I_S$, $V_{GS} = 0\text{V}$, Note 1			1.3 V
t_{rr}	$I_F = 1.5\text{A}$, $-di/dt = 100\text{A}/\mu\text{s}$ $V_R = 100\text{V}$		0.9	μs
Q_{RM}			6.7	μC
I_{RM}			15	A

Note 1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

Littelfuse reserves the right to change limits, test conditions, and dimensions.

LF MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
	4,860,072	5,017,508	5,063,307	5,381,025	6,259,123B1	6,534,343	6,710,405B2	6,759,692	7,063,975B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

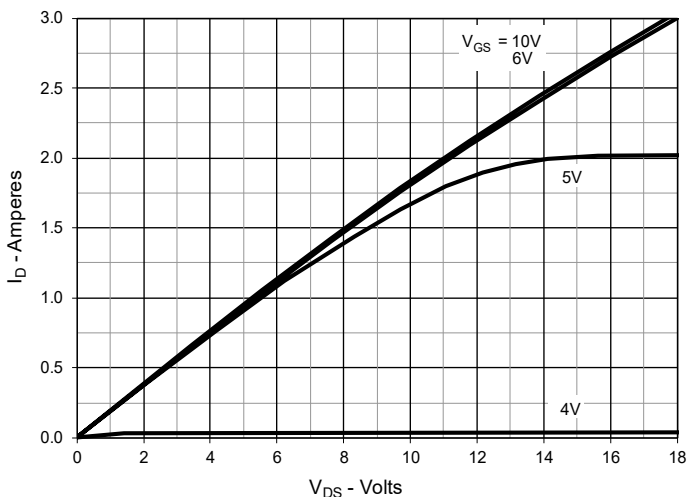


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

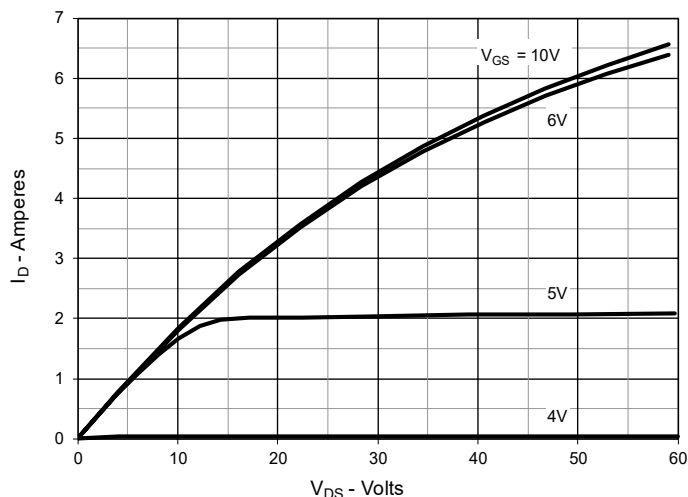


Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

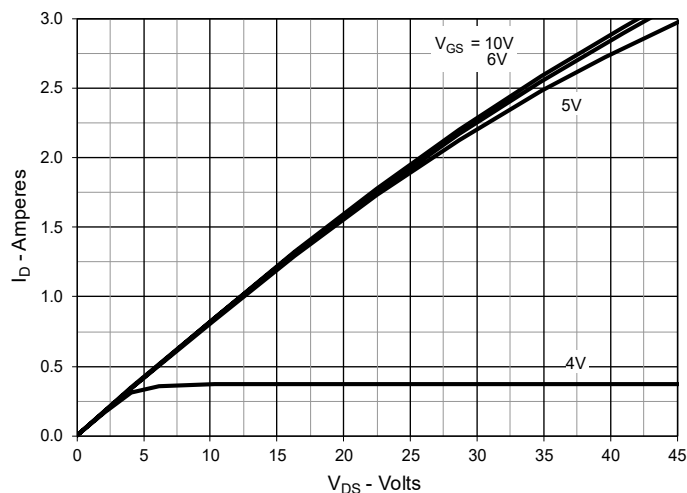


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 1.5\text{A}$ Value vs. Junction Temperature

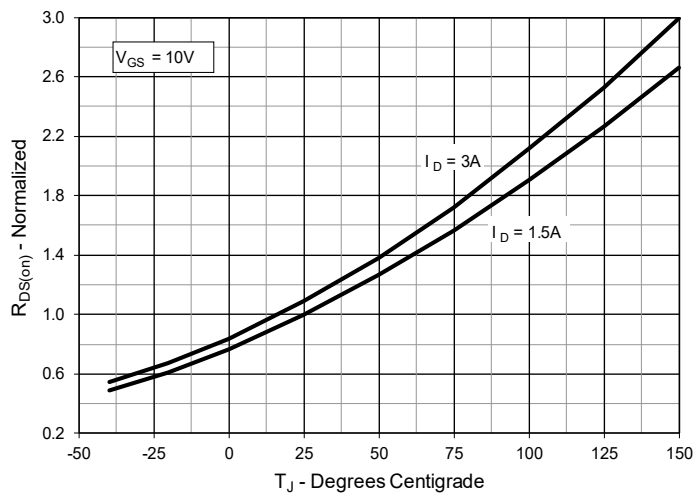


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 1.5\text{A}$ Value vs. Drain Current

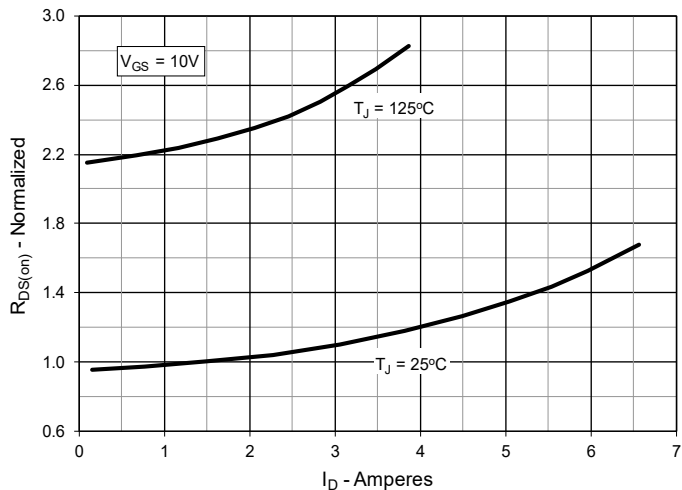


Fig. 6. Input Admittance

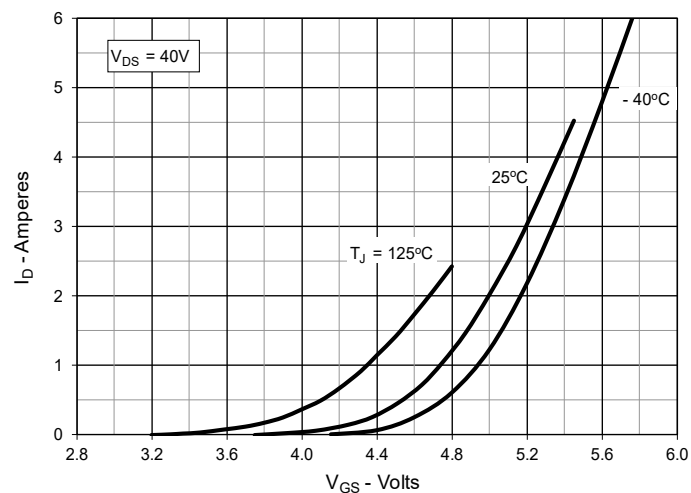


Fig. 7. Transconductance

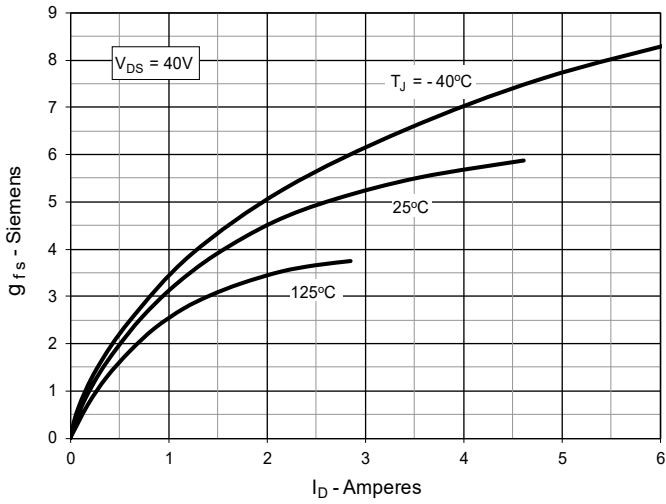


Fig. 8. Forward Voltage Drop of Intrinsic Diode

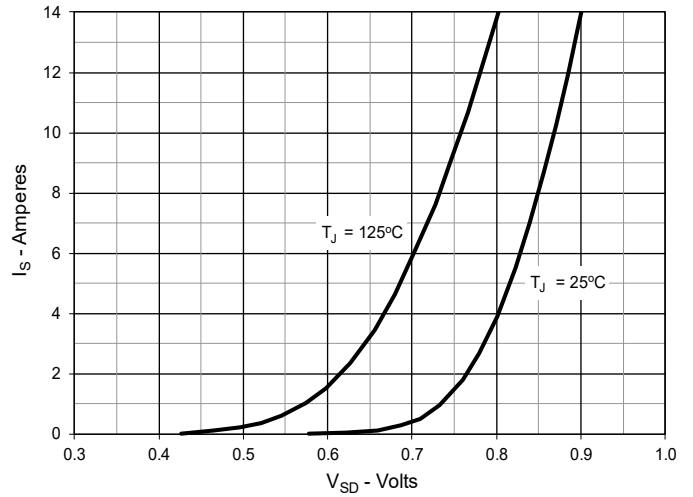


Fig. 9. Gate Charge

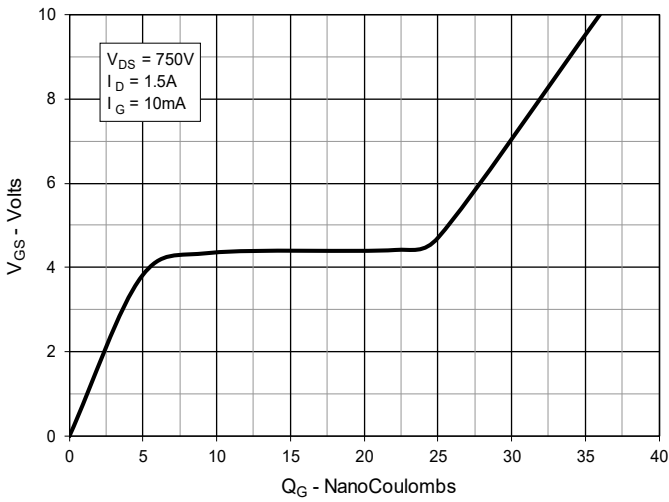


Fig. 10. Capacitance

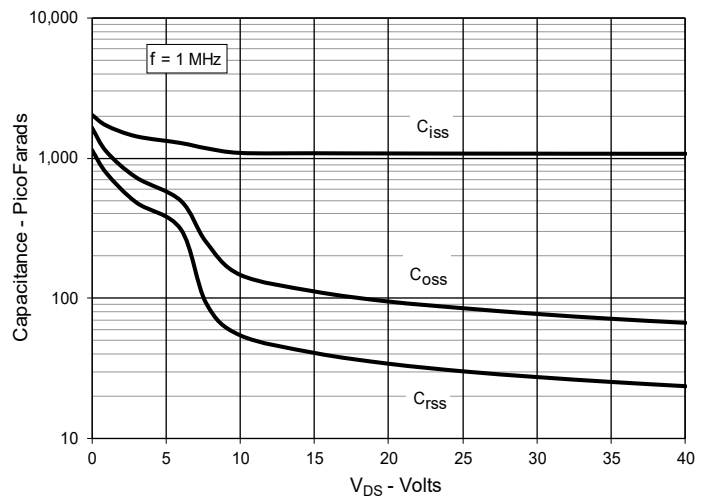
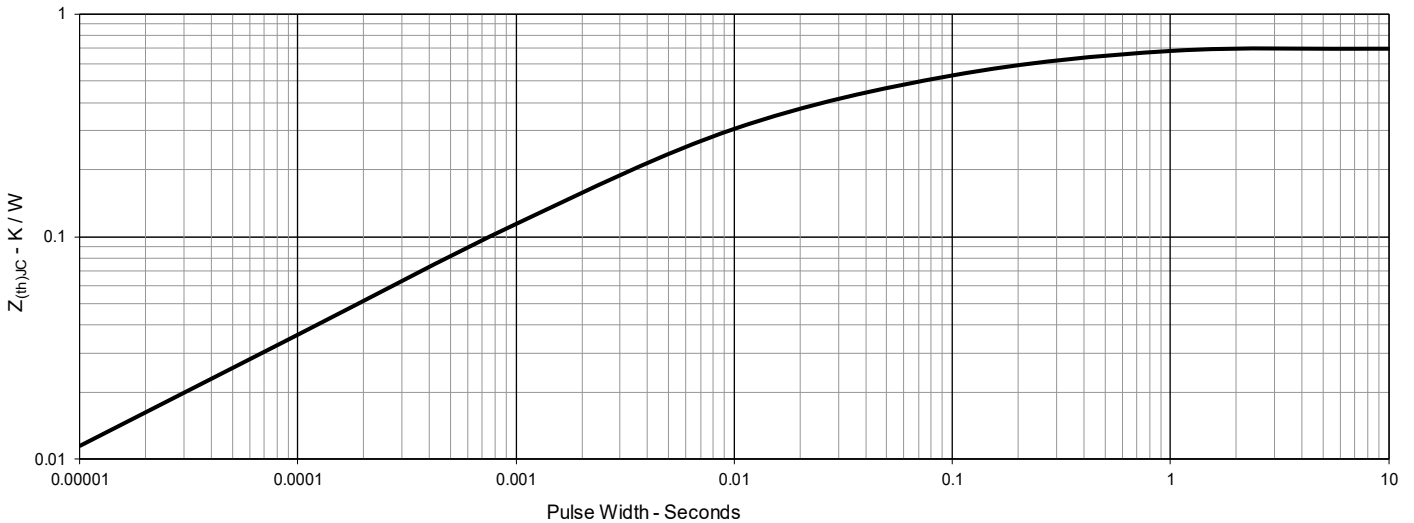
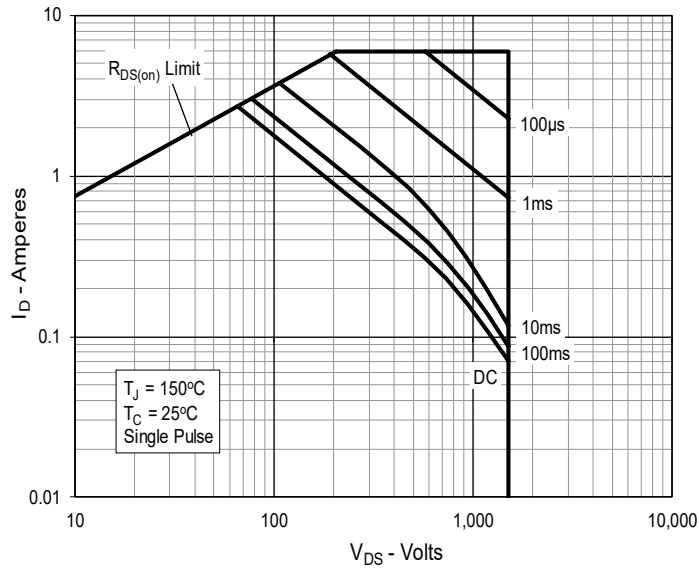


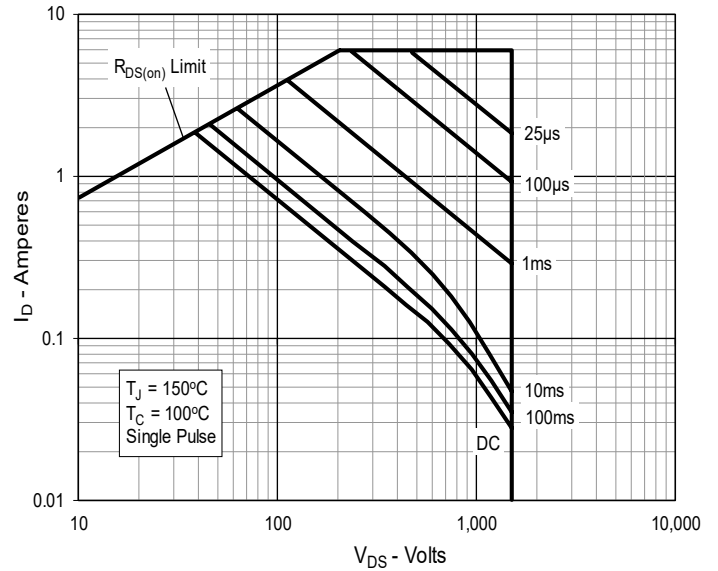
Fig. 12. Maximum Transient Thermal Impedance

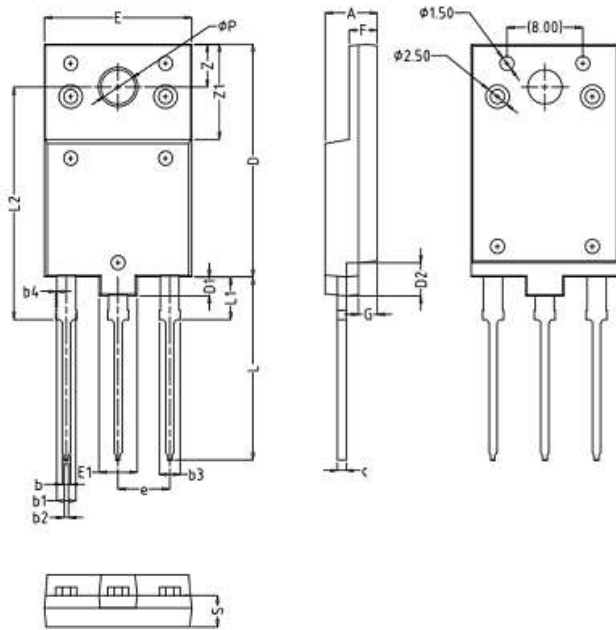


**Fig. 12. Forward-Bias Safe Operating Area
@ $T_C = 25^\circ\text{C}$**



**Fig. 13. Forward-Bias Safe Operating Area
@ $T_C = 100^\circ\text{C}$**



TO-3FPF Outline


SYMBOL	MIN	MAX
A	5.30	5.70
b	0.65	0.95
b1	1.81	2.19
b2	0.30	0.70
b3	1.81	2.40
b4	-	0.20
c	0.80	1.00
D	24.20	24.80
D1	1.80	2.20
D2	3.30	3.70
E	15.30	15.70
E1	3.80	4.20
F	2.80	3.20
e	5.45 BSC	
L	19.00	19.60
L1	4.20	4.80
L2	24.20	24.80
P	3.40	3.80
Z	4.30	4.70
Z1	9.70	10.30
G	1.80	2.20
S	3.10	3.50