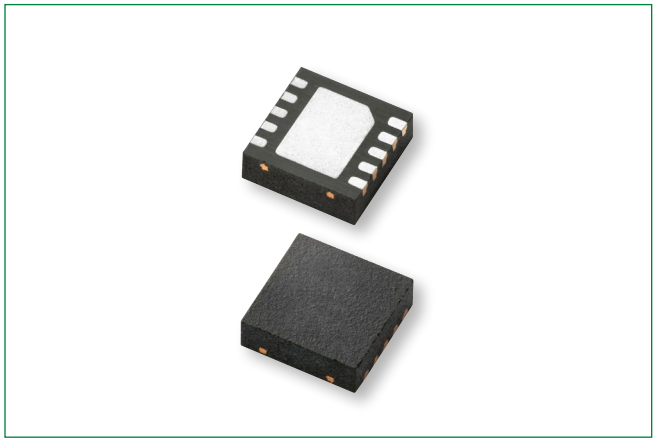
LS12052BD33

18V, 5A eFuse with Over-Voltage Protection and Blocking FET Control

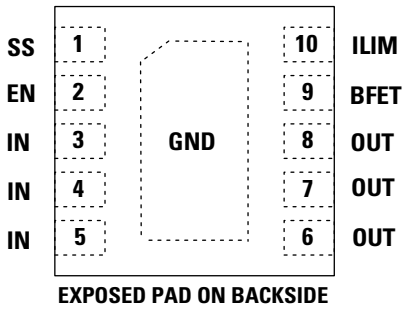
HF RoHS Pb



Web Resources

Download ECAD models, order samples, and find technical recources at www.littelfuse.com

Pinout Designation



Pin Description

Pin #	Pin Name	Description
3,4,5	IN	Power input pin.
9	BFET	External NFET gate driver. Control an external NFET which can be connected "Back to Back" with the LS12052BD33 output to prevent current flowing from the load to the source. Float this pin if it is not used.
10	ILIM	Current limit program pin. Program the current limit by connecting a resister to ground.
1	SS	Soft Start time program pin. Connect a capacitor to ground to program the soft start time.
2	EN	Enable interface pin. EN has accurate ON/OFF threshold of 1.29V and 1.19V respectively. Pull it above ON threshold to enable the IC. Pull it below OFF threshold to disable the IC.
6,7, 8	OUT	Power output pin.
EP	GND	Ground pin.

Description

The LS12052BD33 family of integrated load switches provides an easy circuit protection to power the system. The device uses few external components and provides multiple protection modes. They are a robust defense against overload, short circuit, input voltage surge, excessive inrush current and reverse current blocking with an external NFET. The switch's low $R_{DS(ON)}$ helps to reduce power loss during normal operation. Current limit level can be set with a single external resistor. Input over voltage events are protected by internal clamp circuitry to a safe output voltage. Programmable soft-start controls the slew rate of the output voltage to limit inrush current during plug in. It integrates thermal fold-back function and over temperature shutdown protection. The BFET pin is provided to drive an external NFET which can be connected "Back to Back" with the LS12052BD33 output. The external NFET gate is driven by BFET to prevent current flow from the load to the source. LS12052BD33 is available in small DFN 3mm x 3mm-10 package.

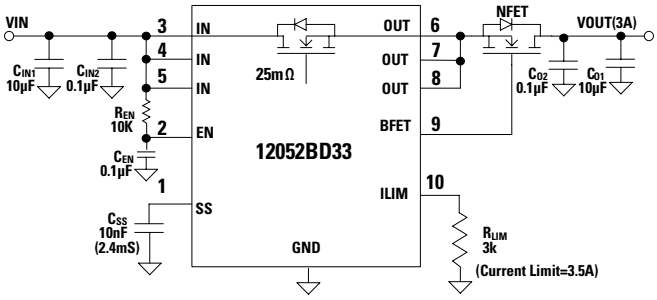
Features and Benefits

- Wide Input Voltage Range from 2.7V to 18V
- Extremely Low $R_{DS(ON)}$ for the Integrated Protection Switch: 25mΩ
- External Programmable Soft-Start Time
- External Programmable Current Limit
- Support Reverse Current Blocking
- Short-circuit Protection
- Fixed Over-voltage 14.4V Output Voltage Clamp
- Accurate 1.29V EN Pin Turn-on Threshold
- Thermal Shutdown Protection& Auto Recovery
- DFN3×3_10L Packages
- Pb-Free and RoHS Compliant

Applications

- HDD and SSD Drives
- Adapter Powered Devices
- Notebook PC
- PCI, PCIe Cards
- Industry

Typical Applications



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18V, 5A eFuse with Over-Voltage Protection and Blocking FET Control

Absolute Maximum Rating (Reference to GND)

Symbol	Value	Units
V_{IN}	-0.3 to +20	V
BFET	-0.3 to V_{IN}+6	V
EN	-0.3 to +20	V
The other Pins	-0.3 to +6.5	V
Junction Temperature Range	-40 to +150	°C
Storage Temperature Range	-65 to +150	°C
ESD, Human Body Model (HBM)	±2000	V
Lead Temperature (Soldering 10s)	260	°C

Notes: Stress exceeding those listed "Absolute Maximum Ratings" may damage the device.

Recommend Operating Conditions

Symbol	Value	Units
Input Voltage (V_{IN})	+2.7 to +18	V
Junction Temperature Range	+125	°C

Note: The device is not guaranteed to function outside of the recommended operating conditions.

Thermal information

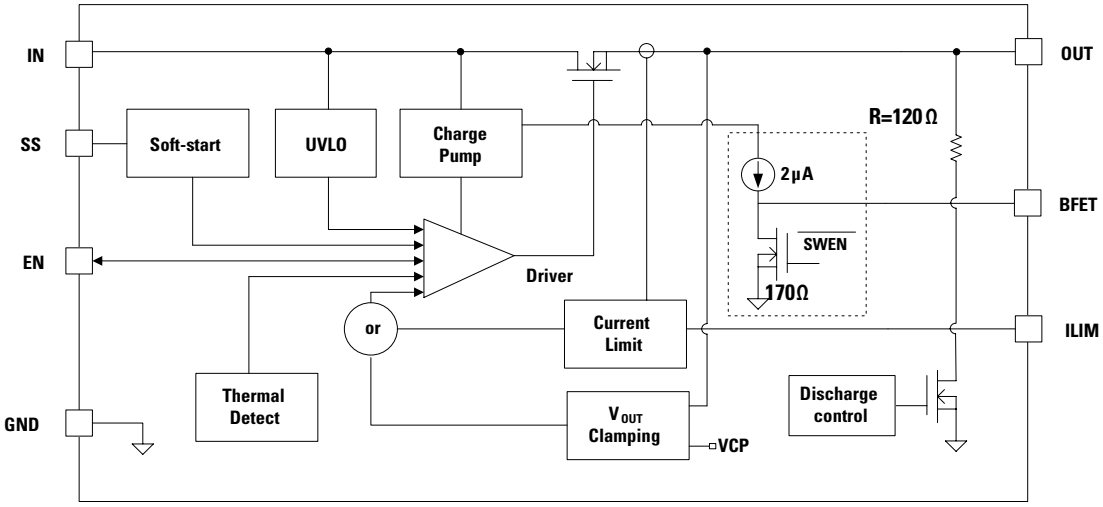
Symbol	Value	Units
Maximum Power Dissipation (T_A=25°C)	2.6	W
Thermal Resistance (θ_{JA})	38	°C/W
Thermal Resistance (θ_{JC})	8	°C/W

Notes:

1. Measured on JESD51-7, 4-Layer PCB.

2. The maximum allowable power dissipation is a function of the maximum junction temperature T_{J_MAX}, the junction to ambient thermal resistance θ_{JA}, and the ambient temperature TA. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_{D_MAX}=(T_{J_MAX}-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

Functional Block Diagram



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18V, 5A eFuse with Over-Voltage Protection and Blocking FET Control

Electrical Characteristics (T_A = +25°C, V_{IN}=12V, R_{LIM}=10kΩ, C_{SS}=100nF, C_{IN}=10µF, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range		2.7		18	V
I_{BIAS}	Quiescent Current			250	280	µA
I_{SHDN}	Shutdown Current	V_{EN}=0V		10	13	µA
V_{ENR}	EN Turn-on Threshold	EN Rising	1.24	1.29	1.34	V
V_{ENF}	EN Turn-off Threshold	EN Falling	1.14	1.19	1.24	V
V_{ENHYS}	EN Hysteresis			100		mV
I_{EN}	EN Input Leakage Current	0V ≤ V_{EN} ≤ 5V	-200		200	nA
R_{OUTdis}	Output Discharging Resistance	V_{EN}=0V		120		Ω
V_{CLP}	Clamping Output Voltage		13.8	14.4	15.0	V
V_{UVLO}	Input UVLO Threshold	V_{IN} Rising	3.4	3.6	3.8	V
V_{HYS}	UVLO hysteresis	V_{IN} Falling		300		mV
R_{DSON}	Protection FET RON			25		mΩ
I_{INLIM}	Current Limit Program Range		1		5	A
I_{INLIM}	Current Limit	R_{LIM}=10kΩ	0.74	1.05	1.36	A
K_{LIM}	Current Limit Setting Factor	I_{INLIM}=1A~5A	7.4	10.5	13.6	A*kΩ
T_{SS}	Soft-start Time	C_{SS}=100nF	20	29	38	msec
		SS float	1.2	1.7	2.2	msec
I_{BFET}	BFET Charging current	V_{BFET}=V_{OUT}		2		µA
V_{BFET}	BFET Regulation Voltage			V_{IN}+4V		V
	BFET Clamp Voltage			V_{OUT}+7.5V		V
$R_{BFETdis}$	BFET Discharging Resistor	V_{EN}=0V		170		Ω
T_{SD}	Thermal Shutdown Temperature			140		°C
T_{HYS}	Thermal Shutdown Hysteresis			20		°C
T_{LIIM}	Junction Temperature Regulation			125		°C

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18V, 5A eFuse with Over-Voltage Protection and Blocking FET Control

Typical Performance Characteristics (C_{IN}=10µF, C_{OUT}=10µF, C_{SS}=10nF, T_A=+25°C)

Figure 1. Current Limit Vs Rlimit

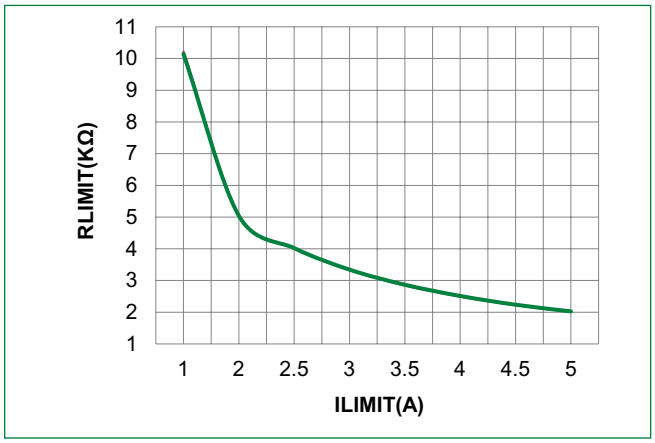


Figure 2. Programmable Current Limit (RLIM=3.3K)

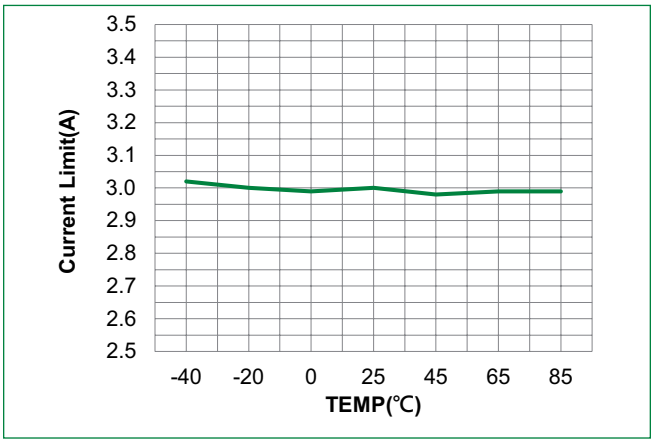


Figure 3. Vin Power On

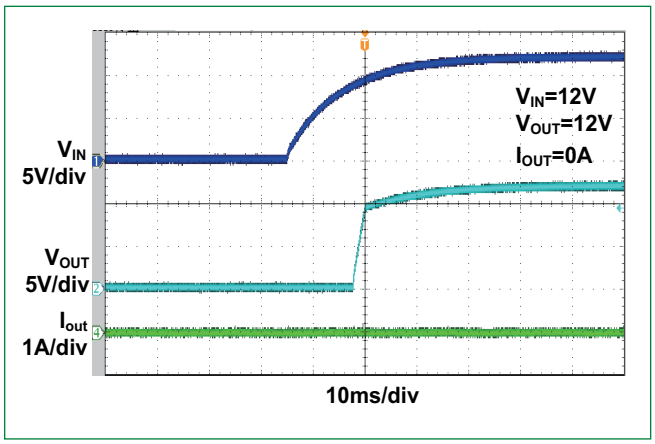
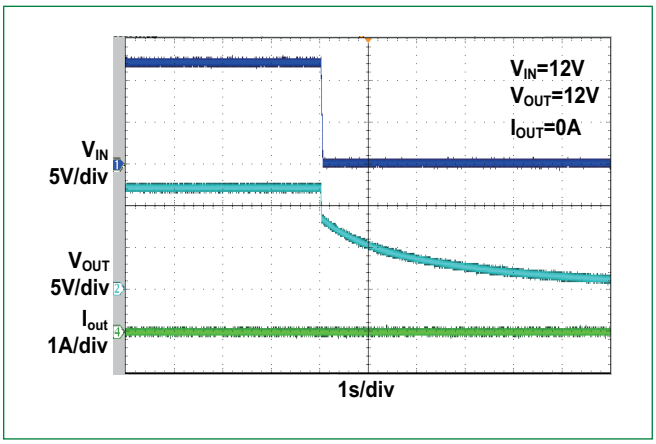
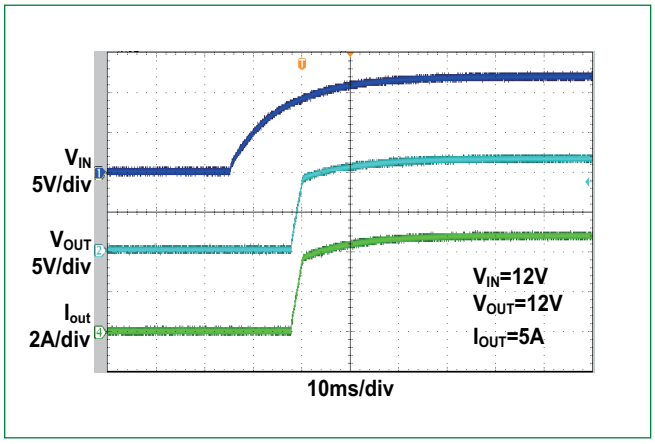


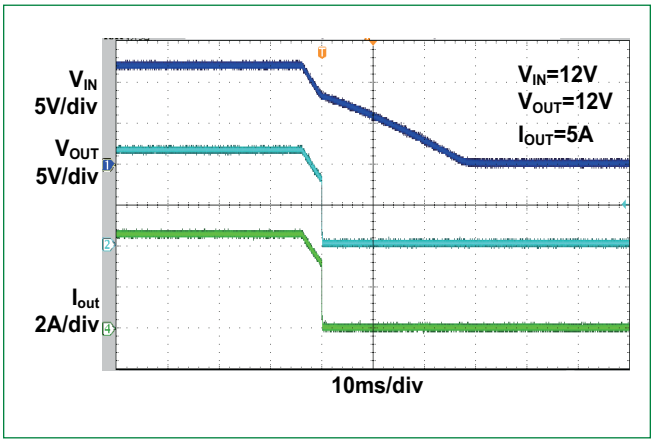
Figure 4. Vin Power Off



Vin Power On



Vin Power Off



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Figure 5. EN Power On

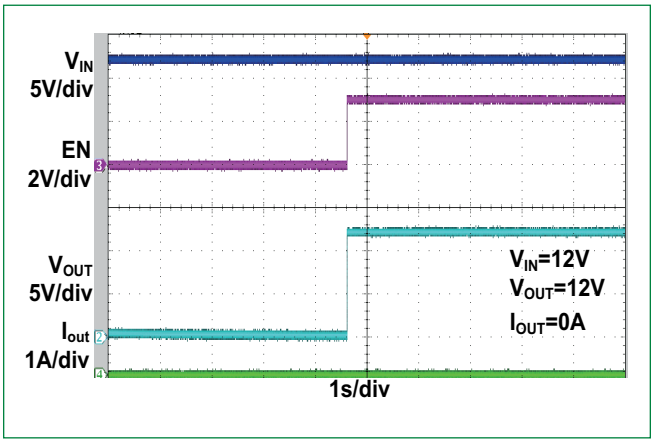


Figure 6. EN Power Off

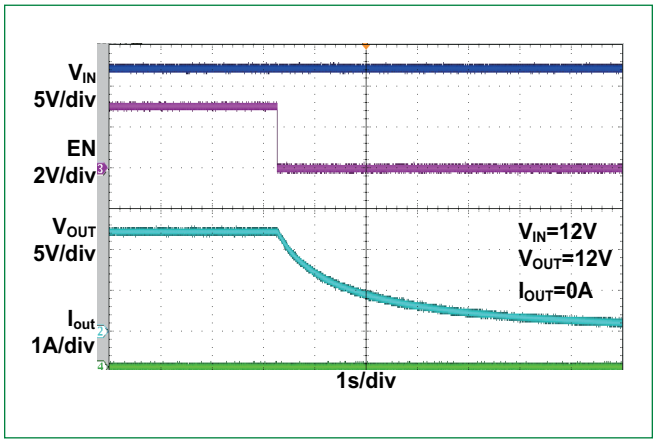


Figure 7. EN Power On

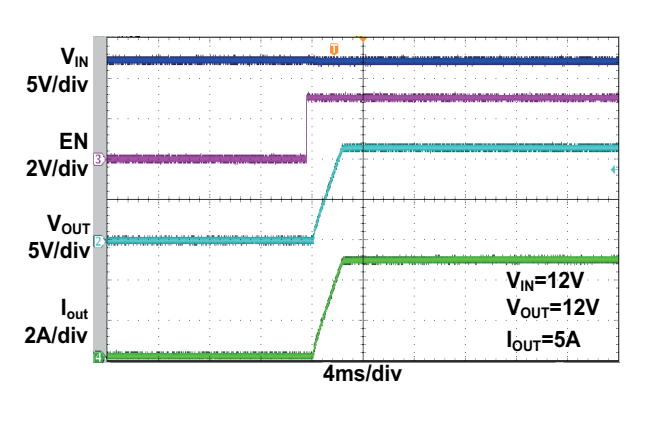


Figure 8. EN Power Off

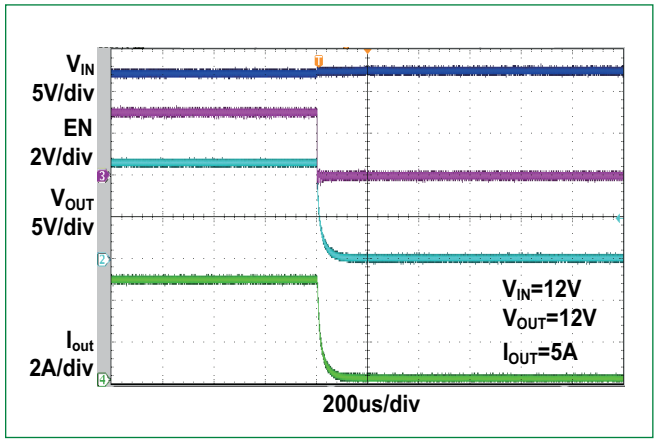
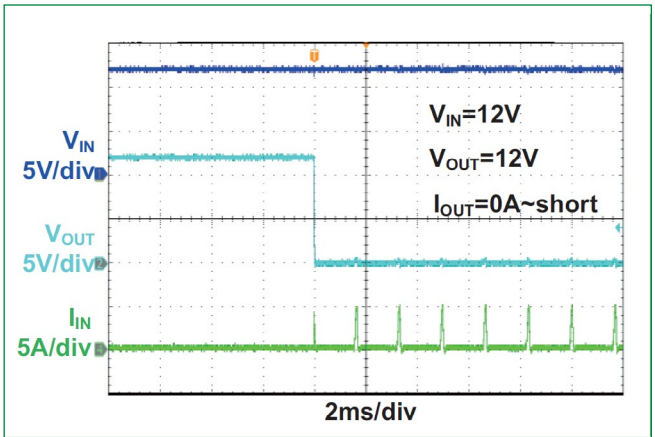


Figure 8. Short Protection



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Figure 9. Soft Start Time

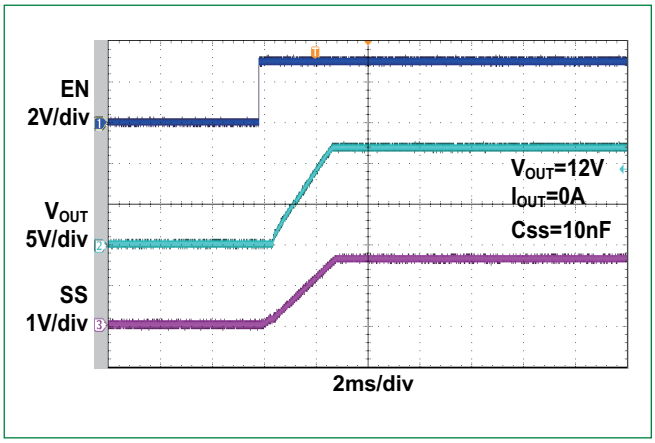


Figure 10. Soft Start Time

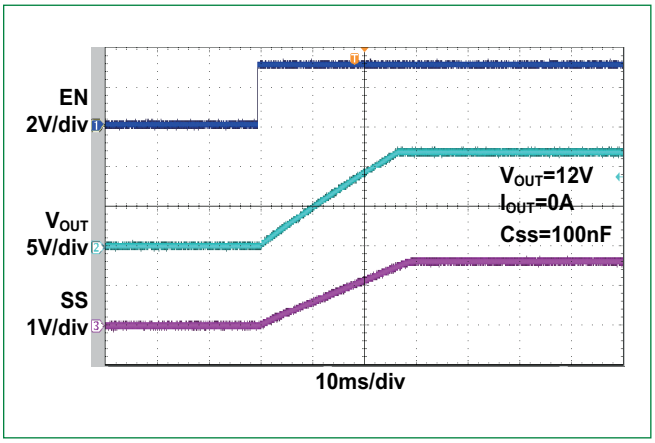


Figure 11. Turnoff Delay to BFET

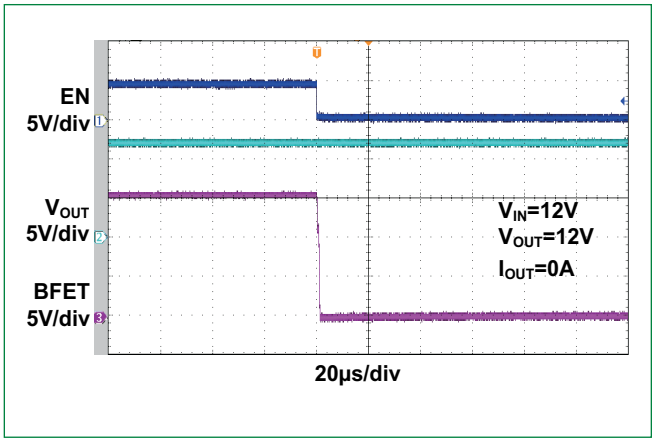
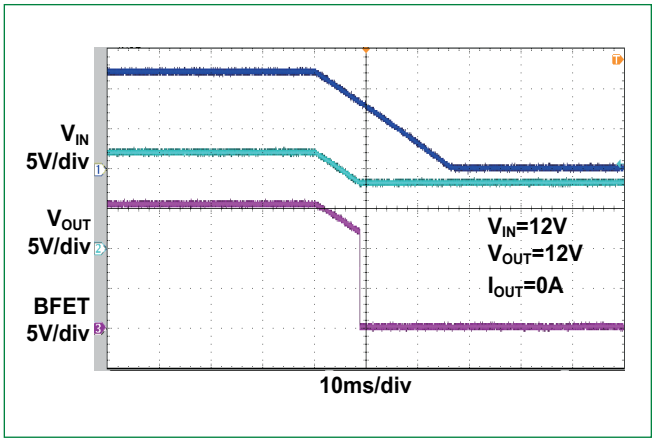


Figure 12. Turnoff Delay to BFET



Detailed Description

The LS12052BD33 is a current limit load switch with integrated power switch that is used to manage current/voltage/start-up voltage ramp to the connected load. A high level on EN pin enables the internal MOSFET. As VIN rises, the internal MOSFET of the device will start conducting and allow current to flow from IN to OUT. When EN is held low, internal MOSFET is turned off. User also has the ability to control the output voltage ramp time by connecting a program capacitor between SS pin and GND. After a successful start-up sequence, the device will actively monitors its load current and input voltage, ensuring that the overload current limit I_{LIMT} programmed by pin I_{LIMT} is not exceeded. It also monitor input voltage and ensures any spikes are safely clamped to pre-determined level at the output. This keeps the output device safe from harmful voltage and current transients. The device also has built-in thermal sensor. In the event device temperature (T_J) exceeds thermal regulation point, current limit will be decreased until the die junction temperature T_J is regulated at T_{LIM} 125°C. When device temperature (T_J) exceeds T_{SD}, typically 140°C, the thermal shutdown circuitry will shut down the internal MOSFET thereby disconnecting the load from the supply. The LS12052BD33 device will remain off during a cooling period until device temperature falls below T_{SD}-20°C, after which it will attempt to restart.

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LS12052BD33

18V, 5A eFuse with Over-Voltage Protection and Blocking FET Control

Application Information

Input and Output Capacitor Selection

Recommend to bypass IN and OUT to GND with 10µF ceramic capacitor for the most application. X7R type ceramic capacitors are recommended.

Enable and External Programmable Input UVLO

Enable interface pin EN has accurate ON/OFF threshold of 1.29V and 1.19V respectively. An external resistor divider connected from IN to GND can set the VIN under-voltage lockout threshold for load switch operation. EN controls both the ON/OFF state of the internal MOSFET and the external blocking FET. Set EN voltage above ON threshold to enable the internal MOSFET and charge up the gate voltage BFET of external FET. Pull EN below OFF threshold to turn off the internal MOSFET and pull down the gate of the external FET, and Output V_{OUT} will be discharged to GND through the internal120Ω discharging resistor.

Soft Start

Connect a program capacitor from this pin to GND to control the slew rate of the output voltage at power-on. This pin can be left floating to obtain a predetermined slew rate (minimum T_{SS}) on the output. The soft start time with different capacitor is below:

$$T_{SS} = \begin{cases} T_{SS_{INT}}, \text{No external } C_{SS} \\ \frac{C_{SS}}{I_{INT}}, T_{SS} > T_{SS_{INT}} \end{cases}$$

SS cap (nF)	None	10	55	100
Rise time (msec)	1.7	2.4	14	29

Where, T_{SS_INT} is the internally default soft-start time (typical 1.7ms) without an external C_{SS}, and I_{INT} is the internal current source, about 3.6µA.

Output Clamp voltage

LS12052BD33 Output clamp voltage is clamped to 14.4V during the input over-voltage fault event.

Part Number	V_{IN}		Clamping Threshold		
			Min	Typ	Max
LS12052BD33	12V	>15V	13.8V	14.4V	15.0V

Input Current Limit

For current limited adaptor or sources, user can program the input current limit level to prevent the load current overload the source. When the input current limit loop is engaged, input current will be automatically reduced to the programmed level to satisfy the limited input power.

Input current limit can be programmed with below equation:

$$I_{INLIM} = \frac{10.5A * k\Omega}{R_{ILIM}}$$

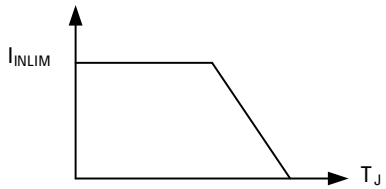
Where R_{LIM} is the program resistor at the I_{LIM} pin.

Program Current Limit Resistance (kΩ)	10.5	5.2	4.2	3.5	3	2.7	2.4	2.1
Current Limit I_{INLIM}(A)	1	2	2.5	3	3.5	4	4.5	5

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For the stable system operation, recommend to set the current limit level 1.2~1.5 times of the maximum system load current to avoid mis-triggering the current limit and causing system malfunctions.

When power dissipation in the internal MOSFET $P_D = (V_{IN} – V_{OUT}) \times I_{OUT}$ is too high, LS12052BD33 engages thermal foldback and reduce the current limit value so that the device junction temperature TJ maintains around +105°C. In the event device temperature (T_J) exceeds T_{SHDN}, typically 140°C, the thermal shutdown circuitry shuts down the internal MOSFET thereby disconnecting the load from the supply.



Current Limit Thermal Fold-back

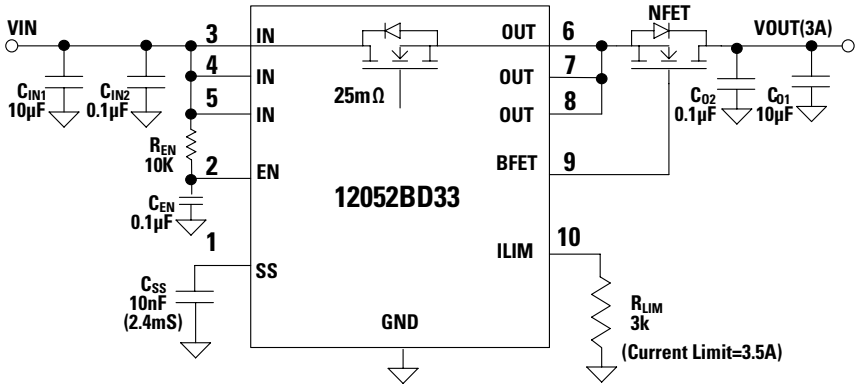
External Blocking MOSFET Gate Control BFET

The BFET pin is provided to drive an external blocking N type MOSFET which can be connected "Back to Back" with the LS12052BD33 output to prevent current flow from load to source in shutdown and in the event of power failure at V_{IN}. When V_{IN} exceeds the under-voltage-lockout threshold and the V_{EN} is above ON threshold, the device turns on the external NFET first. Once the NFET is fully turned on, LS12052BD33 turns on the internal MOSFET and brings up the output with the programmed soft-start ramp rate. When EN pin is pulled low level, both the internal MOSFET and the external blocking NFET are turned off simultaneously.

PCB Layout Guideline

- For all applications, a 10µF or greater ceramic decoupling capacitor is recommended between IN terminal and GND, and a 10µF or greater ceramic decoupling capacitor is recommended between OUT terminal.
- The optimum placement of decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC.
- High current path should be as short as possible.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC. The PCB ground should be a copper plane or island on the board.
- Locate all support components: R_{ILIM}, C_{SS} and resistors for EN, close to their connection pin. Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for the R_{ILIM} and C_{SS} components to the device should be as short as possible to reduce parasitic effects on the current limit and soft start timing.

Application Circuit with an External Reverse Blocking FET



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LS12052BD33

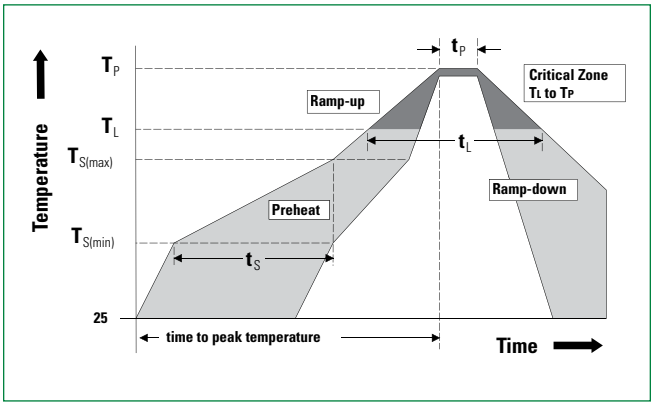
18V, 5A eFuse with Over-Voltage Protection and Blocking FET Control

EVB BOM List

Qty	Ref	Value	Description	Package
1	C_{IN1}	10µF	Ceramic Capacitor, 10V, X5R	0805
1	$_{CO1}$	10µF	Ceramic Capacitor, 10V, X5R	0805
3	C_{IN2}, C_{O2}, Cen	0.1µF	Ceramic Capacitor, 10V, X5R	0603
1	R_{en}	10KΩ	Resistor, ±1%	0603
1	C_{SS}	10nF	Ceramic Capacitor, 10V, X5R	0603
1	R_{ILIM}	3KΩ	Resistor, ±1%	0603
1	NFET	MSG040N03G	RDSON (MAX.) =6mΩ	DFN 3x3_8L
1	U1	LS12052BD33	Load Switch IC	DFN3x3_10L

Soldering Parameters

Average ramp up rate (Tsmin to T_P)		1~2°C/second, 3°C/second max.
Preheat & Soak	**- Temperature Min ($T_{s(min)}$)**	150°C
	- Temperature Max ($T_{s(max)}$)	200°C
	- Time (min to max) (t_s)	60 – 120 secs
Time maintained above	**- Temperature(T_L)**	217°C
	- Time(t_L)	60~150 seconds
Peak Temperature (T_P)		See Classification Temp intable1
Time within 5°C of actual peak Temperature (t_p)		30 seconds max
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.



Notes:

1. Tolerance for peak profile Temperature(T_p) is defined as a supplier minimum and a user maximum.

2. Tolerance for time at peak profile temperature (t_p)is defined as a supplier minimum and a user maximum.

Ordering Information

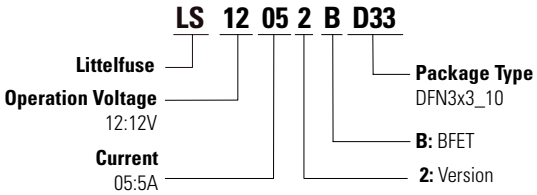
Part Number	Marking	Package	Min. Order Qty.
LS12052BD33	12052B	DFN3x3_10L	5000/Tape & Reel

Pb-freeProcess – Classification Temperatures (TC)

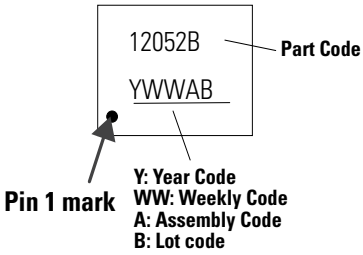
Package Thickness	Volume mm³ <350	Volume mm³ 350-2000	Volume mm³ >2000
<1.6mm	260°C	260°C	260°C
1.6mm–2.5mm	260°C	250°C	245°C
>2.5mm	250°C	245°C	245°C

Note: For all temperature information, please refer to topside of the package, measured on the package body surface..

Part Numbering



Part Marking

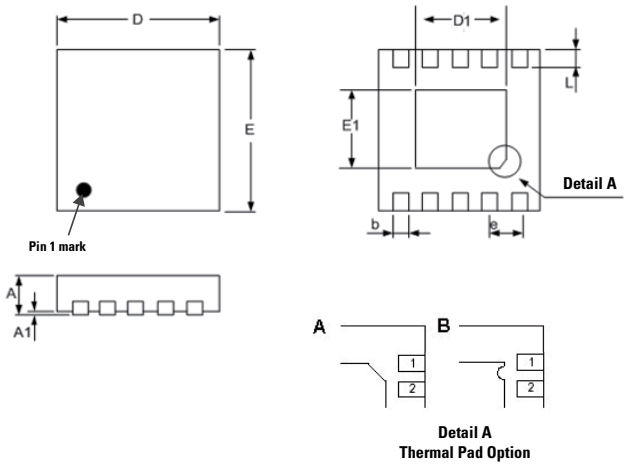


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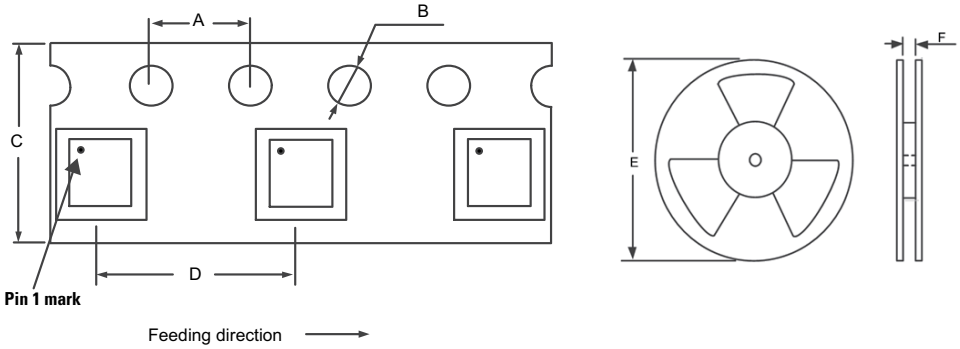
18V, 5A eFuse with Over-Voltage Protection and Blocking FET Control

Dimensions — DFN3x3_10L



Dimension	Millimeters		Inches	
	Min	Max	Min	Max
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D1	2.10	2.60	0.083	0.102
E	2.90	3.10	0.114	0.122
E1	1.35	1.75	0.053	0.069
e	0.50		0.020	
L	0.30	0.50	0.012	0.020

Carrier Tape & Reel Specification — DFN3x3_10L



Symbol	Millimeters
A	4.0
B	1.5
C	12.0
D	8.0
E	13 inch
F	13.0

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LS12052BD33 Protection IC product family revision history			
Revision number	**Comment Date**	**Description (by number)**	**Remarks**
V1	27-Oct-25	as PM Simon request, Please add a line under IINLIM: IINLIM Current Limit RLIM=10kΩ 0.74 (min), 1.05, 1.36 (max) A	Justin Li
V2	17-Nov-25	as PM Simon request, Please remove the line under IINLIM: IINLIM Current Limit RLIM=2.7kΩ 3.6 (min), 4, 4.5 (max) A	Justin Li

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