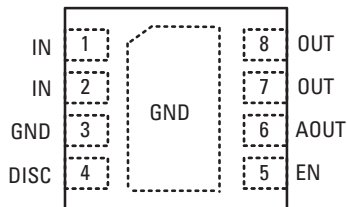


LS2405IDD23

24 V, 5 A Very Low Forward Voltage Diode



Pinout Designation



EXPOSED PAD ON BACKSIDE

Description

The LS2405IDD23 emulates a 5 A very low forward voltage diode that is used in high current diode and diode-OR applications. The LS2405IDD23 integrates a 35 m Ω N-Channel MOSFET to obtain higher efficiency and smaller board area to replace a Schottky diode. LS2405IDD23 detects the forward voltage drop across the MOSFET to ensure the current transfer from one path to the other path smoothly, so it is easily used in the multiple power supplies OR applications that can effectively increase total system reliability. When the input supply fails or is shorted to ground, a fast circuitry can turn off the MOSFET immediately to reduce the reverse current.

LS2405IDD23 is available in low profile 8 lead DFN 2 mmx3 mm package.

Features

- Wide Input Range from 2.7 V to 24 V
- Surge up to 28 V
- Replace a Power Schottky diode with an Integrated 35 m Ω N-Channel MOSFET
- Fast Turn-off Limits Reverse Current
- Smooth Current Transfer from One Power to the Other Power
- Input Supply Rail Discharging Function
- Available in 8 lead 2 mmx3 mm DFN Packages
- Pb-Free and RoHS Compliant

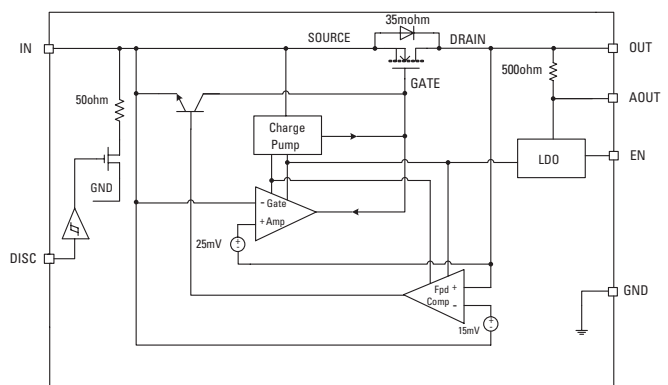
Applications

- USB PD TypeC Ports
- Telecom Infrastructure
- Mutil-input power supply

Pin Description

Pin Name	Pin #	Description
IN	1, 2	Input voltage. Source of the internal N-channel MOSFET.
GND	3	Ground pin.
DISC	4	Input Discharge control input pin. Set DISC pin logic Hi to discharge input through an internal 50 ohm resistor to ground. Set DISC pin logic Lo to disable input discharge. function.
EN	5	Internal N-channel MOSFET Enable pin. EN has accurate ON/OFF threshold of 1.2 V and 1.0 V respectively. Pull it above ON threshold to enable the MOSFET. Pull it below OFF threshold to disable the MOSFET, and the LS2405IDD23 only draws 3 JC.06/05/24 μ A from the AOUT pin. The MOSFET body diode (IN: Anode; OUT: Cathode) can still conduct current when EN pin is pull below OFF threshold. To enable MOSFET all the time, connect EN pin to AOUT pin.
AOUT	6	Supply of the internal circuit. Either connect this pin to OUT directly or bypass this pin to GND with a 1 μ F ceramic capacitor to form a RC hold-up circuit.

Functional Block Diagram



LS2405IDD23

24 V, 5 A Very Low Forward Voltage Diode

Absolute Maximum Rating (Reference to GND)

Symbol	Value	Units
Supply Voltage IN, OUT, AOUT	-0.3 to +28	V
Control Pin EN	-0.3 to +28	V
Control Pin DISC	-0.3 to +6	V
ESD, Human Body Model (HBM)	±2000	V
Junction Temperature Range	-40 to +150	°C
Storage Temperature Range	-65 to +150	°C
Lead Temperature (Soldering 10s)	260	°C

* Notes: Stress exceeding those listed "Absolute Maximum Ratings" may damage the device.

Thermal information

Symbol	Value	Units
Maximum Power Dissipation ($T_A=25\text{ °C}$)	1.4	W
Thermal Resistance (θ_{JA})	72.11	°C/W
Thermal Resistance (θ_{JC})	30.14	°C/W

Note1: Measured on JESD51-7, 4-Layer PCB.

Note 2: The maximum allowable power dissipation is a function of the maximum junction temperature $T_{J,MAX}$, the junction to ambient thermal resistance θ_{JA} , and the ambient temperature T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_{D,MAX} = (T_{J,MAX} - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

Recommend Operating Conditions

Symbol	Value	Units
Supply Input Voltage, V_{IN}	+3 to +24	V
Operating Voltage, V_{OUT}	+2.7 to +24	V
Junction Temperature Range	-40 to +125	°C

* Notes: The device is not guaranteed to function outside of the recommended operating conditions.

Electrical Characteristics ($T_A = +25\text{ °C}$, $V_{IN}=12\text{ V}$, $OUT=AOUT=EN$, $C_{IN}=C_{OUT}=1\text{ }\mu\text{F}$, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range		2.7		24	V
I_{IN}	Quiescent Current	$V_{IN} = 5\text{ V}, V_{EN} = 5\text{ V}, I_{OUT} = 0$		300	350	μA
I_{AOUT}		$V_{IN} = 0\text{ V}, V_{OUT} = V_{AOUT} = V_{EN} = 5\text{ V}, I_{OUT} = 0$		90		μA
I_{STBY}	Standby Current (Internal MOSFET Disabled)	$V_{IN} = 24\text{ V}, V_{EN} = 0\text{ V}$		4	6	μA
V_{ENR}	EN Turn-on Threshold	EN Rising	1.1	1.2	1.3	V
V_{ENF}	EN Turn-off Threshold	EN Falling	0.9	1.0	1.1	V
I_{EN}	EN Internal Pull up Current	$V_{EN} = 1.2\text{ V}$		0.1	0.5	μA
V_{OUTR}	Output UVLO Rising Threshold	AOUT=OUT, Output Rising	2.1	2.2	2.3	V
V_{OUTF}	Output UVLO Falling Threshold	AOUT=OUT, Output Falling	1.95	2.05	2.15	V
t_{ON}	MOSFET Turn-On Time	From EN Lo-to-Hi to MOSFET fully On		90		μs
t_{OFF}	MOSFET Turn-Off Time	From $V_{OUT}-V_{IN} > 15\text{ mV}$ to MOSFET off		300		ns
ΔV_{SD}	Source-Drain Regulation Voltage	$I_{OUT} = 100\text{ mA}$	10	25	40	mV
ΔV_{REV}	Source-Drain Reverse Current Blocking Threshold Voltage			-15		mV
V_{DIODE}	N-Channel MOSFET Body diode Forward Voltage Drop	$V_{IN} = 5\text{ V}, V_{EN} = 0\text{ V}, I_{OUT} = 100\text{ mA}$		0.6	0.8	V
$R_{DS(ON)}$	N-Channel MOSFET Ron	$V_{IN} = V_{EN} = 5\text{ V}, I_{OUT} = 2\text{ A}$		35		m Ω
I_{NCH_LKG}	N-Channel MOSFET Leakage Current	$V_{IN} = V_{EN} = 0\text{ V}, V_{OUT} = 24\text{ V}$, Measure I_{IN}		1	10	μA
V_{HI}	DISC Logic Input High		1.2			V
V_{LO}	DISC Logic Input Low				0.4	V
R_{DPD}	DISC Internal Pull Down Resistor		700	1000	1300	k Ω
R_{DISC}	Input Voltage Discharge Resistor	$V_{IN} = V_{DISC} = 5\text{ V}, V_{EN} = 0\text{ V}$		50	100	Ω

LS2405IDD23

24 V, 5 A Very Low Forward Voltage Diode

Figure 1 : Power Dissipation vs. Load Current

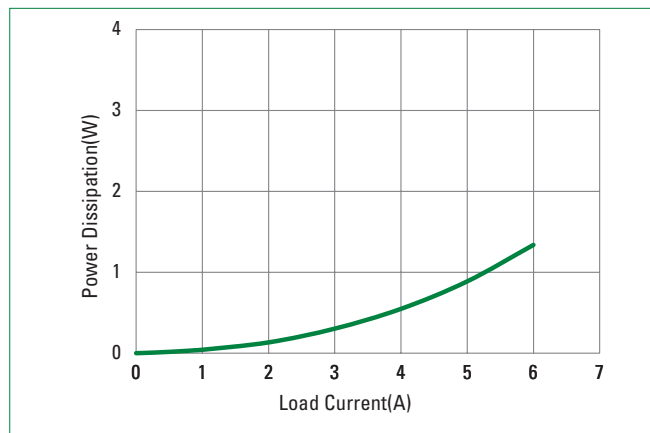


Figure 2 : Quiescent Current vs. V_{IN}

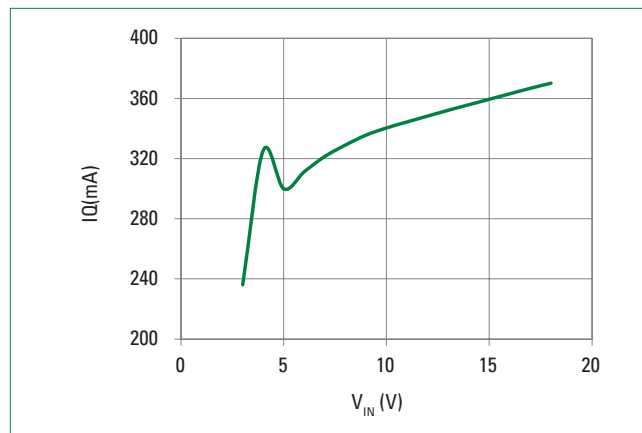


Figure 3 : Shut Down Current vs V_{IN}

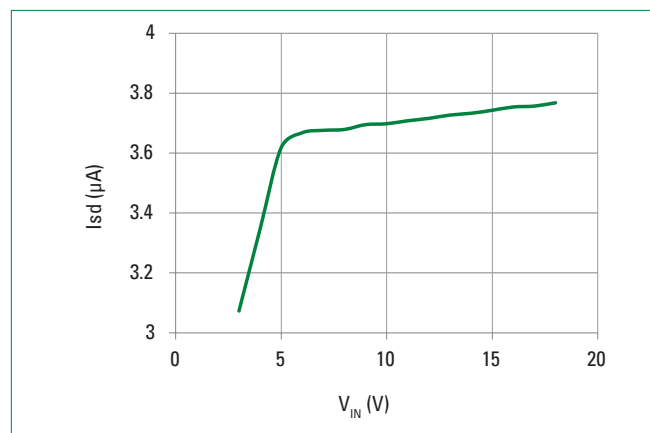


Figure 4 : OUT Current vs V_{OUT}

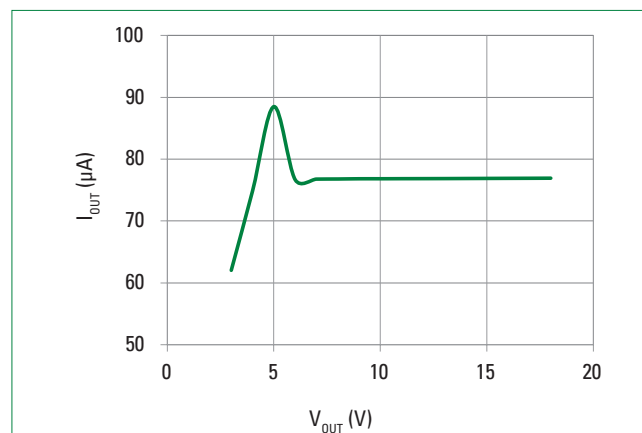


Figure 5 : MOSFET Turn On

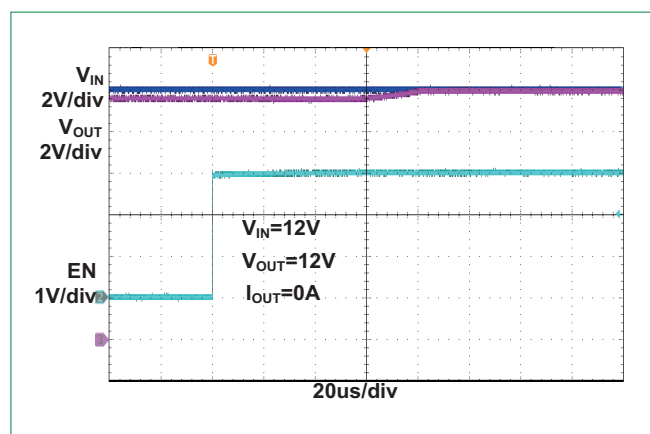
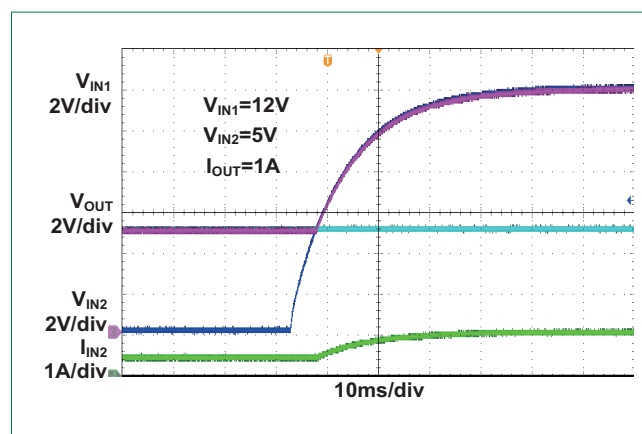


Figure 6 : Switchover from a Lower Input to a Higher Input Supply



LS2405IDD23

24 V, 5 A Very Low Forward Voltage Diode

Figure 7 : Switchover from a Higher Input to a Lower Input Supply

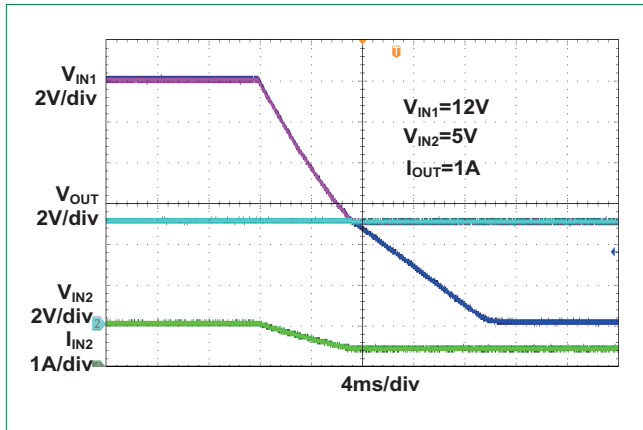


Figure 8 : V_{IN} Power on

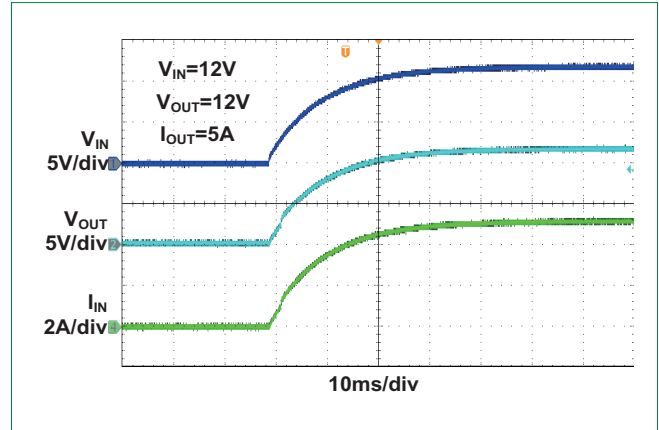


Figure 9 : 2-Redundant Input Supplies Switchover

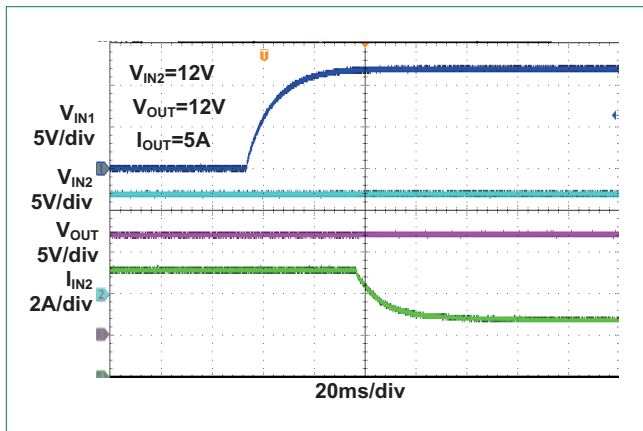
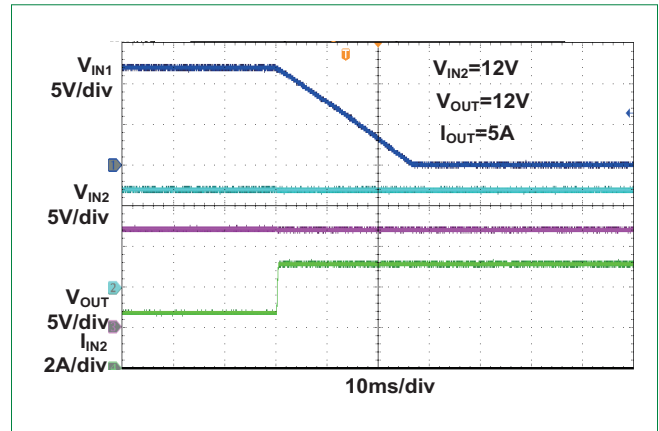


Figure 10 : 2-Redundant Input Supplies Switchover



LS2405IDD23

24 V, 5 A Very Low Forward Voltage Diode

Theory of Operation

Parallel-connected supplies are widely used to enhance system reliability. High availability system often applies ORing diodes to connect these supplies in parallel at the point of load, however, the forward drop voltage of the diode increases energy dissipation and reduces the efficiency. The LS2405IDD23 integrates an internal N-channel MOSFET to replace the diode that can improve the available voltage and effectively reduce the power loss, heat sinks and large thermal layouts.

The LS2405IDD23 is a single positive voltage diode that drives an internal N-channel MOSFET as a pass transistor in parallel with MOSFET body diode to replace a Schottky diode. The IN and OUT pins form the anode and cathode of the diode. The input supply is connected to the IN pins, while the OUT pins serve as the output. AOUT pin is the supply for the LS2405IDD23, and connect this pin to OUT either directly or through an RC hold-up circuit.

At power-up, the load current initially flows through the body diode of the internal N-channel MOSFET. The internal N-channel MOSFET turns on and an amplifier tries to regulate the voltage drop across the IN and OUT connections to 25 mV. If the load current causes more than 25mV of drop, the MOSFET is driven fully on and the voltage drop is equal to $R_{DS(ON)} \times I_{LOAD}$.

If the load current is reduced causing the forward drop to fall below 25 mV, the internal MOSFET gate voltage is regulated lower in an attempt to maintain the drop at 25 mV. If the load current reverses, the MOSFET is turned off quickly with a strong pull-down circuit.

Where LS2405IDD23's are used to combine the outputs of two supplies, the power supply with the highest output voltage sources most or all of the current. If this supply's output is quickly shorted to ground while delivering load current, the current temporarily reverses and flows backwards through the LS2405IDD23. When reverse current flows, the LS2405IDD23 is quickly turned off.

Application Information

The LS2405IDD23 is an diode that uses an internal N-channel MOSFET to replace the Schoktty diode. It is typically used for redundant supplies application. It operates with high efficiency and provides reverse current protection for systems.

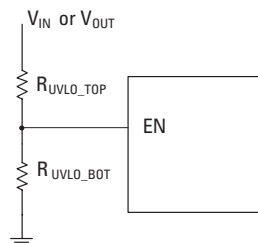
Input and Output Capacitor Selection

For stable operation, recommend to place a 1μF or higher ceramic type X5R or X7R bypass capacitor at the VIN and VOUT pins.

Setting Input or Output Under-voltage Lockout (UVLO) for Nch-MOSFET

EN has accurate ON/OFF threshold of 1.2 V and 1.0 V respectively. The EN pin voltage must be greater than 1.2 V (typical) to enable the LS2405IDD23 internal Nch-MOSFET. The device enters standby mode when the EN voltage is less than 0.4 V. In standby mode, the input supply current for the device is less than 4 μA. En accurate ON threshold can be used to build an external IN or OUT adjustable under-voltage lockout circuit. As shown in Picture 1, a resistor divider from the VIN pin to GND sets the input UVLO level. EN pin has an internal 160 nA(Typical) pull up current, and choose the bottom UVLO resistor RUVLO_BOT in the 10 kΩ~200 kΩ range to set the divider current at 10 μA or higher. Typically select RUVLO_BOT=100 kΩ. The value of top resistor RUVLO_TOP, depending on the desired turn-on voltage VSTART at the VIN pin, can be calculated with Equation 1:

$$R_{UVLO_TOP} = R_{UVLO_BOT} \times \left(\frac{V_{START}}{V_{EN}} - 1 \right) = 100 \text{ k}\Omega \times \left(\frac{V_{START}}{1.2V} - 1 \right) \quad (\text{Equation 1})$$



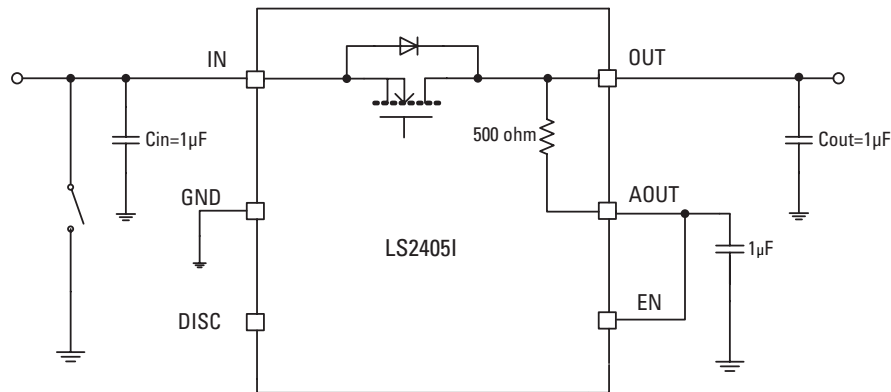
Picture 1. Input/Output UVLO Setting for Nch-MOSFET

LS2405IDD23

24 V, 5 A Very Low Forward Voltage Diode

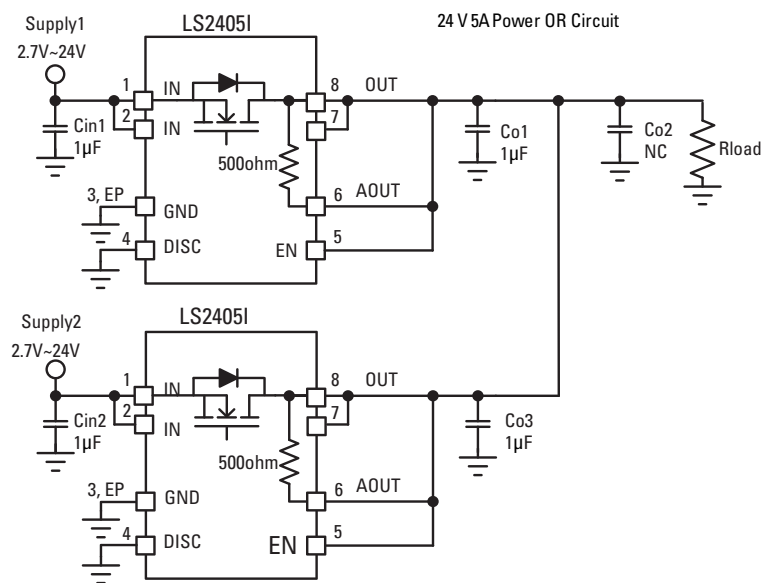
AOUT Hold-Up Circuit

In the event of an input short, parasitic inductance between the input supply of the LS2405IDD23 and the load bypass capacitor may cause AOUT to glitch below its minimum operating voltage. This causes the turn-off time to increase. To preserve the fast turn-off time failure, recommend to bypass AOUT to GND with 1 μ F ceramic capacitor to form RC hold-up circuit as shown in Picture 2.



Picture 2. Protect AOUT Collapse from Input Short with Large Parasitic Inductance

Application Schematic



Picture 3. Application Example

EVB BOM List

Qty	Ref	Value	Description	Package
2	C _{IN1} , C _{IN2}	1 μ F	Ceramic Capacitor, 10V, X5R	0603
1	C _{O1} , C _{O3}	1 μ F	Ceramic Capacitor, 10V, X5R	0603
1	C _{O2}	NC	-	-
1	R _{LOAD}	-	System Loading	-
2	U1,U2	LS2405IDD23	Very Low Forward Voltage Diode IC	DFN2x3_8

LS2405IDD23

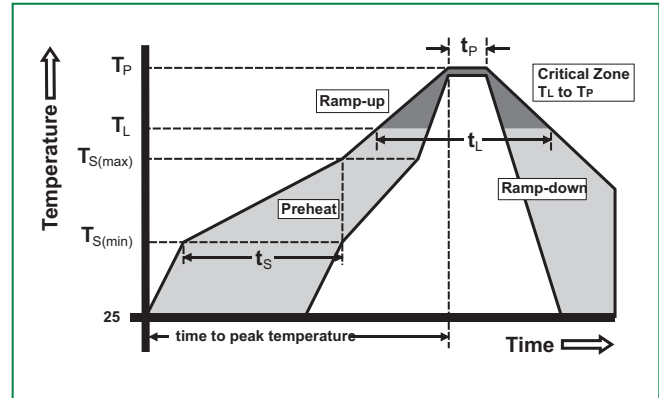
24 V, 5 A Very Low Forward Voltage Diode

Soldering Parameters

Average ramp up rate (T_{smin} to T_p)		1~2 °C/second, 3 °C/second max.
Preheat & Soak	- Temperature Min ($T_{s(min)}$)	150 °C
	- Temperature Max ($T_{s(max)}$)	200 °C
	- Time (min to max) (t_s)	60 – 120 secs
Time maintained above	- Temperature(T_L)	217 °C
	- Time(t_L)	60~150 seconds
Peak Temperature (T_p)		See Classification Temp intable1
Time within 5°C of actual peak Temperature (t_p)		30 seconds max
Ramp-down Rate		6 °C/second max
Time 25°C to peak Temperature (T_p)		8 minutes Max.

Note 1: Tolerance for peak profile Temperature(T_p) is defined as a supplier minimum and a user maximum.

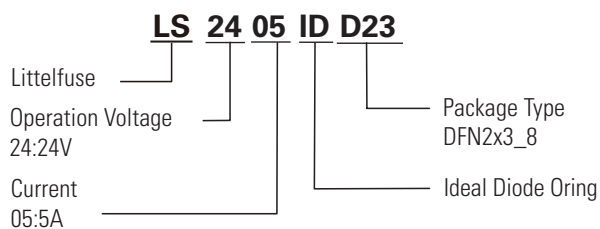
Note 2: Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.



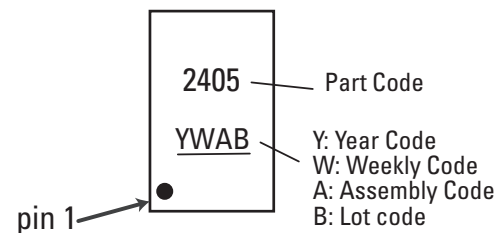
Ordering Information

Part Number	Package	Min. Order Qty.
LS2405IDD23	DFN2x3_8	3000/Tape & Reel

Part Numbering



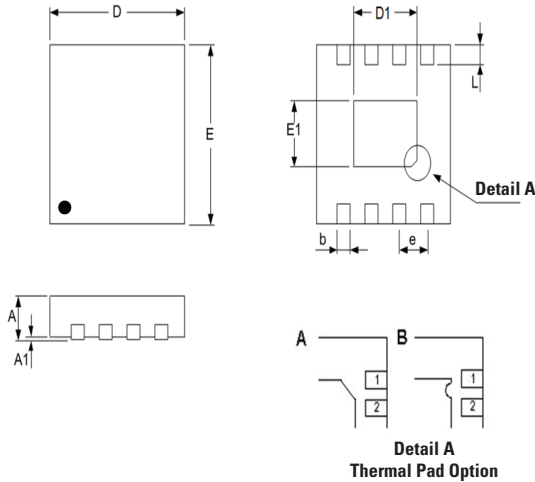
Part Marking



LS2405IDD23

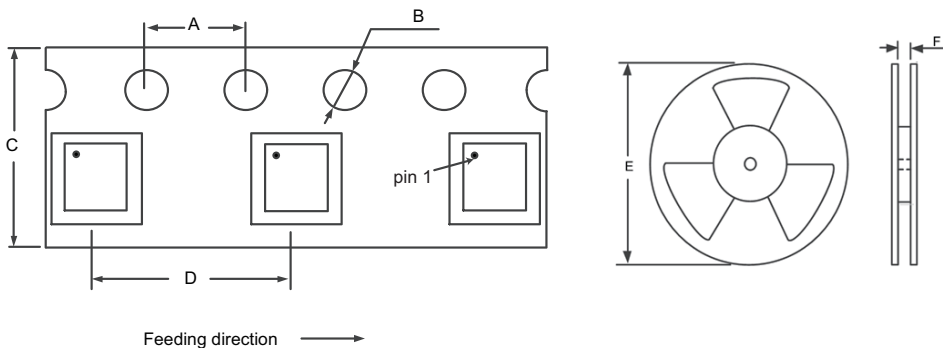
24 V, 5 A Very Low Forward Voltage Diode

Dimensions — DFN2x3_8



Dimension	Millimeters		Inches	
	Min	Max	Min	Max
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
b	0.20	0.30	0.008	0.012
D	1.90	2.10	0.075	0.083
D1	1.35	1.60	0.053	0.063
E	2.90	3.10	0.114	0.122
E1	1.25	1.60	0.049	0.063
e	0.50		0.020	
L	0.22	0.40	0.009	0.016

Carrier Tape & Reel Specification — DFN2x3_8



Symbol	Millimeters
A	4.0
B	1.5
C	8.0
D	4.0
E	7 inch
F	9.0

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