Overvoltage Protection for Power Semiconductors in Solid-State DC Breakers for BESS and Datacenter Applications

Abstract

This white paper reviews the effective use of Transient Voltage Suppression (TVS) diodes in solid-state DC-breaker applications and their constraints. The thermal behavior under surge conditions is simulated, and insights are provided into how the switching behavior of the power semiconductor and its packaging influence the effectiveness of a TVS diode. Finally, suggestions are offered for optimizing externally placed TVS diodes to protect the power semiconductors at large. The main content of this work was previously published at the PCIM Europe Conference 2025.

1. Introduction

With the increasing interest in DC-grid technology [1] and its fast adoption in battery energy storage systems (BESS) and datacenter applications, the need for solid-state DC circuit breakers (SSCB) has gained momentum. The SSCB offers much faster response times over conventional protection components such as fuses or mechanical contactors, which is essential for managing the high voltages and currents typically found in DC systems and for avoiding catastrophic failures of BESS [2, 3]. Additionally, SSCBs can quickly interrupt fault currents multiple times, reducing potential damage and ensuring system stability. In contrast, fuses are limited to single events and mechanical relays exhibit a significantly shorter current-breaking lifetime compared to their mechanical lifetime. However, the power semiconductors within these breakers are prone to overvoltage failures and require protection.

For this reason, solutions such as Transient Voltage Suppression (TVS) diodes, Metal-oxide varistors (MOV), snubber circuits, or combinations thereof are employed. TVS diodes effectively clamp excessive transient voltages at narrow voltage tolerances, preventing semiconductor failure and enhancing the overall durability and efficiency of DC-grid systems. MOVs, on the other hand, can dissipate higher energy in a smaller form factor, though at the cost of higher voltage limiting tolerances and a limited lifetime. Selecting the appropriate TVS diode for a given application is critical to ensuring safe and reliable operation in modern electrical infrastructures. Additionally, for the overall voltage clamping function, active clamping offers another mechanism to protect the power semiconductor during turn-off transition. In case of short-circuit events, for Insulated Gate Bipolar Transistors (IGBTs), desaturation detection combined with soft turn-off can help to protect SSCBs during operation.

1.1. Solid-State DC Breakers

Figure 1 illustrates the basic block diagram of a bi-directional solid-state DC breaker. Depending on the voltage class, Silicon or Silicon-carbide MOSFETs or Silicon IGBTs are possible power semiconductor technologies that can be used in solid-state DC breakers.

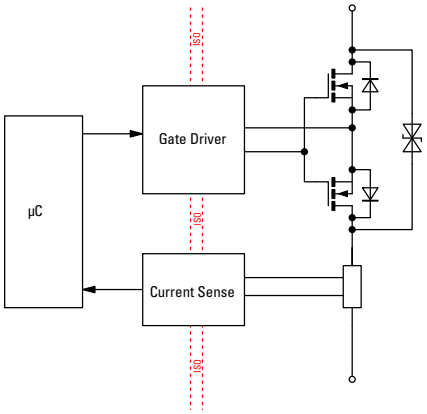

Figure 1.Block diagram of a bi-directional solid-state DC breaker using MOSFETs and TVS

Solid-state DC breakers are crucial for high-reliability and safety applications. Especially when arc flashing must be avoided, solid-state DC breakers are superior to mechanical contactors [2]. Application fields range from battery protection in low-voltage systems, such as forklift batteries, to heavy duty commercial truck batteries [3], medium-voltage BESS in ships [4], and DC grids used in industrial and datacenter applications. In general, the higher the system voltage gets, the more critical the overvoltage protection devices become, since catastrophic failures will have more drastic impacts.

A solid-state DC breaker can be designed by using single power semiconductor switches, for example, discrete MOSFETs like IXFA230N075T2-7 [5] or discrete IGBTs like IXYN220N65A5 [6], or built as a power module shown in [3] or as a single switch like FZ2400R12HE4_B9 [7]. A control and sensing circuitry, as well as over-voltage protection, need to be added, as indicated in Figure 1. For industrial and upcoming datacenter DC-grids, DC-breakers need to work with nominal voltages of U_{DC} = 600…800 V and turn-off at overvoltages of U_{DC} = 850 V [1]. Therefore, IGBTs with blocking capability of at least $U_{CE,max}$ = 1200 V, preferrably 1700 V, are utilized to ensure immunity against grid transients.

As a generic example, Figure 2 shows the schematic of a uni-directional DC breaker using three independent IGBTs as integrated in the module [7]. The package of the power module [7] has three single switches that are not connected with each other internally. Therefore, an external bus bar is required to connect them, and additional overvoltage protection is required. The internal stray inductance from the datasheet is given with only 6 nH for the whole module. However, from the outer dimensions of the package, a total loop stray inductance of more than 100 nH can be expected, if the protection device and the main terminal connections are mounted only on one side of the module, meaning asymmetrically, as indicated by Figure 2.

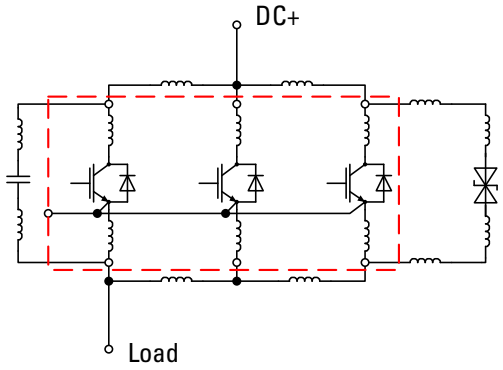

Figure 2. Circuit diagram of a uni-directional DC-breaker based on an IGBT module in high-power package, with externally added TVS for overvoltage protection in asymmetric assembly

To overcome these challenges, a symmetric layout approach is important. Figure 3 indicates the schematic of such a symmetric approach using external TVS diodes and snubber capacitors.

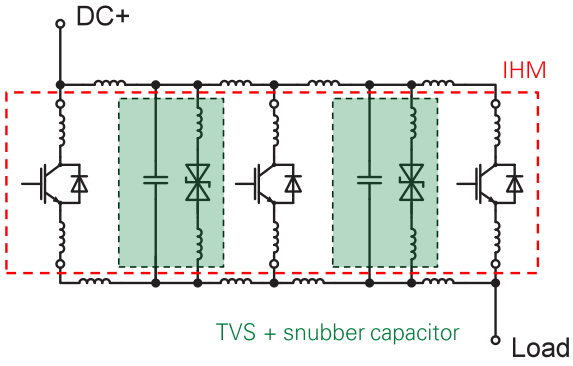

Figure 3. Circuit diagram of a symmetric approach for the power module of [7] using external protection components

The same principle applies to bi-directional DC breaker switches, both for voltage levels below 60 V_{DC} for residential BESS and 48 V for datacenter applications, and higher voltage levels around 1 kV for industrial BESS.

1.2. Design Considerations for Overvoltage Protection of Power Semiconductors in SSCB

For the previously described example, careful consideration must be given to the overvoltage protection of power semiconductors in the SSCB application. Ideally, an SSCB should not be switched on under full load current. It must be capable of withstanding certain inrush current levels without getting damaged. More critical are scenarios involving switching off at nominal load current conditions, and especially under short circuit conditions. The inherent stray inductances, both within the SSCB and in the load cabling, will create induction voltages upon any change of load current.

Taking the module FZ2400R12HE4_B9 [7] as an example, when assuming a maximum turn-off current of I_{CRM} = 4800 A and a current slope of di/dt = 10 kA/µs, it can safely operate at U_{DC} = 1140 V, (see [7], RBSOA diagram on page 6). If an additional load cable inductance of L_{cable} = 1 µH exists, the energy stored in the cable's inductance amounts to 11.52 J, as shown in Equations 1 and 2. The overvoltage caused by the cable inductance would then result in U_{cable} = 10 kV, based on Equation 3.

$$E_{cable} = ½ \cdot L_{cable} \cdot i^2_{load} \quad (1)$$

$$E_{cable} = ½ \cdot 1\ \mu H \cdot (4800\ A)^2 = 11.52\ J \quad (2)$$

$$U_{cable} = L_{cable} \cdot di/dt \quad (3)$$

Hence, to protect the IGBT from breakdown, an external TVS or MOV assembly needs to clamp the voltage and dissipate the energy of the cable reliably. For the given example of the FZ2400R12HE4_BE9 module, the 6 kA-rated Littelfuse AK6-430C-Y [8] device could be suitable. This high-power TVS diode series is one of the most capable discrete devices on the market.

For a typical ambient temperature inside of electrical cabinets of T_{amb} = 70°C, a maximum virtual junction temperature of T_{vj} = 125°C, and a temperature swing of ΔT = 55 K, the peak power needs to be derated to approximately 85 % based on the datasheet [8]. The peak pulse power at a pulse width of approximately 100 µs can be read from the datasheet to approximately P_{PPM} = 1050 kW, which corresponds to an energy of $E_{TVS,max}$ = 105 J that can be absorbed by the AK6 device. Derating to 85 % results in E_{surge} = 89.25 J. Vice versa, this means that the cable inductance could amount to the maximum value of:

$$L_{cable} = 89.25\ J/11.52\ J/1\ \mu H = 7.7\ \mu H$$

2. Test Circuit Design

For testing purposes, a small SSCB prototype was designed to demonstrate the influence of parasitic stray inductances of the overall PCB design, component placements, and the connection of the SSCB to the main circuitry. A test board was designed to incorporate the challenges shown in section 1.1 with asymmetric and symmetric protection layout design. As an example application, the test board targets BESS or datacenter power supplies with voltages up to 96 V. Four Littelfuse 200 V MOSFETs in a TO-leadless package with $R_{DS(on)}$ = 10.6 mΩ were assembled in parallel. The test board included different options for mounting TVS diodes for both overvoltage clamping of the external connections and active clamping of the MOSFETs. Additionally, the external connections to the load circuit could be varied. Figure 4 shows a rendering of the test board.

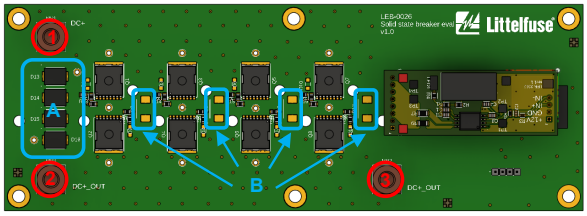

Figure 4. 3D rendering of the test board including gate driver board, TVS diode positions A and B and active clamping circuitry. The main terminals are indicated by 1, 2, and 3.

The board incorporates the possible test configurations given in Table 1.

Table 1. Possible test cases with different configurations of the main terminal connection and TVS configurations

Test Case	Main Terminal Connection	TVS Configuration
1	Asymmetric (1-2)	Asymmetric (A)
2	Symmetric (1-3)	Asymmetric (A)
3	Asymmetric (1-2)	Symmetric (B)
4	Symmetric (1-3)	Symmetric (B)

The asymmetric main terminal connection is defined as a cable connection at terminals 1 and 2. This causes the load current flow from terminal 1 through the MOSFETs SW1–SW4 to terminal 2. The symmetric main terminal connection is defined as a cable connection at terminals 1 and 3. This causes the current to flow from terminal 1 through the MOSFETs SW1–SW4 to terminal 3. The geometrically symmetric connection helps to balance the current sharing of the MOSFETs.

Test cases 1 and 2 closely represent the configuration that is seen when using standard power modules, where space constraints or large assembly sizes limit the ability to place TVS diodes in close proximity to the power semiconductor switches. Test cases 3 and 4 incorporate the possibility of a symmetric layout and put TVS diodes close to the power semiconductor switches. Therefore, test case 1 is expected to show the worst results while test case 4 is likely to produce the best results with regards to overvoltage protection.

The TVS diodes used for this test case are standard Littelfuse 8.0SMDJ100CA [9] off-the-shelf devices, without sorting. Based on datasheet values, this device can handle up to P_{PPM} = 21 kW Peak Pulse Dissipation at a pulse width of t_d = 100 µs and need to be derated to 80 % at T_{vj} = 70°C. This corresponds to an energy handling capacity of E_{surge} = 1.68 J. The tests were conducted MOSFET by MOSFET to harmonize the probe signals and avoid tolerance variations. Rogowski coils (PEM, CWTUM/6/B) and passive probes (Teledyne LeCroy, PP021) were used to measure the currents and voltages respectively. To account for a large cable inductance, a separate air-cored coil was used. Figure 5 illustrates the test setup.

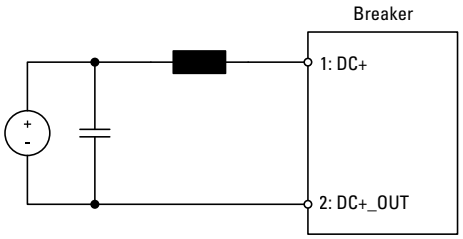

Figure 5. Circuit diagram of test setup

3. Measurement Results

The tests were conducted according to the test cases listed in Table 1. The results are discussed in the following sections.

3.1. Effect of Terminal Connection Symmetry with Asymmetric TVS Clamping

The measured waveforms for test cases 1 and 2 are illustrated in Figure 6 and Figure 7 respectively. The TVS diodes are mounted asymmetrically close to the main terminals 1–2 at the left of the PCB, as indicated in Figure 4, while the cables are connected differently in both test cases.

For test case 1, the overvoltage at the MOSFETs during the turn-off event increases with the distance of the MOSFET position from the TVS assembly. From Figure 6 in test case 1, the maximum overvoltage at the terminals is below 139.6 V, while the maximum voltage at SW4 reaches 159.6 V. The voltage is 152.0 V at SW1, 157.2 V at SW2, and 159.1 V at SW3. The measured waveforms of test case 2 are illustrated in Figure 7. The maximum voltage at the terminals is approximately 128 V, while the maximum voltage for SW4 is 158 V. The overvoltage on SW1 – SW3 reduces slightly.

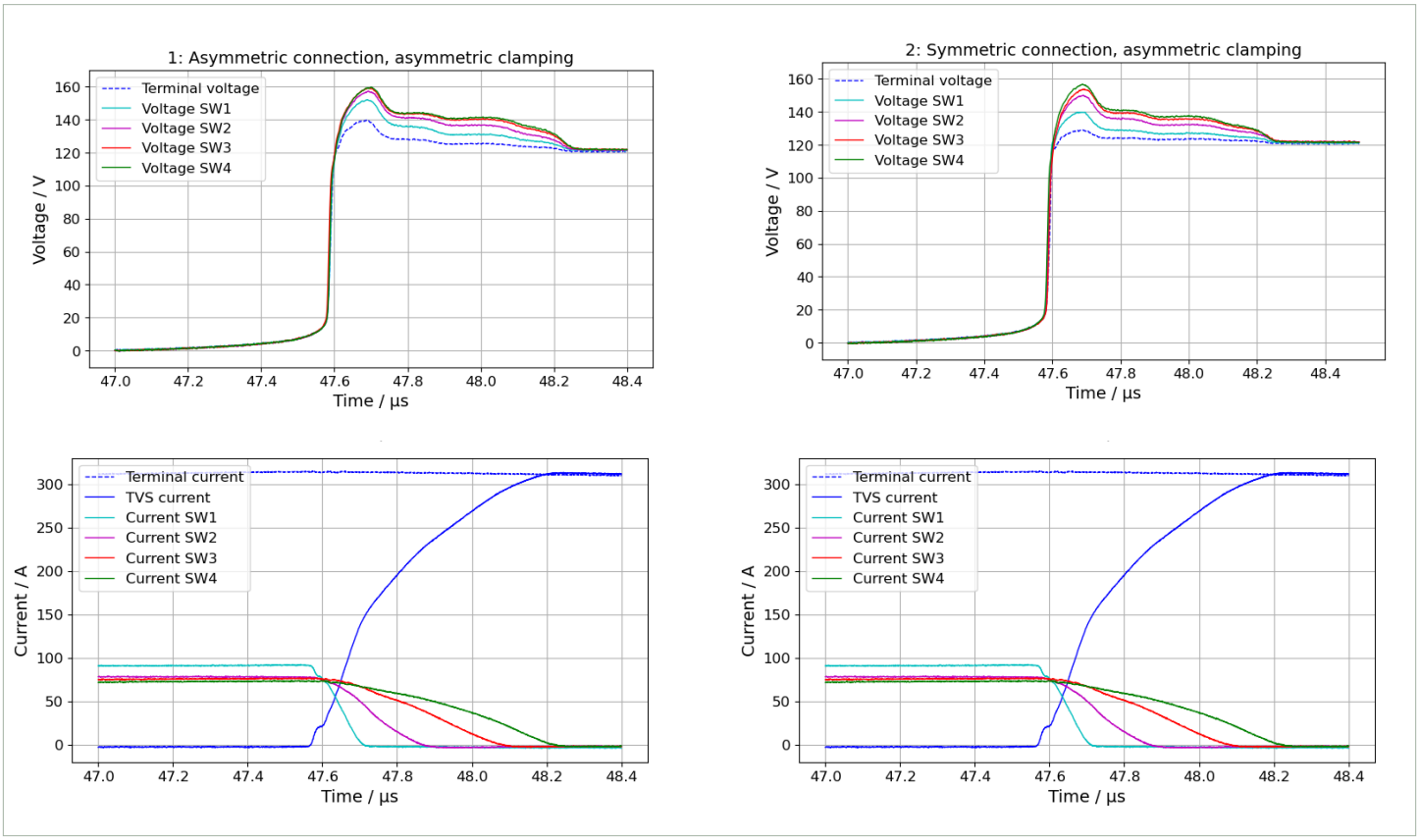

Figure 6. Measured waveforms of test case 1 with asymmetric terminal connections on terminals 1 and 2 and asymmetric TVS clamping

Figure 7. Measured waveforms of test case 2 with symmetric terminal connections on terminals 1 and 3 and asymmetric TVS clamping

Although the main terminals are connected to the test board in a symmetric manner, the overvoltage reduction at SW2–4 is less significant than expected. However, the distance of the asymmetric TVS assembly from the switch still increases for each MOSFET, leading to high overvoltage. For both test cases 1 and 2, the current fall times of the MOSFETs are very similar to each other.

3.2. Effect of Terminal Connection Symmetry with Symmetric TVS Clamping

The measured waveforms of test cases 3 and 4 are illustrated in Figure 8 and Figure 9, respectively. The TVS diodes are mounted symmetrically close to each MOSFET, while the cables are connected differently in both test cases.

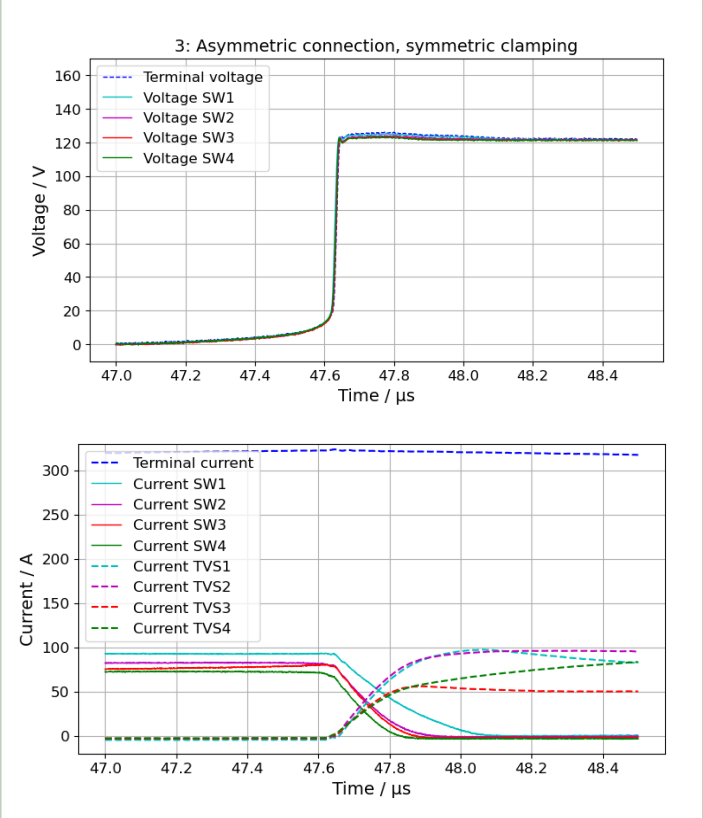

Figure 8. Measured waveforms of test case 3 with asymmetric terminal connections on terminals 1 and 2 and symmetric TVS clamping

3.2. Effect of Terminal Connection Symmetry with Symmetric TVS Clamping

The measured waveforms of test cases 3 and 4 are illustrated in Figure 8 and Figure 9, respectively. The TVS diodes are mounted symmetrically close to each MOSFET, while the cables are connected differently in both test cases.

Compared to test cases 1 and 2, the overvoltage across switches SW1 to SW4 is significantly reduced by more than 17 % and up to 22.7 %, as seen in Table 2. The value is clamped very closely to the breakdown voltage V_{BR} of the utilized 100 V rated 8.0SMDJ100CA TVS diode [9], which has a maximum specified V_{BR} 0f 123 V, as listed in Table 3.

Table 2. Percentage of overvoltage reduction for each test case with reference to test case 1

Test Case	1	2	3	4
Terminals	100 %	-7.6 %	-9.7 %	-9.7 %
SW1	100 %	-8.1 %	-17.6 %	-17.4 %
SW2	100 %	-4.6 %	-21.1 %	-20.7 %
SW3	100 %	-3.4 %	-22.2 %	-22.0 %
SW4	100 %	-1.8 %	-22.7 %	-22.6 %

Table 3. Overvoltage at different measurement positions for each test case

Test Case	1	2	3	4
Terminals	139.6 V	129.0 V	126.1 V	126.1 V
SW1	152.0 V	139.7 V	125.2 V	125.5 V
SW2	157.2 V	150.0 V	124.1 V	124.7 V
SW3	159.1 V	153.7 V	123.8 V	124.1 V
SW4	159.6 V	156.7 V	123.4 V	123.6 V

From the waveforms in Figure 8 and Figure 9, it is also obvious that the current sharing of the single TVS diodes is unbalanced. Since TVS diodes are designed to clamp defined voltages, the clamping current varies with the tolerances of the devices.

Additionally, due to the negative temperature coefficient, it is not feasible to ensure that TVS diodes share the current evenly. Therefore, paralleling of TVS diodes is generally not recommended. This limitation should be considered during the design phase, for example, stray inductance optimization.

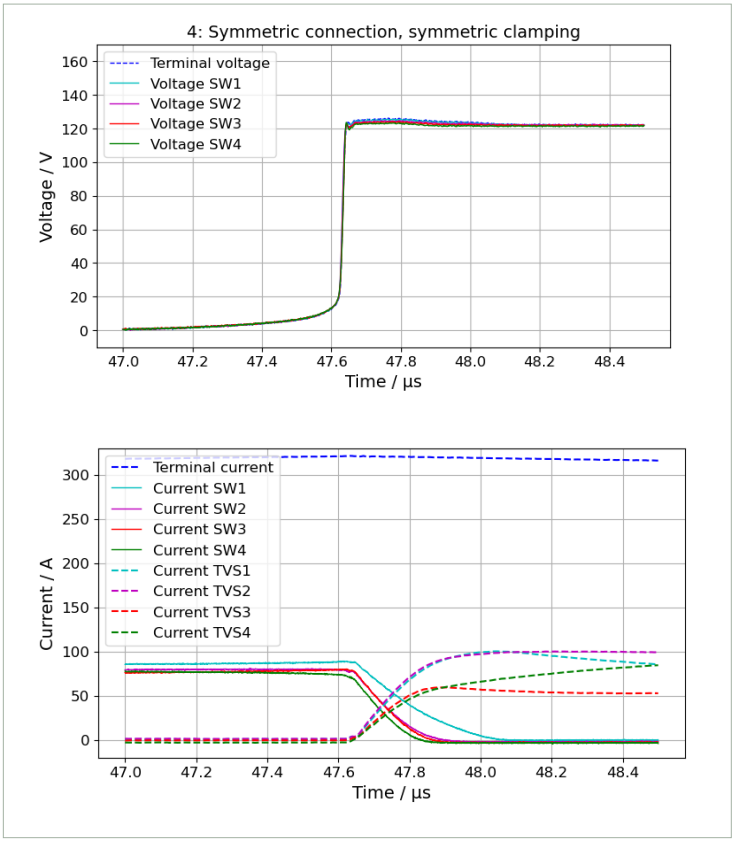

Figure 9. Measured waveforms of test case 4 with symmetric terminal connections on terminals 1 and 3 and symmetric TVS clamping

4. Summary

In this study, the authors investigated the voltage clamping performance of TVS diodes in the application of SSCB under different mechanical layout scenarios. The presented test results affirm that while TVS diodes are effective in providing over-voltage protection, their inherent characteristics limit their ability to share current evenly when paralleled. The results underscore the importance of understanding the influence of parasitic stray inductances and voltage tolerances of the target TVS diode attachment regarding the MOSFET position during the overvoltage clamping event. In the example of the 96 V BESS or 48 V datacenter application, typically MOSFETs with a blocking voltage of 150 V would suffice; however, the results show that for a high stray inductance design, 200 V MOSFETs are required, although the TVS is selected for the corresponding voltage class. Only the reduction of stray inductance with the symmetric TVS attachment close to the MOSFETs significantly reduced the overvoltage and therefore the MOSFET voltage class. This emphasizes the need for thorough device investigations and layout optimization during the early engineering stage of the PCB layout and assembly to ensure reliable and efficient protection of the SSCB. Future research may explore alternative methods and components to enhance current sharing and overall performance in overvoltage protection systems.

5. References

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