

DFNAK3 Series

Surface Mount - DFN10*8*3 - 3 kA



Maximum Ratings and Thermal Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Operating Junction Temperature	T_J	-55 to 125	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 to 150	$^\circ\text{C}$
Current Rating ¹	I_{PP}	3	kA
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	70	$^\circ\text{C/W}$
Thermal Resistance Junction to Case	$R_{\theta JC}$	20	$^\circ\text{C/W}$

Note:

1. Rated I_{PP} measured with 8/20 μs pulse.

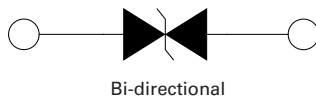
Description

The DFNAK3 series offers a clamping voltage lower than alternative technologies such as MOVs and GDTs. Rated to 3 kA (8/20 μs) surge current, DFNAK3 series offers a high level of protection for mission critical and high reliability applications. It aids compliance to surge requirements such as IEC 61000-4-5 (Level 4). The compact surface mount DFN10*8*3 package is compatible with automated PCBA processes and enables high power density designs.

Features

- Compact surface mount DFN10*8*3 package
- Ideal for automated PCBA processes with reduced manufacturing cost and increased soldering quality as compared to axial leaded packages
- Foldback technology for superior clamping factor
- $V_{BR} @ T_J = V_{BR} @ 25^\circ\text{C} \times (1 + \alpha T \times (T_J - 25))$ (αT : Temperature Coefficient, typical value is 0.1 %)
- Glass passivated chip junction
- ESD protection of data lines in accordance with IEC 61000-4-2, 30 kV(Air), 30 kV (Contact)
- Low dynamic resistance enabling superior low clamping voltage
- UL recognized compound meeting flammability rating UL94 V-0
- Meets MSL level 1, per J-STD-020, LF maximum peak of 250 $^\circ\text{C}$
- Matte tin lead-free plated
- Halogen free and RoHS compliant
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin (Sn) (IPC/JEDEC J-STD-609A.01)

Functional Diagram



Applications

DFNAK3 Series is ideal for the protection of I/O Interfaces, V_{CC} bus and other vulnerable circuits used in ICT, Industrial and Consumer electronic applications.

It aids compliance to surge requirements such as IEC 61000-4-5 (Level 4) for interfaces used in exposed PoE ports, Small Cells, Remote Radio Units (RRUs) and Baseband Units (BBUs), and other high power DC bus in harsh environments.

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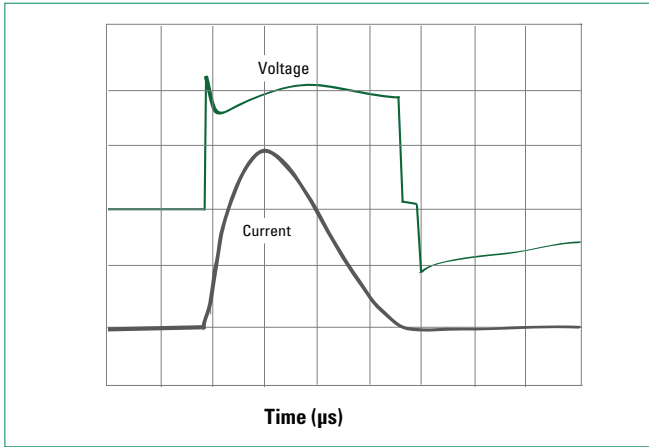
Electrical Characteristics ($T_A = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Part Number (Bi)	Marking	Standoff Voltage (V_R) (V)	Max Reverse Leakage (I_R) @ V_R (μA)	Reverse Breakdown Voltage (V_{BR}) @ I_T		Test Current I_T (mA)	Max Clamping Voltage V_C @ Peak Pulse Current (I_{PP}) (8/20 μs)		Max Capacitance 0 V Bias 10 kHz (nF)
				Min Volts	Max Volts		V_C Volts	I_{PP} (A)	
DFNAK3-058C-D1	58C3K	58	10	64	70	10	100	3000	3.1
DFNAK3-066C-D1	66C3K	66	10	72	80	10	110	3000	2.7
DFNAK3-072C-D1	72C3K	72	10	80	90	10	120	3000	2.4
DFNAK3-076C-D1	76C3K	76	10	85	95	10	125	3000	2.2
DFNAK3-080C-D1	80C3K	80	10	89	100	10	130	3000	2.1

Note: Using 8/20 μs wave shaped defined in IEC 61000-4-5.

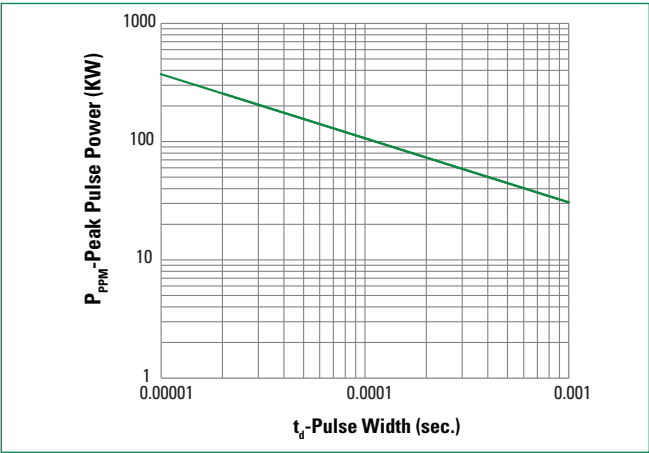
Ratings and Characteristic Curves ($T_A = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Figure 1 - Surge Response (8/20 Surge current waveform)



Note:
The power dissipation causes a change in avalanche voltage during the surge and the avalanche voltage eventually returns to the original value when the transient has passed.

Figure 2 - Typical Peak Pulse Power Rating



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Figure 3 - Pulse Waveform

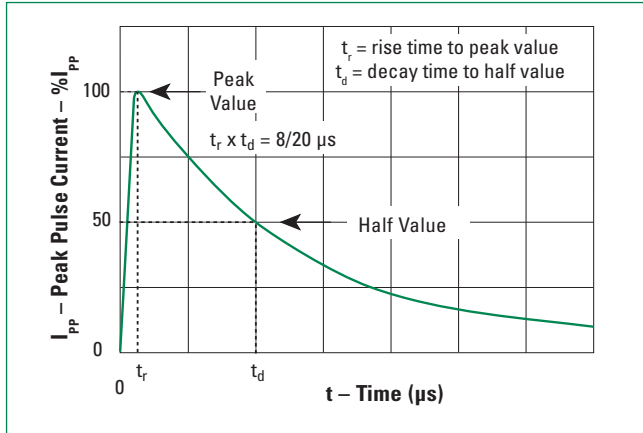
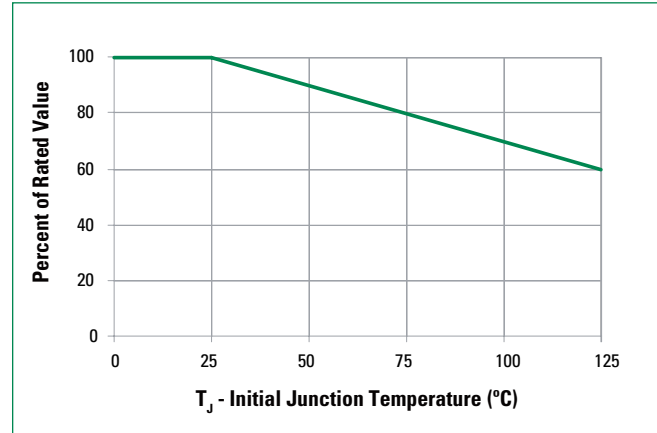


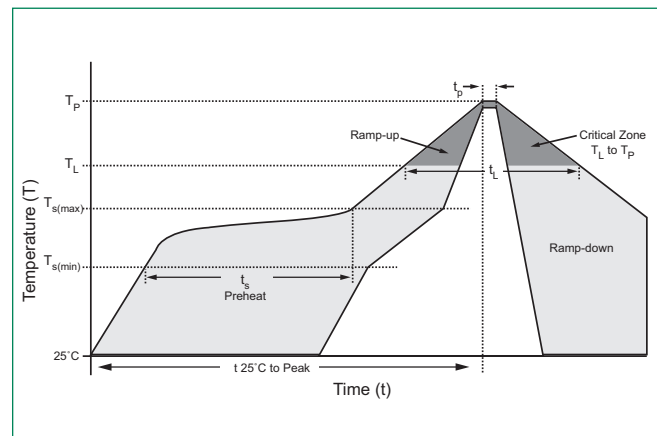
Figure 4 - Peak Power Derating



Please contact Littelfuse for reliability or FIT/MTBF data, the performance is subject to vary and depends on the end customers' application condition.

Soldering Parameters

Reflow Condition		Lead-free assembly
Pre Heat	- Temperature Min ($T_{s(min)}$)	150 $^{\circ}C$
	- Temperature Max ($T_{s(max)}$)	200 $^{\circ}C$
	- Time (min to max) (t_p)	60 – 120 seconds
Average Ramp Up Rate (Liquidus Temp (T_L) to Peak)		3 $^{\circ}C$ /second max
$T_{s(max)}$ to T_A - Ramp-up Rate		3 $^{\circ}C$ /second max
Reflow	- Temperature (T_L) (Liquidus)	217 $^{\circ}C$
	- Time (min to max) (T_s)	60 – 150 seconds
Peak Temperature (T_p)		250 $^{+0/-5}$ $^{\circ}C$
Time within 5 $^{\circ}C$ of Actual Peak Temperature (t_p)		30 seconds
Ramp-down Rate		6 $^{\circ}C$ /second max
Time 25 $^{\circ}C$ to Peak Temperature (T_p)		8 minutes max
Do Not Exceed		250 $^{\circ}C$



Physical Specifications

Weight	0.02 ounce, 0.57 grams
Case	UL recognized compound meeting flammability rating UL94 V-0
Terminal	Matte tin-plated leads, solderable per JESD22-B102

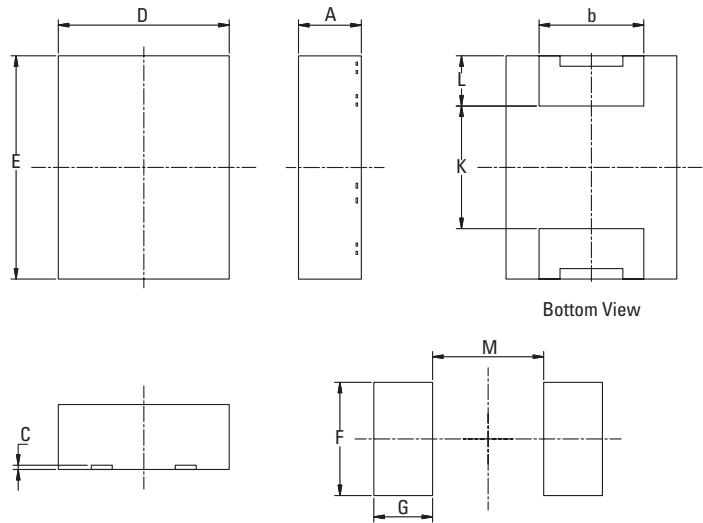
Environmental Specifications

High Temp Voltage Blocking (HTRB)	100 % DC reverse voltage rated 125 $^{\circ}C$, 1008 hours JEDEC, JESD22-A-108
Biased Temp & Humidity (H3TRB)	80 % breakdown voltage (+85 $^{\circ}C$) 85 %RH, 1008 hours JEDEC, JESD22-A-101
Unbiased Highly Accelerated Stress Test (UHAST)	96 hours at $T_A = 130^{\circ}C$ /85 %RH. JEDEC, JESD22-A-118
Temp Cycling (TC)	-55 $^{\circ}C$ to +125 $^{\circ}C$, 15 min. dwell, 1000 cycles. JEDEC, JESD22-A104
Moisture Sensitivity Level (MSL)	85 %RH, +85 $^{\circ}C$, 168 hours, 3 reflow cycles (+250 $^{\circ}C$ Peak). JEDEC, JEDEC-J-STD-020, Level 1
Resistance to Solder Heat (RSH)	+260 $^{\circ}C$, 30 seconds JEDEC, JEDEC JESD22-A-111

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Dimensions - DFN10*8*3

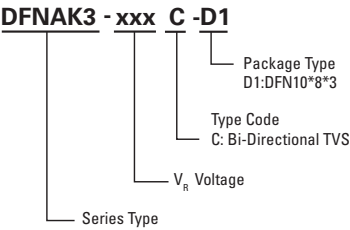


Recommended Soldering Pattern

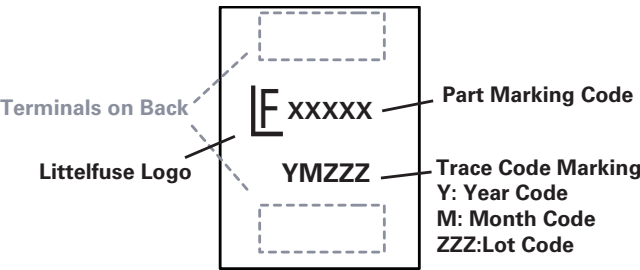
Dimensions	Millimeters		Inches	
	Min	Max	Min	Max
A	2.90	3.10	0.114	0.122
b	4.80	5.20	0.189	0.205
C	0.22	0.28	0.009	0.011
D	8.00	8.20	0.315	0.323
E	10.50	10.70	0.413	0.421
F	5.40 REF		0.213 REF	
G	2.80 REF		0.110 REF	
K	5.85 TYP		0.230 TYP	
L	2.20	2.60	0.087	0.102
M	5.30 REF		0.209 REF	

Dimensions are only for reference and might be changed later on. But the soldering pattern is fixed.

Part Numbering System



Part Marking System



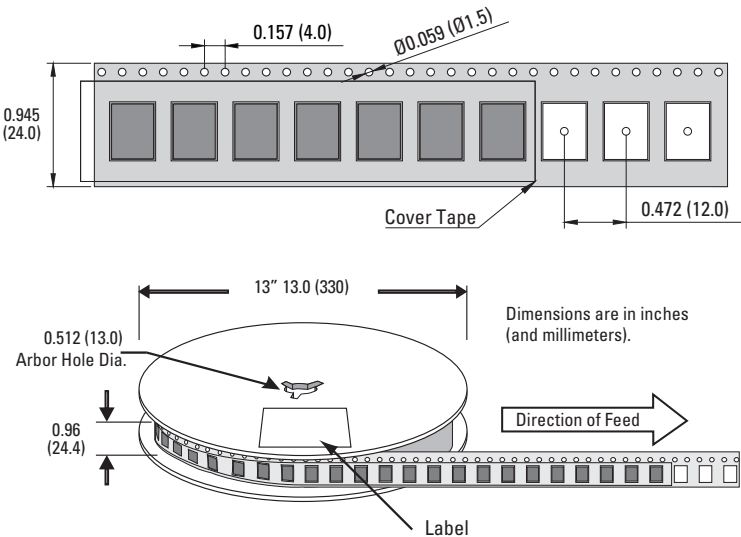
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Packing Option

Part Number	Component Package	Quantity	Packaging Option	Packaging Specification
DFNAK3-xxxX-D1	DFN10*8*3	1500	Tape & Reel -24 mm tape/13" reel	EIA STD RS-481

Tape and Reel Specification



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