

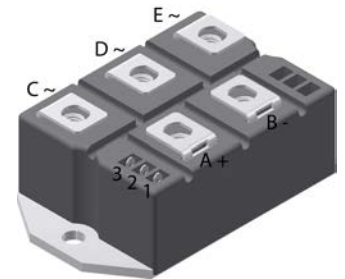
Thyristor Module

3~ Rectifier
$V_{RRM} = 1200\text{ V}$
$I_{DAV} = 120\text{ A}$
$I_{FSM} = 1050\text{ A}$

3~ Rectifier Bridge, half-controlled (high-side)

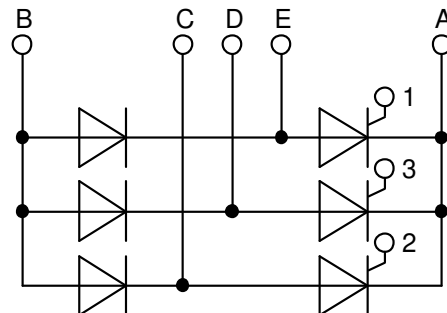
Part number

VVZ110-12io7



Backside: isolated

 E72873



Features / Advantages:

- Package with DCB ceramic base plate
- Improved temperature and power cycling
- Planar passivated chips
- Very low forward voltage drop
- Very low leakage current

Applications:

- Line rectifying 50/60 Hz
- Drives
- SMPS
- UPS

Package: PWS-E

- Isolation Voltage: 3000 V~
- Industry standard outline
- RoHS compliant
- Easy to mount with two screws
- Base plate: Copper internally DCB isolated
- Advanced power cycling

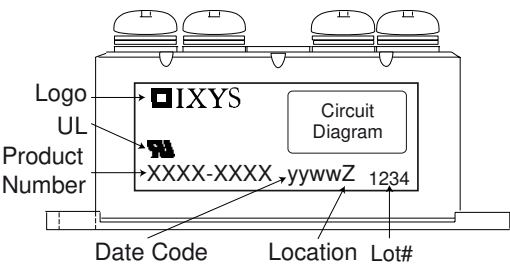
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Rectifier				Ratings			
Symbol	Definition	Conditions		min.	typ.	max.	Unit
$V_{RSM/DSM}$	<i>max. non-repetitive reverse/forward blocking voltage</i>	$T_{VJ} = 25^{\circ}\text{C}$				1300	V
$V_{RRM/DRM}$	<i>max. repetitive reverse/forward blocking voltage</i>	$T_{VJ} = 25^{\circ}\text{C}$				1200	V
$I_{R/D}$	<i>reverse current, drain current</i>	$V_{R/D} = 1200\text{ V}$	$T_{VJ} = 25^{\circ}\text{C}$			300	μA
		$V_{R/D} = 1200\text{ V}$	$T_{VJ} = 125^{\circ}\text{C}$			5	mA
V_T	<i>forward voltage drop</i>	$I_T = 40\text{ A}$	$T_{VJ} = 25^{\circ}\text{C}$			1,11	V
		$I_T = 120\text{ A}$				1,45	V
		$I_T = 40\text{ A}$	$T_{VJ} = 125^{\circ}\text{C}$			1,06	V
		$I_T = 120\text{ A}$				1,49	V
I_{DAV}	<i>bridge output current</i>	$T_C = 85^{\circ}\text{C}$ rectangular $d = \frac{1}{3}$	$T_{VJ} = 125^{\circ}\text{C}$			120	A
V_{T0}	<i>threshold voltage</i>	} <i>for power loss calculation only</i>	$T_{VJ} = 125^{\circ}\text{C}$			0,84	V
r_T	<i>slope resistance</i>					5,4	m Ω
R_{thJC}	<i>thermal resistance junction to case</i>					0,65	K/W
R_{thCH}	<i>thermal resistance case to heatsink</i>				0,15		K/W
P_{tot}	<i>total power dissipation</i>		$T_C = 25^{\circ}\text{C}$			150	W
I_{TSM}	<i>max. forward surge current</i>	$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}\text{C}$			1,05	kA
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$			1,14	kA
		$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 125^{\circ}\text{C}$			895	A
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$			965	A
I^2t	<i>value for fusing</i>	$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}\text{C}$			5,52	kA ² s
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$			5,36	kA ² s
		$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 125^{\circ}\text{C}$			4,01	kA ² s
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$			3,88	kA ² s
C_J	<i>junction capacitance</i>	$V_R = 400\text{ V}$ $f = 1\text{ MHz}$	$T_{VJ} = 25^{\circ}\text{C}$		46		pF
P_{GM}	<i>max. gate power dissipation</i>	$t_p = 30\text{ }\mu\text{s}$	$T_C = 125^{\circ}\text{C}$			10	W
		$t_p = 300\text{ }\mu\text{s}$				1	W
P_{GAV}	<i>average gate power dissipation</i>					0,5	W
$(di/dt)_{cr}$	<i>critical rate of rise of current</i>	$T_{VJ} = 125^{\circ}\text{C}; f = 50\text{ Hz}$ repetitive, $I_T = 120\text{ A}$				150	A/ μs
		$t_p = 200\text{ }\mu\text{s}; di_G/dt = 0,3\text{ A}/\mu\text{s};$ $I_G = 0,3\text{ A}; V_D = \frac{2}{3} V_{DRM}$ non-repet., $I_T = 40\text{ A}$				500	A/ μs
$(dv/dt)_{cr}$	<i>critical rate of rise of voltage</i>	$V_D = \frac{2}{3} V_{DRM}$ $R_{GK} = \infty$; method 1 (linear voltage rise)	$T_{VJ} = 125^{\circ}\text{C}$			1000	V/ μs
V_{GT}	<i>gate trigger voltage</i>	$V_D = 6\text{ V}$	$T_{VJ} = 25^{\circ}\text{C}$			1,5	V
			$T_{VJ} = -40^{\circ}\text{C}$			1,6	V
I_{GT}	<i>gate trigger current</i>	$V_D = 6\text{ V}$	$T_{VJ} = 25^{\circ}\text{C}$			100	mA
			$T_{VJ} = -40^{\circ}\text{C}$			200	mA
V_{GD}	<i>gate non-trigger voltage</i>	$V_D = \frac{2}{3} V_{DRM}$	$T_{VJ} = 125^{\circ}\text{C}$			0,2	V
I_{GD}	<i>gate non-trigger current</i>					5	mA
I_L	<i>latching current</i>	$t_p = 30\text{ }\mu\text{s}$	$T_{VJ} = 25^{\circ}\text{C}$			450	mA
		$I_G = 0,3\text{ A}; di_G/dt = 0,3\text{ A}/\mu\text{s}$					
I_H	<i>holding current</i>	$V_D = 6\text{ V}$ $R_{GK} = \infty$	$T_{VJ} = 25^{\circ}\text{C}$			200	mA
t_{gd}	<i>gate controlled delay time</i>	$V_D = \frac{1}{2} V_{DRM}$	$T_{VJ} = 25^{\circ}\text{C}$			2	μs
		$I_G = 0,3\text{ A}; di_G/dt = 0,3\text{ A}/\mu\text{s}$					
t_q	<i>turn-off time</i>	$V_R = 100\text{ V}; I_T = 40\text{ A}; V_D = \frac{2}{3} V_{DRM}$ $di/dt = 10\text{ A}/\mu\text{s}; dv/dt = 20\text{ V}/\mu\text{s}; t_p = 300\text{ }\mu\text{s}$	$T_{VJ} = 100^{\circ}\text{C}$		200		μs

Package PWS-E				Ratings			
Symbol	Definition	Conditions		min.	typ.	max.	Unit
I _{RMS}	<i>RMS current</i>	per terminal				250	A
T _{VJ}	<i>virtual junction temperature</i>			-40		125	°C
T _{op}	<i>operation temperature</i>			-40		100	°C
T _{stg}	<i>storage temperature</i>			-40		125	°C
Weight					284		g
M _D	<i>mounting torque</i>			4,25		5,75	Nm
M _T	<i>terminal torque</i>			4,25		5,75	Nm
d _{Spp/App}	<i>creepage distance on surface striking distance through air</i>		<i>terminal to terminal</i>	12,0			mm
<i>terminal to backside</i>			26,0			mm	
d _{Spb/Apb}							
V _{ISOL}	<i>isolation voltage</i>	t = 1 second	50/60 Hz, RMS; I _{ISOL} ≤ 1 mA	3000			V
		t = 1 minute		2500			V

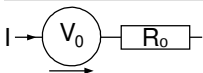


Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	VVZ110-12io7	VVZ110-12io7	Box	5	464902

Equivalent Circuits for Simulation

* on die level

$T_{VJ} = 125^{\circ}\text{C}$

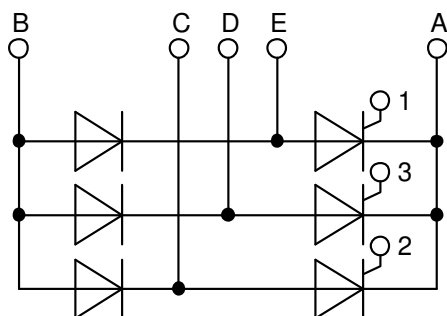
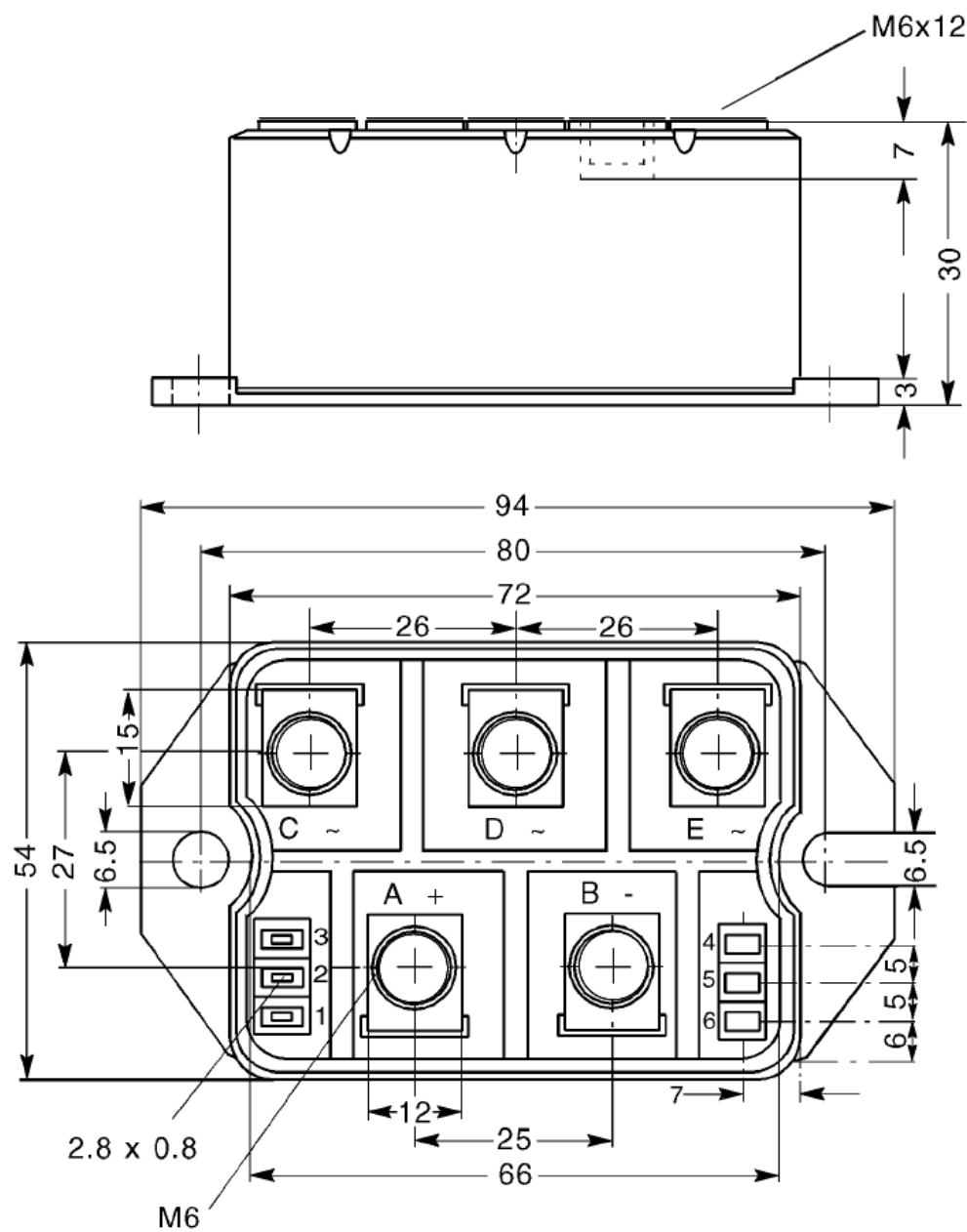


Thyristor

$V_{0\text{ max}}$
threshold voltage
0,84
V

$R_{0\text{ max}}$
*slope resistance **
4,3
mΩ

Outlines PWS-E



Thyristor

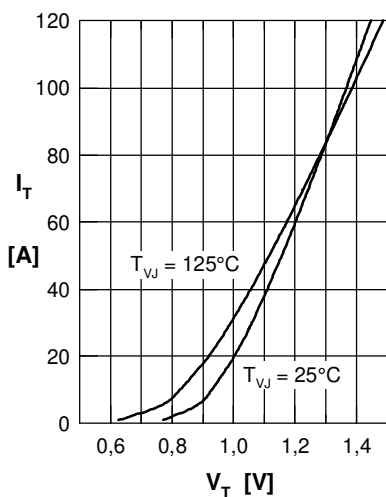


Fig. 1 Forward characteristics

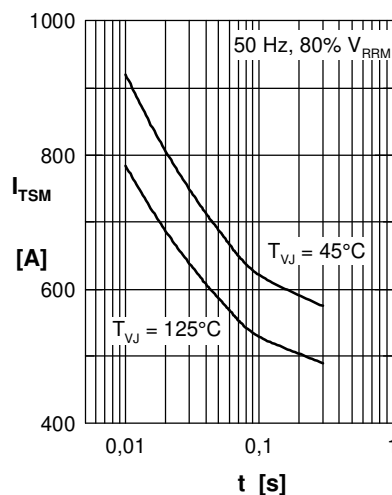


Fig. 2 Surge overload current
 I_{TSM} : crest value, t : duration

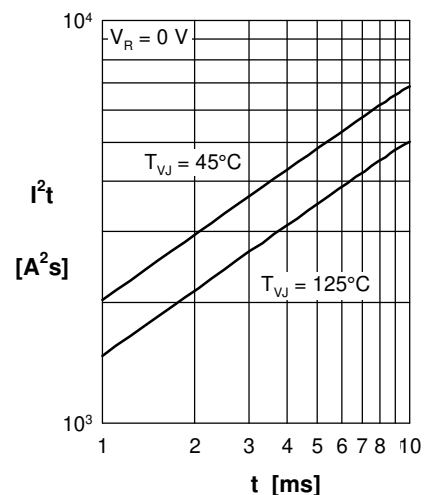


Fig. 3 I^2t versus time (1-10 s)

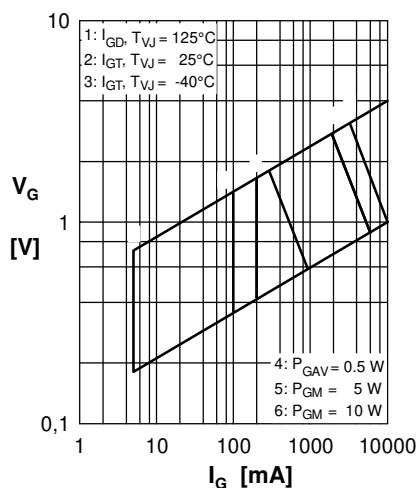


Fig. 4 Gate voltage & gate current

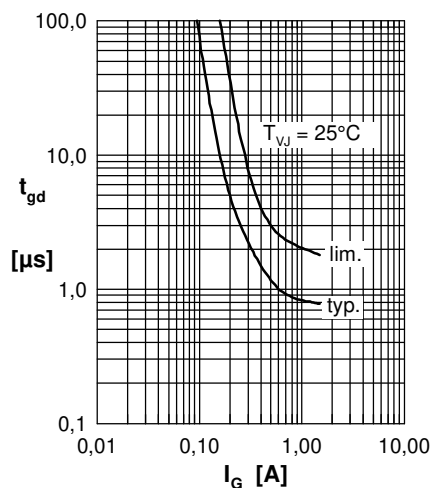


Fig. 5 Gate controlled delay time t_{gd}

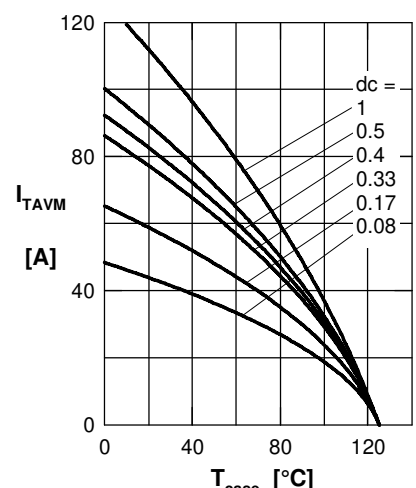


Fig. 6 Max. forward current at case temperature

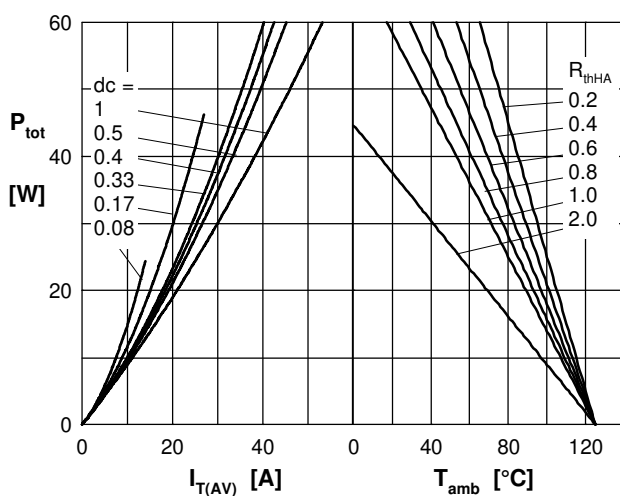


Fig. 7a Power dissipation versus direct output current
 Fig. 7b and ambient temperature

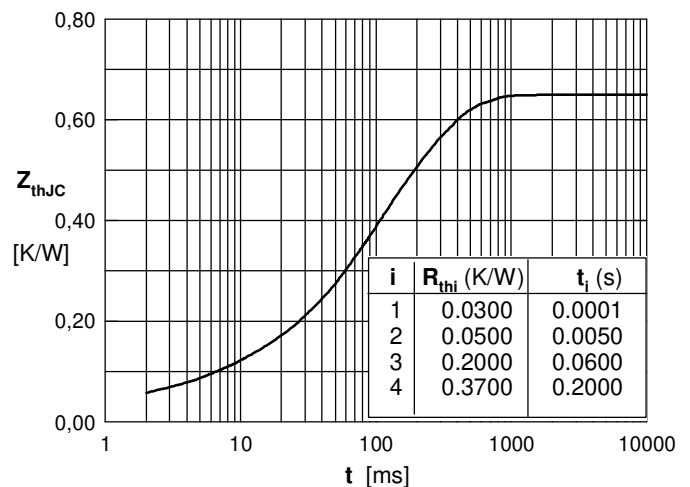


Fig. 8 Transient thermal impedance junction to case