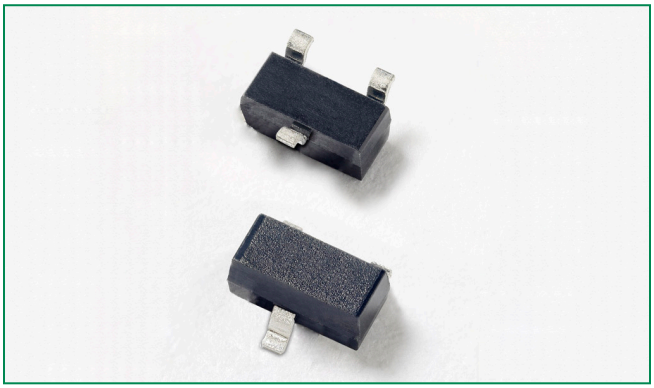
SP712 Series 640W Asymmetrical TVS Diode Array

HF RoHS Pb GREEN

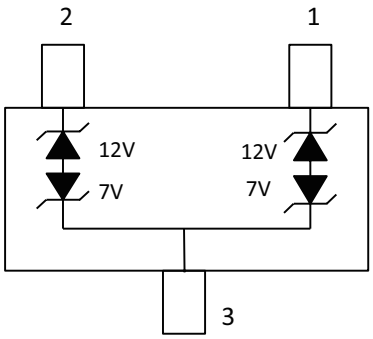


Description

The SP712 TVS Diode Array is designed to protect RS-485 applications with asymmetrical working voltages (-7V to 12V) from damage due to electrostatic discharge (ESD), electrical fast transients (EFT), and lightning induced surges.

The SP712 can absorb repetitive ESD strikes above the maximum level specified in IEC 61000-4-2 international standard without performance degradation and safely dissipate up to 20A of 8/20us induced surge current (IEC 61000-4-5) with very low clamping voltages.

Pinout and Functional Block Diagram



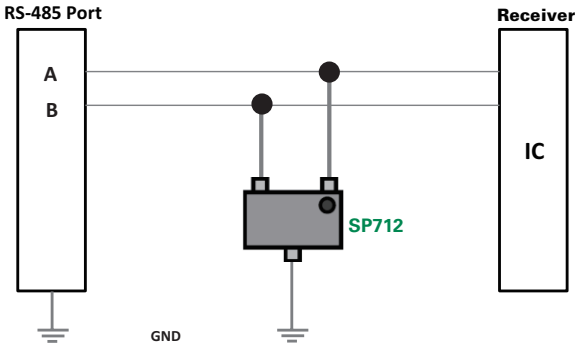
Features

- ESD, IEC 61000-4-2, ±30kV contact, ±30kV air
- EFT, IEC 61000-4-4, 50A (5/50ns)
- Lightning, IEC 61000-4-5 2nd edition, 20A (t_P=8/20μs)
- Working Voltages: -7V to 12V
- Low clamping voltage
- Low leakage current
- Halogen free, Lead free and RoHS compliant
- Moisture Sensitivity Level(MSL -1)
- AEC-Q101 qualified

Applications

- RS-485
- Fieldbus
- Modbus
- Profibus
- DMX512
- Security Systems
- Automated Teller Machines (ATMs)
- Lighting Control - DALI
- Communication Equipments

RS-485 Application Example



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TVS Diode Arrays (SPA® Diodes)
General Purpose ESD Protection - SP712

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
P_{Pk}	Peak Pulse Power (t_p=8/20µs)	640	W
I_{PP}	Peak Pulse Current (t_p=8/20µs)	20	A
T_{OP}	Operating Temperature	-40 to 125	°C
T_{STOR}	Storage Temperature	-55 to 150	°C

Notes:

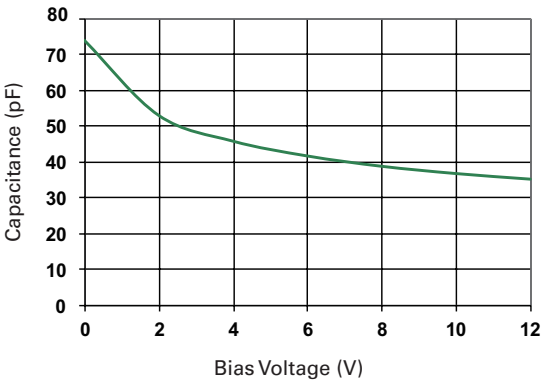
CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the component. This is a stress only rating and operation of the component at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics (T_{OP}=25°C)

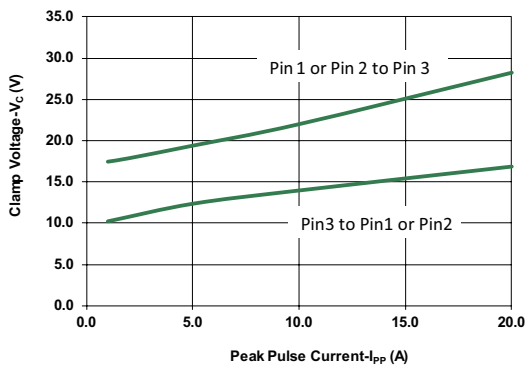
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	V_{RWM}	I_R=1µA, Pin 3 to Pin 1 or Pin 2			7.0	V
		I_R=1µA, Pin 1 or Pin 2 to Pin 3			12.0	V
Breakdown Voltage	V_{BR}	I_R=1mA, Pin 3 to Pin 1 or Pin 2	7.5	9		V
		I_R=1mA, Pin 1 or Pin 2 to Pin 3	13.3	14.5		V
Reverse Leakage Current	I_{LEAK}	V_R=7V			20	µA
		V_R=12V			1	µA
Clamp Voltage[1]	V_C	I_{PP}=1A, t_p=8/20µs, Pin 1 or Pin 2 to Pin 3		17	19	V
		I_{PP}=1A, t_p=8/20µs, Pin 3 to Pin 1 or Pin 2		10	11	V
		I_{PP}=20A, t_p=8/20µs, Pin 1 or Pin 2 to Pin 3		28	32	V
		I_{PP}=20A, t_p=8/20µs, Pin 3 to Pin 1 or Pin 2		17	20	V
Dynamic Resistance[2]	R_{DYN}	TLP, t_P=100ns		0.26		Ω
ESD Withstand Voltage[1]	V_{ESD}	IEC 61000-4-2 (Contact Discharge)	±30			kV
		IEC 61000-4-2 (Air Discharge)	±30			kV
Diode Capacitance[1]	$C_{I/O-GND}$	Reverse Bias=0V, f=1MHz; Pin 1 or Pin 2 to Pin 3			75	pF

Notes : 1. Parameter is guaranteed by design and/or component characterization.
2 Transmission Line Pulse (TLP) test setting : Std.TDR(50Ω),tp=100ns, tr=0.2ns ITLP and VTLP averaging window: start t1=70ns to end t2=90ns

Capacitance vs. Reverse Bias



Clamping Voltage vs. I_{PP}



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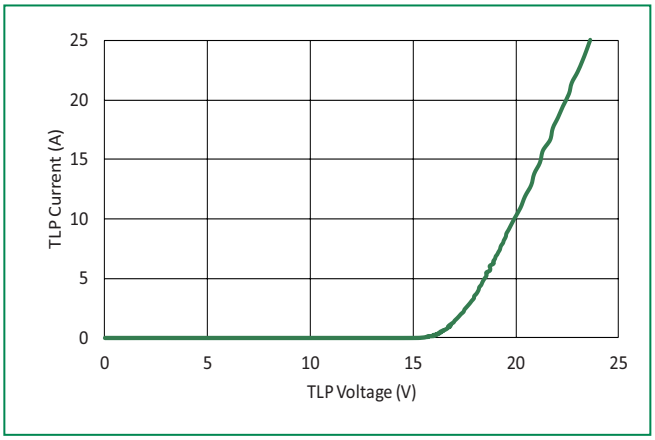
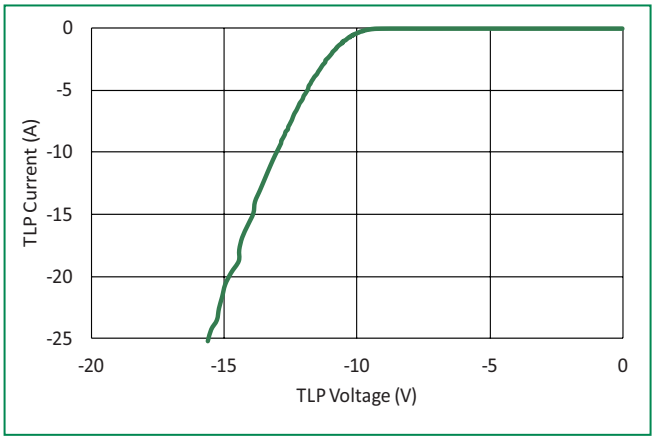
TVS Diode Arrays (SPA® Diodes)

General Purpose ESD Protection - SP712

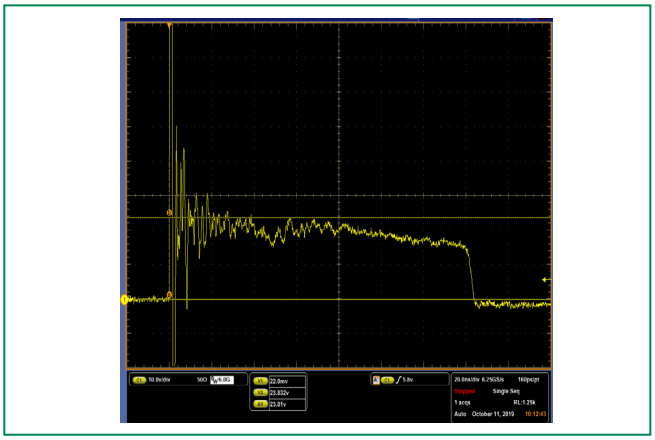
Positive Transmission Line Pulsing (TLP) Plot



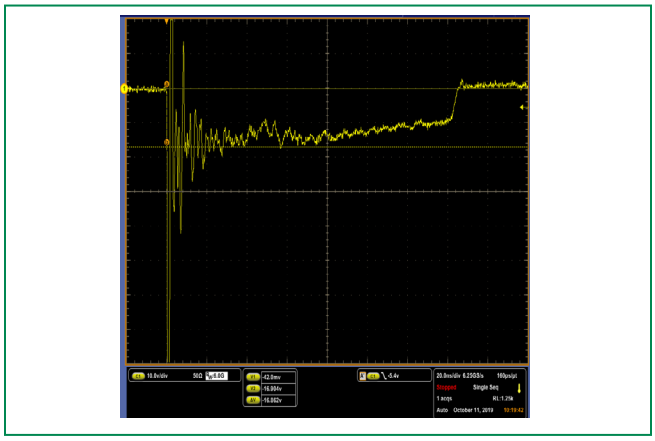
Negative Transmission Line Pulsing (TLP) Plot



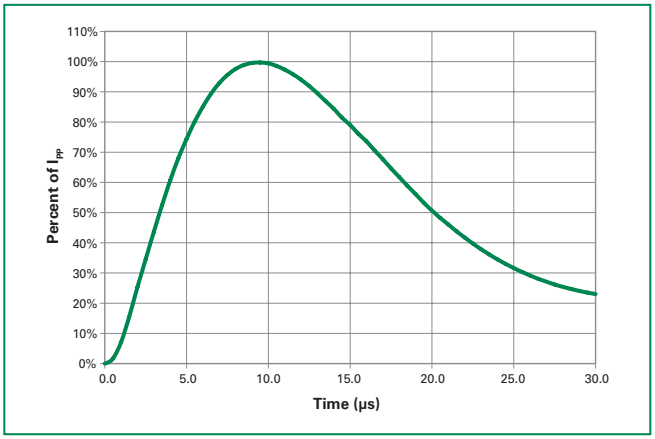
IEC 61000-4-2 +8kV Contact ESD Clamping Voltage



IEC 61000-4-2 -8kV Contact ESD Clamping Voltage



8/20µs Pulse Waveform



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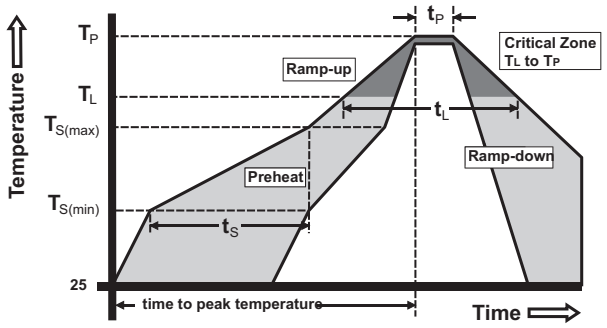
TVS Diode Arrays (SPA® Diodes)

General Purpose ESD Protection - SP712

Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	- Temperature Min ($T_{s(min)}$)	150°C
	- Temperature Max ($T_{s(max)}$)	200°C
	- Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	- Temperature (T_L) (Liquidus)	217°C
	- Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Part Marking System

AE : Part code
F : Assembly code
D : Date code

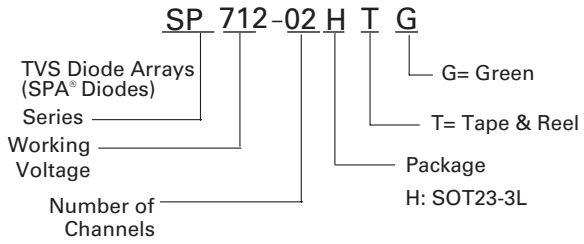
Product Characteristics

Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.004 inches(0.102mm)
Substrate Material	Silicon
Body Material	Molded Compound
Flammability	UL Recognized compound meeting flammability rating V-0

Ordering Information

Part Number	Package	Min. Order Qty.
SP712-02HTG	SOT23-3L	3000

Part Numbering System



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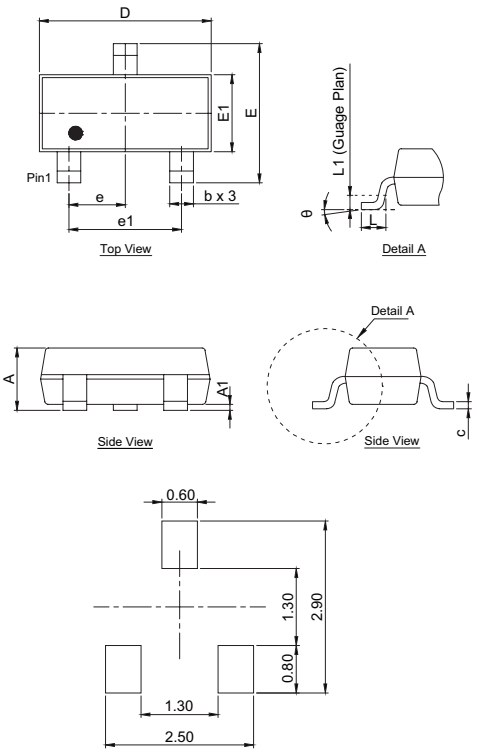
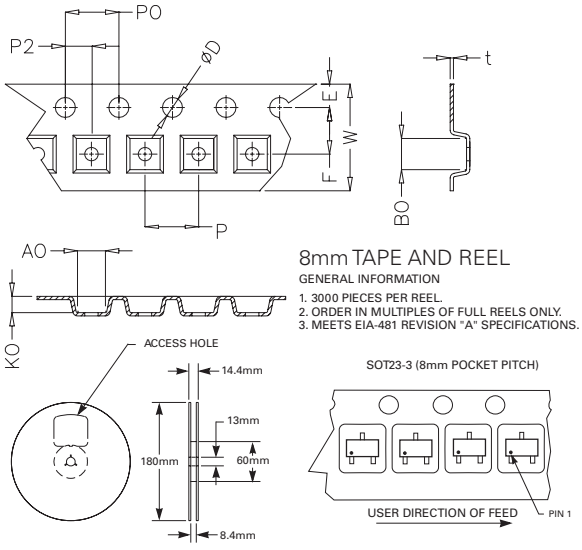
Package Dimensions — SOT23-3



Recommended soldering pad layout (unit :mm)
Drawing# : H03-B

Package	SOT23-3			
Pins	3			
JEDEC	TO-236			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.90	1.15	0.035	0.045
A1	0.00	0.10	0.000	0.004
b	0.30	0.51	0.012	0.020
c	0.08	0.20	0.003	0.008
D	2.80	3.04	0.110	0.120
E	2.10	2.64	0.083	0.104
E1	1.20	1.40	0.047	0.055
e	0.95 BSC		0.038 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.55	0.012	0.022
L1	0.25 BSC		0.010 BSC	
θ	0°	8°	0°	8°

Embossed Carrier Tape & Reel Specification — SOT23-3



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	3.40	3.60	0.134	0.142
P2	1.90	2.10	0.075	0.083
D	1.40	1.60	0.055	0.063
P0	3.90	4.10	0.154	0.161
W	7.70	8.30	0.303	0.327
P	3.90	4.10	0.154	0.161
A0	3.05	3.25	0.120	0.128
B0	2.67	2.87	0.105	0.113
K0	1.12	1.32	0.044	0.052
t	0.22	0.24	0.009	0.009

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