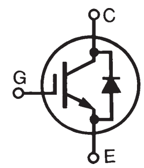
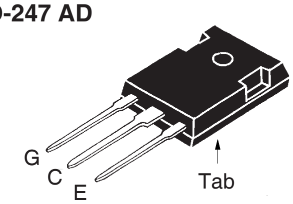
High Voltage, High Gain BIMOSFET™ Monolithic Bipolar MOS Transistor

IXBH42N250

V_{CES} = 2500V
I_{C110} = 42A
$V_{CE(sat)}$ ≤ 3.0V



TO-247 AD



G = Gate C = Collector
E = Emitter Tab = Collector

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_C = 25°C to 150°C	2500	V
V_{CGR}	T_J = 25°C to 150°C, R_{GE} = 1MΩ	2500	V
V_{GES}	Continuous	± 25	V
V_{GEM}	Transient	± 35	V
I_{C25}	T_C = 25°C	104	A
I_{C110}	T_C = 110°C	42	A
I_{CM}	T_C = 25°C, 1ms	400	A
SSOA (RBSOA)	V_{GE} = 15V, T_{VJ} = 125°C, R_G = 20Ω Clamped Inductive Load	I_{CM} = 84 1250	A V
T_{SC} (SCSOA)	V_{GE} = 15V, T_J = 125°C, R_G = 82Ω, V_{CE} = 1250V, Non-Repetitive	10	µs
P_C	T_C = 25°C	500	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	°C
M_d	Mounting Torque	1.13/10	Nm/lb.in
Weight		6	g

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{CES}	I_C = 1mA, V_{GE} = 0V	2500			V
$V_{GE(th)}$	I_C = 1mA, V_{CE} = V_{GE}	3.0		5.0	V
I_{CES}	V_{CE} = 0.8 • V_{CES}, V_{GE} = 0V			50	µA
	T_J = 125°C		250		µA
I_{GES}	V_{CE} = 0V, V_{GE} = ± 25V			±200	nA
$V_{CE(sat)}$	I_C = 42A, V_{GE} = 15V, Note 1		2.5	3.0	V
	T_J = 125°C		3.1		V

Features

- High Blocking Voltage
- International Standard Package
- Anti-Parallel Diode
- Low Conduction Losses

Advantages

- Low Gate Drive Requirement
- High Power Density

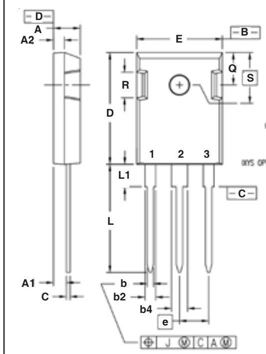
Applications

- Switch-Mode and Resonant-Mode Power Supplies
- Uninterruptible Power Supplies (UPS)
- Laser Generators
- Capacitor Discharge Circuits
- AC Switches

IXYS IXBH42N250

Symbol	Test Conditions ($T_J = 25°C$ Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
g_{fS}	$I_C = 42A$, $V_{CE} = 10V$, Note 1	28	45		S
C_{ies}	$V_{CE} = 25V$, $V_{GE} = 0V$, f = 1MHz		4780		pF
C_{oes}			170		pF
C_{res}			56		pF
R_{Gi}	Gate Input Resistance		3.0		Ω
Q_g	$I_C = 42A$, $V_{GE} = 15V$, $V_{CE} = 1000V$		200		nC
Q_{ge}			28		nC
Q_{gc}			75		nC
$t_{d(on)}$	**Resistive Switching Times, $T_J = 25°C$**		72		ns
t_r	$I_C = 42A$, $V_{GE} = 15V$		330		ns
$t_{d(off)}$	$V_{CE} = 1250V$, $R_G = 20Ω$		445		ns
t_f			610		ns
$t_{d(on)}$	**Resistive Switching Times, $T_J = 125°C$**		72		ns
t_r	$I_C = 42A$, $V_{GE} = 15V$		580		ns
$t_{d(off)}$	$V_{CE} = 1250V$, $R_G = 20Ω$		460		ns
t_f			490		ns
R_{thJC}				0.25	°C/W
R_{thCS}			0.21		°C/W

TO-247 (IXBH) Outline



1 - Gate
2,4 - Collector
3 - Emitter

Dim.	Millimeter min	max	Inches min	max
A	4.70	5.30	0.185	0.209
A1	2.21	2.59	0.087	0.102
A2	1.50	2.49	0.059	0.098
b	0.99	1.40	0.039	0.055
b2	1.65	2.39	0.065	0.094
b4	2.59	3.43	0.102	0.135
c	0.38	0.89	0.015	0.035
D	20.79	21.45	0.819	0.845
D1	13.07	-	0.515	-
D2	0.51	1.35	0.020	0.053
E	15.48	16.24	0.610	0.640
E1	13.45	-	0.53	-
E2	4.31	5.48	0.170	0.216
e	5.45 BSC		0.215 BSC	
L	19.80	20.30	0.078	0.800
L1	-	4.49	-	0.177
Ø P	3.55	3.65	0.140	0.144
Ø P1	-	7.39	-	0.290
Q	5.38	6.19	0.212	0.244
S	6.14 BSC		0.242 BSC	

Reverse Diode

Symbol	Test Conditions ($T_J = 25°C$ Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max	
V_F	$I_F = 42A$, $V_{GE} = 0V$, Note 1			2.5	V
t_{rr}	$I_F = 21A$, $V_{GE} = 0V$, $-di_F/dt = 100A/μs$		1.7		μs
I_{RM}	$V_R = 100V$, $V_{GE} = 0V$		43		A

Note 1. Pulse test, t < 300μs, duty cycle, d < 2%.

ADVANCE TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

Fig. 1. Output Characteristics @ T_J = 25ºC

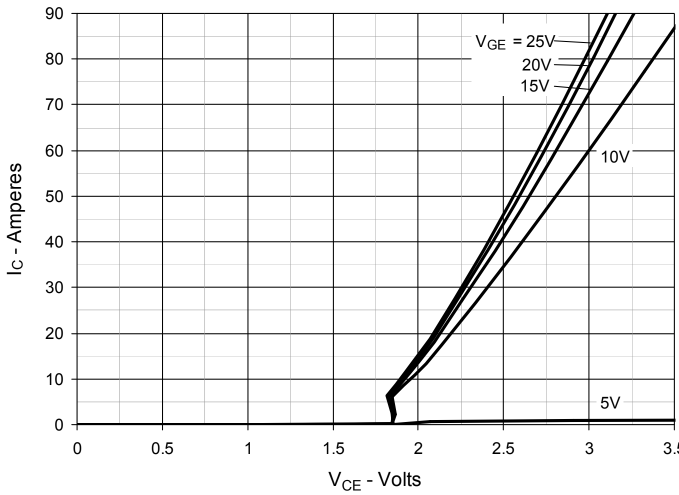


Fig. 2. Extended Output Characteristics @ T_J = 25ºC

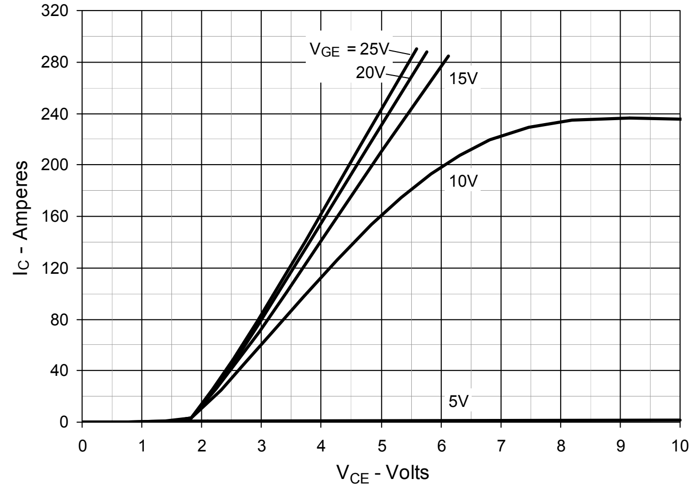


Fig. 3. Output Characteristics @ T_J = 125ºC

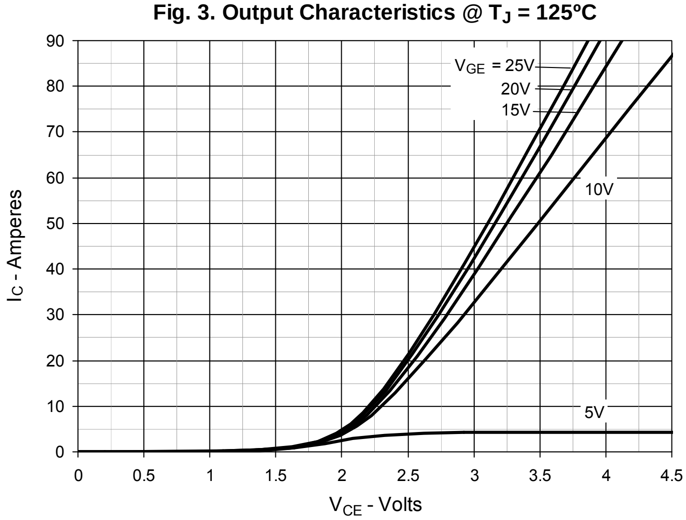


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

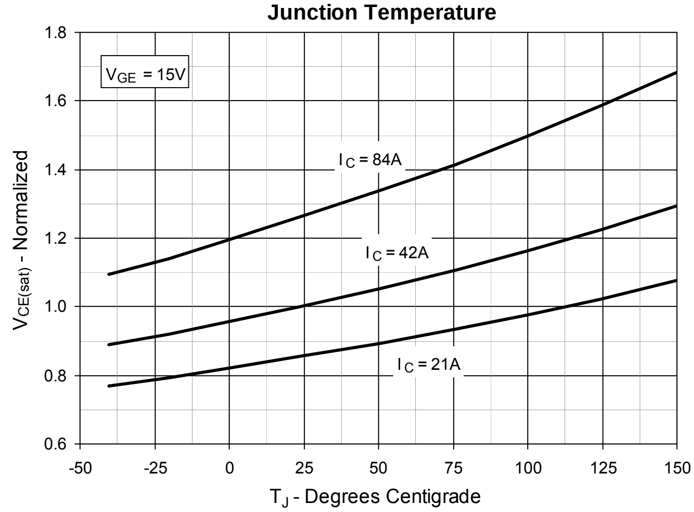


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

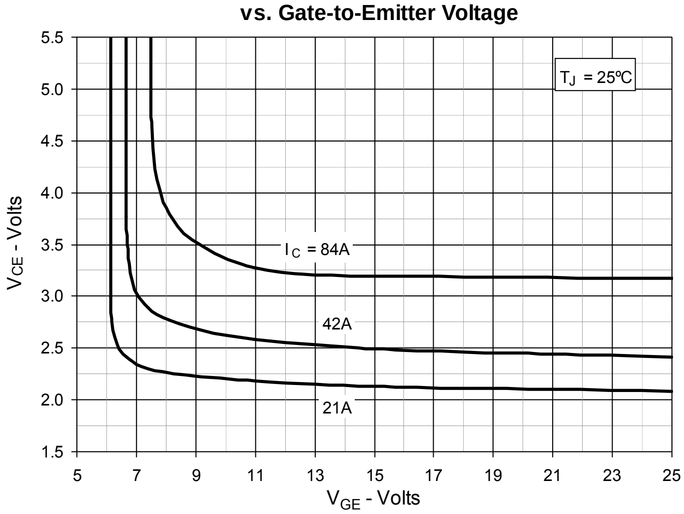


Fig. 6. Input Admittance

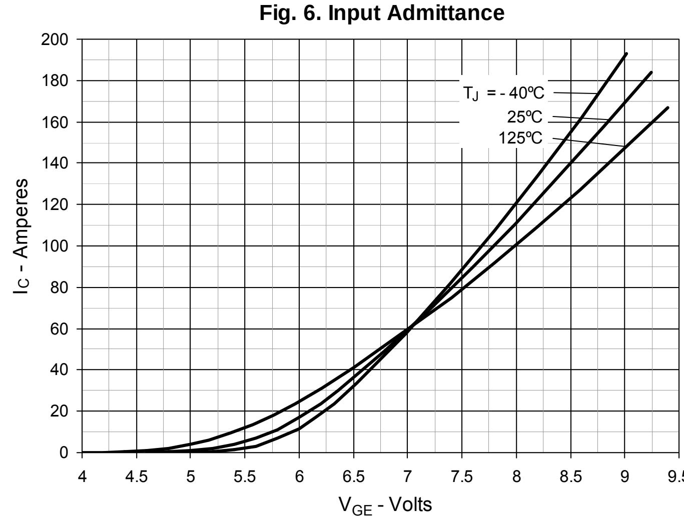


Fig. 7. Transconductance

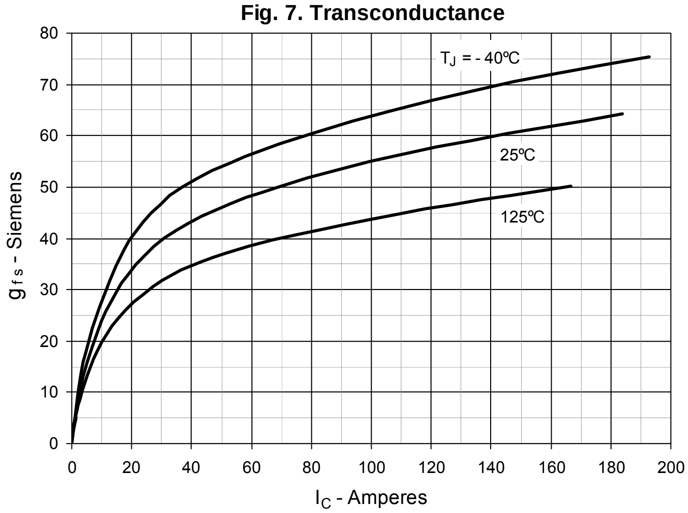


Fig. 8. Forward Voltage Drop of Intrinsic Diode

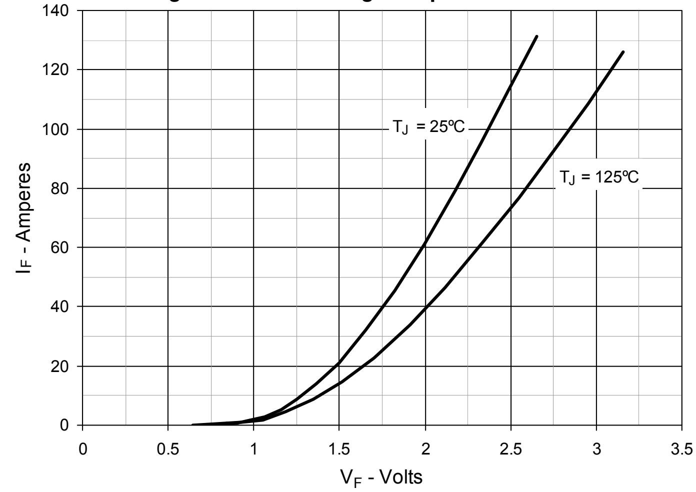


Fig. 9. Gate Charge

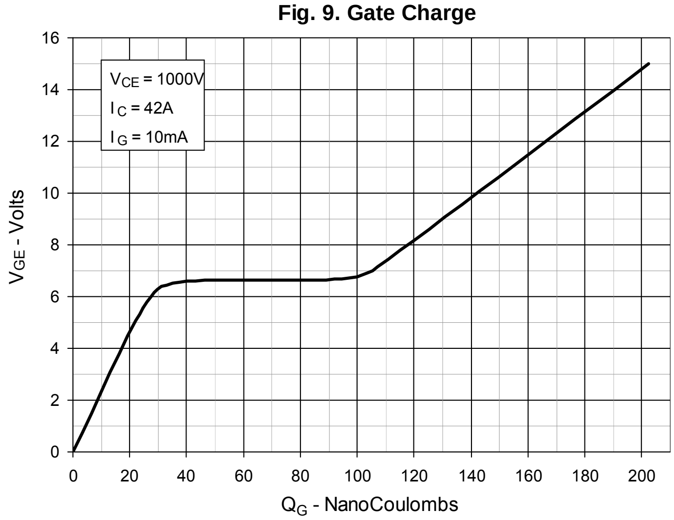


Fig. 10. Capacitance

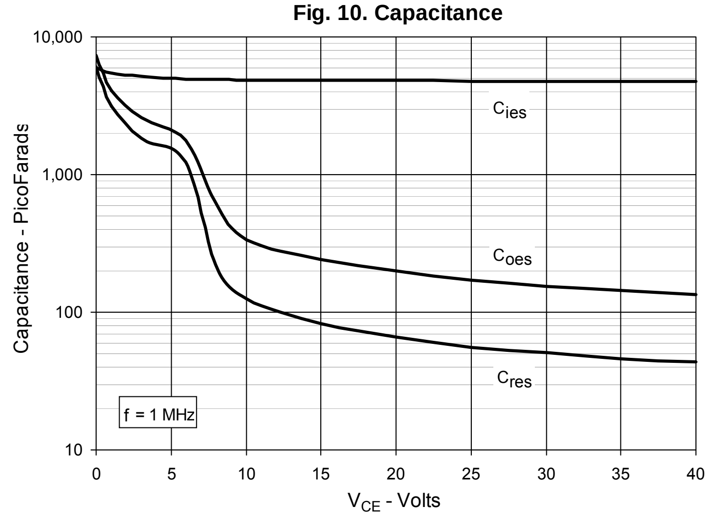


Fig. 11. Reverse-Bias Safe Operating Area

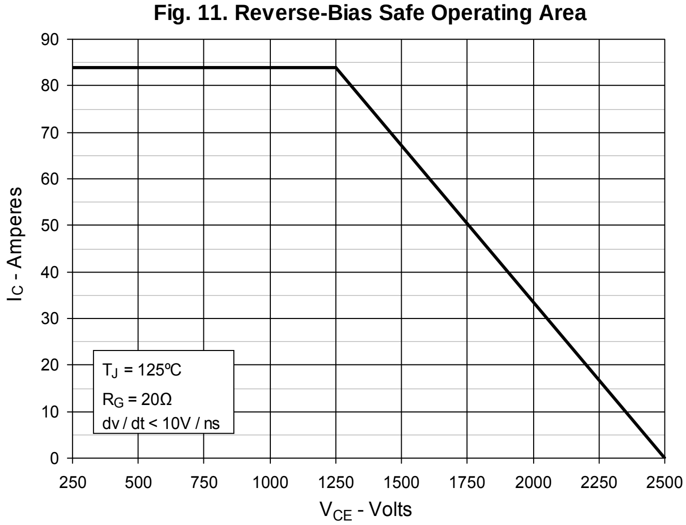


Fig. 12. Maximum Transient Thermal Impedance

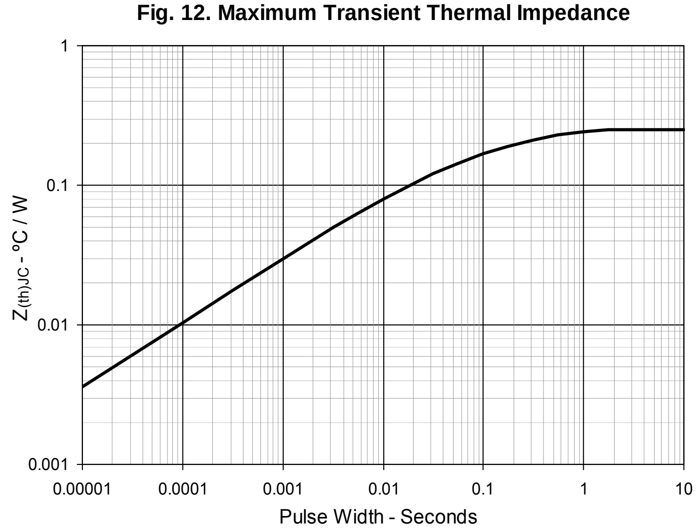


Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

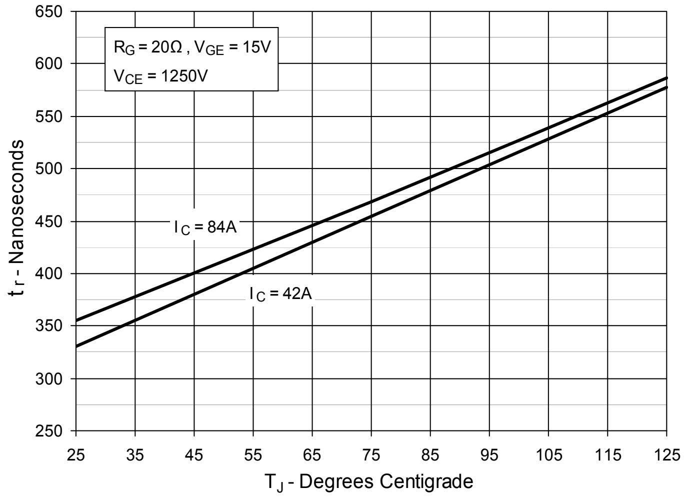


Fig. 14. Resistive Turn-on Rise Time vs. Collector Current

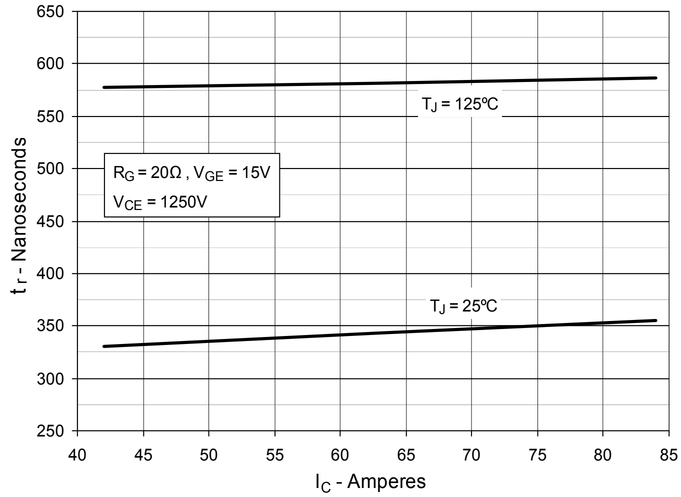


Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

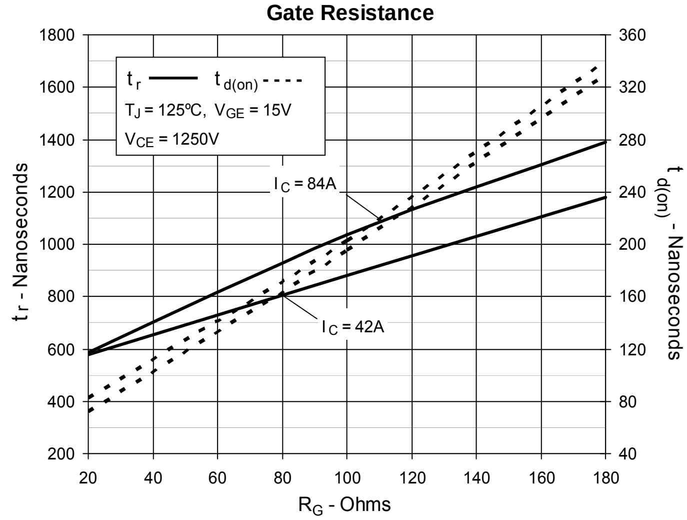


Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

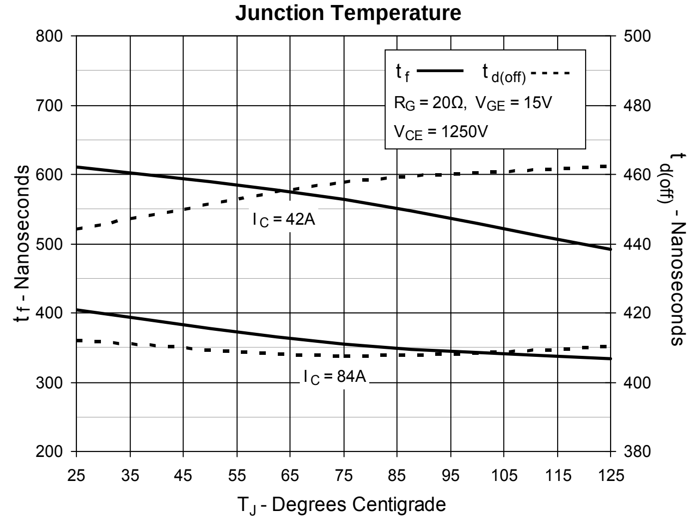


Fig. 17. Resistive Turn-off Switching Times vs. Collector Current

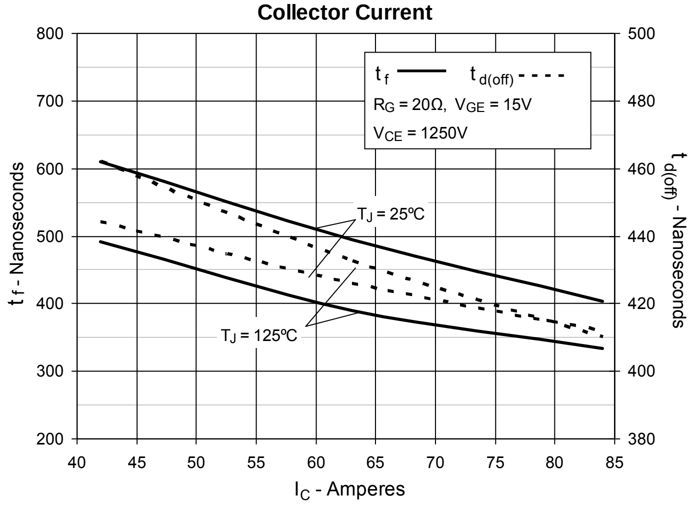


Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance

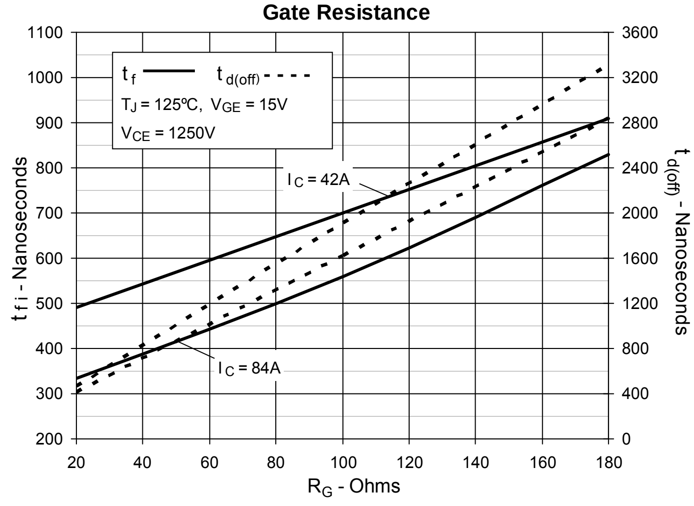


Fig. 19. Forward-Bias Safe Operating Area @ T_C = 25ºC

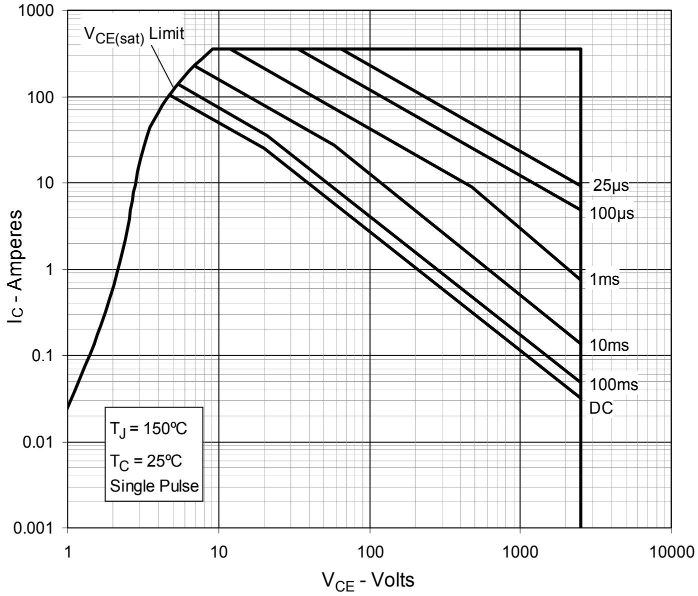


Fig. 20. Forward-Bias Safe Operating Area @ T_C = 115ºC