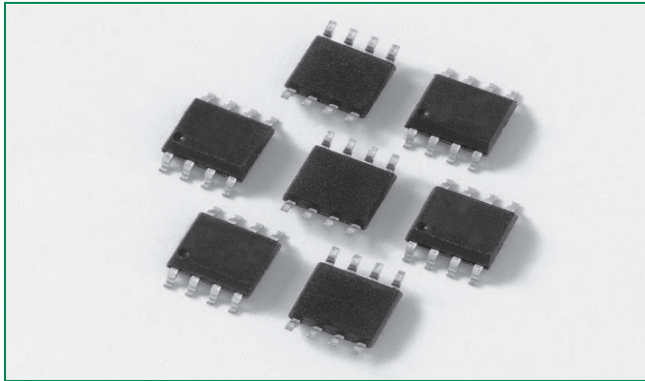
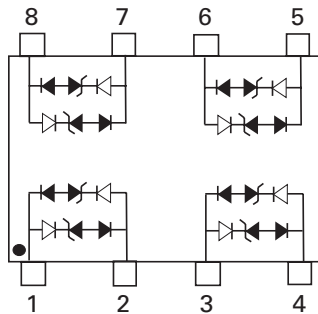


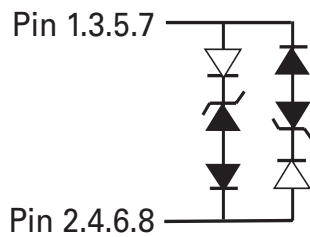
## SLVU2.8-8 Series 2.8V 30A TVS Array



### Pinout



### Functional Block Diagram



### Description

The SLVU2.8-8 was designed to protect low voltage, CMOS devices from ESD and lightning induced transients. There is a compensating diode in series with each low voltage TVS to present a low loading capacitance to the line being protected. These robust structures can safely absorb repetitive ESD strikes at  $\pm 30\text{kV}$  (contact discharge) per IEC 61000-4-2 standard and can safely dissipate up to 30A (IEC 61000-4-5 2nd Edition,  $t_p=8/20\mu\text{s}$ ) with very low clamping voltages.

### Features

- ESD, IEC 61000-4-2,  $\pm 30\text{kV}$  contact,  $\pm 30\text{kV}$  air
- EFT, IEC 61000-4-4, 40A (5/50ns)
- Lightning, IEC 61000-4-5 2nd Edition, 30A (8/20 $\mu\text{s}$ )
- Low capacitance of 2.6pF per line
- Low leakage current of 0.1 $\mu\text{A}$  (MAX) at 2.8V
- SOIC-8 (JEDEC MO-012) pin configuration allows for protection of all 4 differential pair for 1GbE
- RoHS Compliant and Lead Free
- Moisture Sensitivity Level (MSL-1)

### Applications

- 10/100/1000 Ethernet
- WAN/LAN Equipment
- Switching Systems
- Desktops, Servers, and Notebooks
- Analog Inputs
- Base Stations

### Additional Information



Datasheet



Resources



Samples

### Absolute Maximum Ratings

Parameter	Rating	Units
Peak Pulse Power ( $t_p=8/20\mu s$ )	750	W
Peak Pulse Current ( $t_p=8/20\mu s$ )	30	A
Operating Temperature	-40 to 125	°C
Storage Temperature	-55 to 150	°C

### Thermal Information

Parameter	Rating	Units
Storage Temperature Range	-55 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s)	260	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

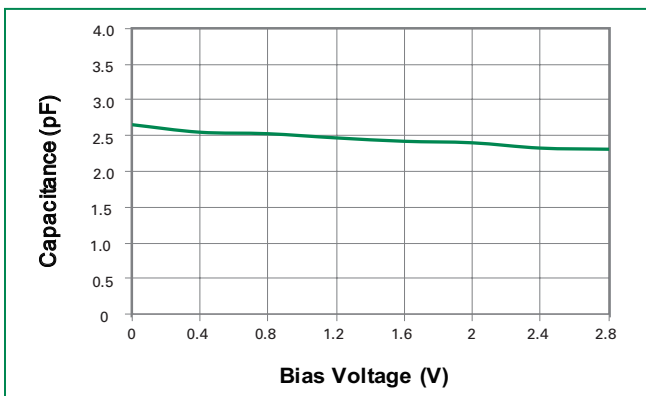
### Electrical Characteristics ( $T_{op} = 25^\circ C$ )

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	$V_{RWM}$	$I_r \leq 1\mu A$ (Each Line)			2.8	V
Reverse Breakdown Voltage	$V_{BR}$	$I_r = 2\mu A$ (Each Line)	3.0			V
Snapback Voltage	$V_{SB}$	$I_{SB} = 50mA$	2.8			V
Reverse Leakage Current	$I_{LEAK}$	$V_r = 2.8V$ (Each Line)			0.1	$\mu A$
Clamping Voltage <sup>1</sup>	$V_C$	$I_{PP} = 5A, t_p = 8/20\mu s$ (Each Line)			8.5	V
		$I_{PP} = 24A, t_p = 8/20\mu s$ (Each Line)			17	
ESD Withstand Voltage <sup>1</sup>	$V_{ESD}$	IEC61000-4-2 (Contact)	$\pm 30$			kV
		IEC61000-4-2 (Air)	$\pm 30$			
Dynamic Resistance <sup>2</sup>	$R_{DYN}$	TLP $t_p = 100ns$ , (Each Line)		0.3		$\Omega$
Diode Capacitance <sup>1</sup>	$C_D$	$V_r = 0V, f = 1MHz$ (Each Line)		2.6	3.0	pF

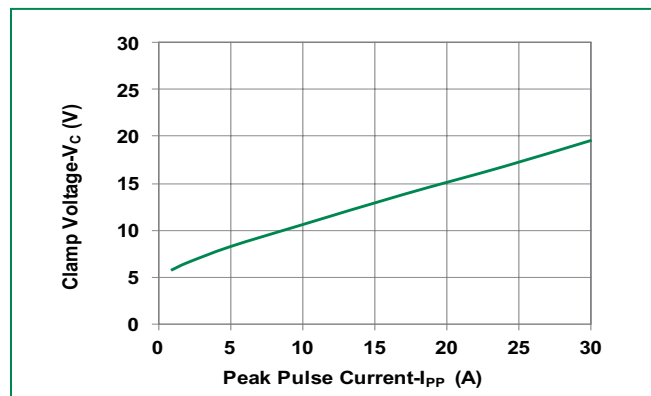
Note: 1 Parameter is guaranteed by design and/or device characterization.

2 Transmission Line Pulse (TLP) test setting : Std.TDR(50 $\Omega$ ),  $t_p = 100ns$ ,  $t_r = 0.2ns$  ITLP and VTLP averaging window: star  $t_1 = 70ns$  to end  $t_2 = 80ns$

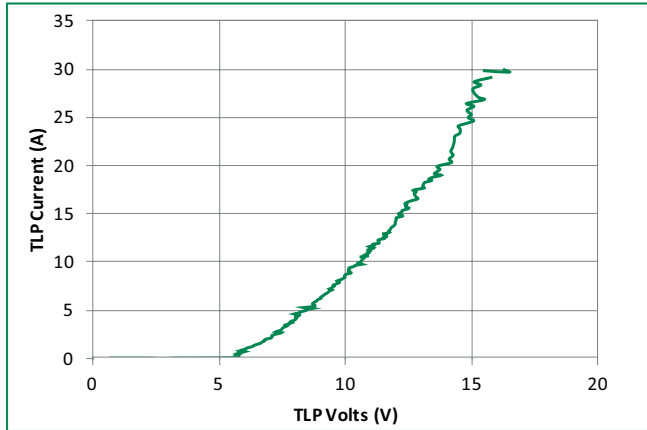
### Capacitance vs. Reverse Bias (Each line)



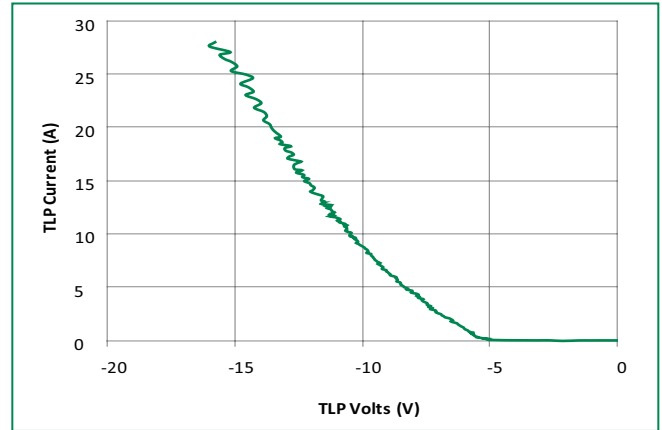
### Clamping Voltage vs. Peak Pulse Current (Each line)



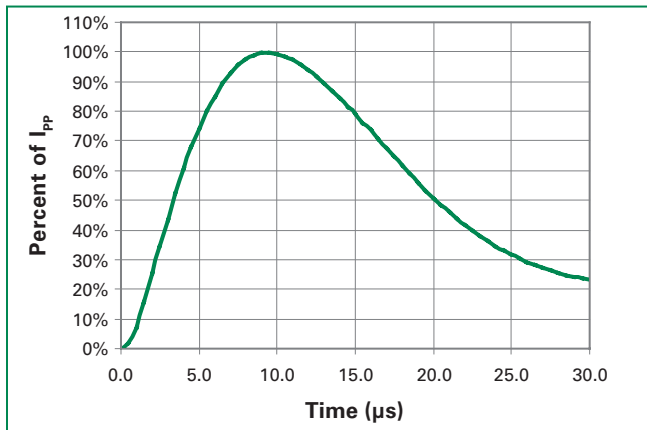
**Positive Transmission Line Pulsing (TLP) Plot (Each line)**



**Negative Transmission Line Pulsing (TLP) Plot (Each line)**



**8/20 μs Pulse Waveform**



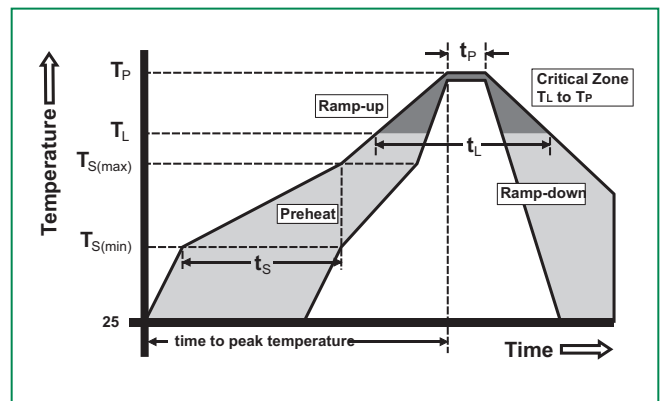
**Product Characteristics**

<b>Lead Plating</b>	Matte Tin
<b>Lead Material</b>	Copper Alloy
<b>Lead Coplanarity</b>	0.0004 inches (0.102mm)
<b>Substrate material</b>	Silicon
<b>Body Material</b>	V-0 per UL 94 Molded Epoxy

- Notes :
1. All dimensions are in millimeters
  2. Dimensions include solder plating.
  3. Dimensions are exclusive of mold flash & metal burr.
  4. All specifications comply to JEDEC SPEC MO-203 Issue A
  5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
  6. Package surface matte finish VDI 11-13.

**Soldering Parameters**

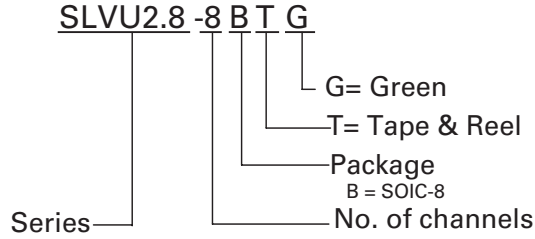
Reflow Condition		Pb – Free assembly
Pre Heat	- Temperature Min ( $T_{s(min)}$ )	150°C
	- Temperature Max ( $T_{s(max)}$ )	200°C
	- Time (min to max) ( $t_s$ )	60 – 180 secs
Average ramp up rate (Liquidus) Temp ( $T_L$ ) to peak		5°C/second max
$T_{s(max)}$ to $T_L$ - Ramp-up Rate		5°C/second max
Reflow	- Temperature ( $T_L$ ) (Liquidus)	217°C
	- Temperature ( $t_L$ )	60 – 150 seconds
Peak Temperature ( $T_p$ )		260 <sup>+0/-5</sup> °C
Time within 5°C of actual peak Temperature ( $t_p$ )		20 – 40 seconds
Ramp-down Rate		5°C/second max
Time 25°C to peak Temperature ( $T_p$ )		8 minutes Max.
Do not exceed		260°C



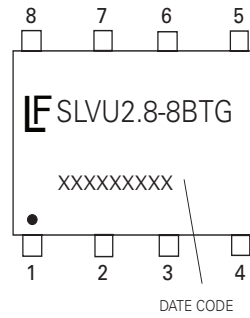
**Ordering Information**

Part Number	Package	Min. Order Qty.
SLVU2.8-8BTG	SOIC-8	2500

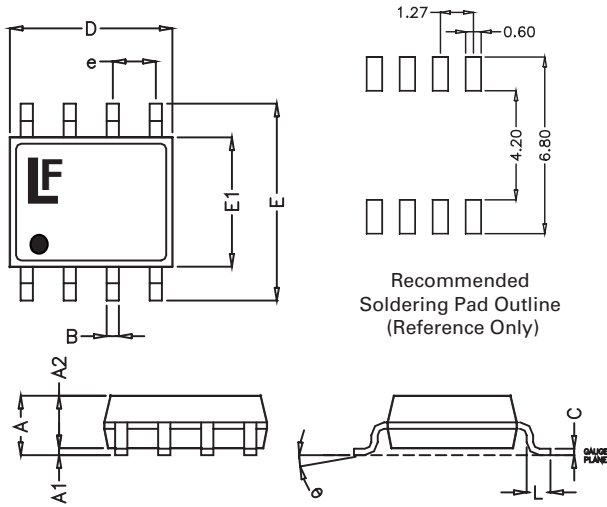
**Part Numbering System**



**Part Marking System**

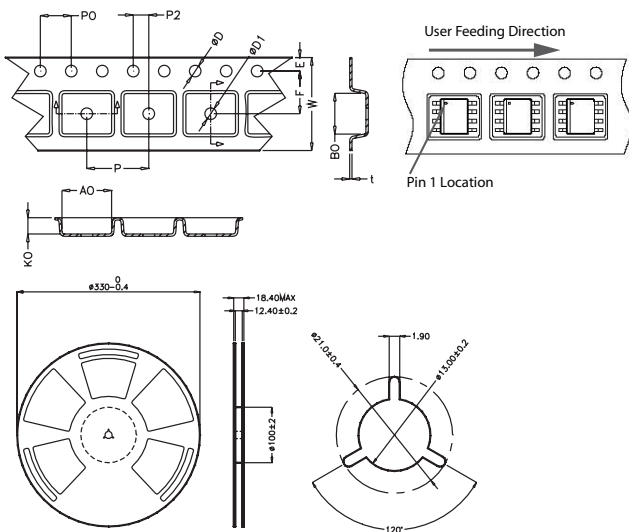


**Package Dimensions – Mechanical Drawings and Recommended Solder Pad Outline**



Package	SOIC-8			
Pins	8			
JEDEC	MS-012			
	Millimetres		Inches	
	Min	Max	Min	Max
<b>A</b>	1.35	1.75	0.053	0.069
<b>A1</b>	0.10	0.25	0.004	0.010
<b>A2</b>	1.25	1.65	0.050	0.065
<b>B</b>	0.31	0.51	0.012	0.020
<b>c</b>	0.17	0.25	0.007	0.010
<b>D</b>	4.80	5.00	0.189	0.197
<b>E</b>	5.80	6.20	0.228	0.244
<b>E1</b>	3.80	4.00	0.150	0.157
<b>e</b>	1.27 BSC		0.050 BSC	
<b>L</b>	0.40	1.27	0.016	0.050

**Embossed Carrier Tape & Reel Specification – SOIC Package**



Symbol	Millimetres		Inches	
	Min	Max	Min	Max
<b>E</b>	1.65	1.85	0.065	0.073
<b>F</b>	5.4	5.6	0.213	0.22
<b>P2</b>	1.9	2.1	0.075	0.083
<b>D</b>	1.5	1.6	0.059	0.063
<b>D1</b>	1.50 Min		0.059 Min	
<b>P0</b>	3.9	4.1	0.154	0.161
<b>10P0</b>	40.0 +/- 0.20		1.574 +/- 0.008	
<b>W</b>	11.9	12.1	0.468	0.476
<b>P</b>	7.9	8.1	0.311	0.319
<b>A0</b>	6.3	6.5	0.248	0.256
<b>B0</b>	5.1	5.3	0.2	0.209
<b>K0</b>	2	2.2	0.079	0.087
<b>t</b>	0.30 +/- 0.05		0.012 +/- 0.002	