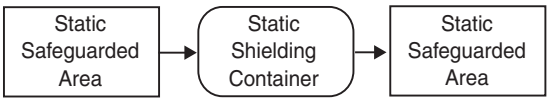
Handling MOS Devices

Static Discharge

Metal Oxide Semiconductor (MOS) devices have gained broad acceptance in telecommunications. This includes use of n-channel (NMOS) transistors, p-channel (PMOS) transistors, or both (complementary or CMOS) transistors. Most IXYS IC Division devices are fabricated using CMOS techniques, but some use PMOS. In any case, MOS circuits require special attention in design and handling because of their susceptibility to damage through buildup of static charges and the currents that occur during discharge.

Whether alone or mounted in circuit boards, MOS ICs are subject to buildup of static charges and damaging discharges. Voltage of several hundred volts can affect these devices, while one or two thousand volts will certainly cause harm. Five hundred volts can easily be generated by a person walking around or moving in a chair, and thousands of volts can be generated by the simple act of pulling out and tearing off a piece of transparent tape. Under these circumstances, precautions must be taken to limit the potential for damage to costly IC devices. MOS ICs should be handled in static-protected or “safeguarded” areas. Such areas include ionized air flow over nonconducting surfaces. When not in these areas, ICs should be kept in static shielded containers. ICs must be handled in safeguarded areas (receiving inspection, stores, assembly, and test) and, when moved from area to area, should be protected by shielded containers. Failure to implement procedures of this sort or relaxation of procedures can result in loss of valuable parts, increased production fallout, and higher repair costs.

Static Transmission



CMOS Latchup

Though all ICs are subject to static discharge damage, CMOS ICs can experience another kind of damaging event known as “latchup” or “SCR.” In this case, large currents can follow-through the part from the power supply, damaging transistors and interconnections. This occurs when currents are injected into the chip where they were not intended, usually through an I/O pin which has been driven to a voltage outside the supply range by some external device or event. This phenomenon is equivalent to four-layer conduction as used in SCRs, where a semiconductor device is “turned on” by injecting a current into a trigger layer. The device stays “on” until voltage is removed. This is useful in SCR control circuits, but in the case of CMOS ICs they may (1) recover completely after power has been cycled, (2) recover, but act very strangely, or (3) blow up completely. Causes can be inadequate power supply filtering, transient protection, or coincidences of PWB track layout. Static discharge may also trigger latchup.

For additional information please visit our website at: www.ixysic.com

Specification: AN-130-R04

4/10/2014