IXYS
INTEGRATED CIRCUITS DIVISION

**CPC1580 Application
Technical Information**

1 Using the CPC1580 Isolated Gate Driver IC

The CPC1580 is an excellent choice for remote switching of DC and low frequency loads where isolated power is unavailable. The device uses external components to satisfy design switching requirements, which enables the designer to choose from a great number of MOSFETs. The designer also has several options when designing over-voltage protection circuitry. The case studies look at only two of many methods, but each has unique constraints that should prove useful to many other designs.

Figure 1 shows a typical DC application circuit for using the CPC1580 gate driver. The driver allows the user to turn on the gate of a MOSFET and keep it on until the LED current is turned off. The application circuit uses a bootstrap diode (internal to the part) and

storage capacitor (C_{ST}) to provide the charge needed for fast turn-on switching of an external MOSFET device. When the MOSFET is on, the photo current from the LED keeps the MOSFET gate biased to the device's specified gate to source voltage (V_{GS}) continuously.

The CPC1580 uses charge from the load voltage when turning off to recover the MOSFET gate switching charge for the next turn-on event. The transistor will turn on even without this recovery of charge (in the case of no load voltage), although the turn-on will be much slower because only internal photo current will be charging the gate of the MOSFET. This feature can be exploited during system startup.

2 Application Component Selection

2.1 Storage Capacitor Selection C_{ST}

The storage capacitor (C_{ST}) enables the part to turn on quickly by holding a reservoir of charge to be transferred to the gate of the MOSFET. The turn-off cycle doesn't depend on the storage capacitor.

Equation 1: Charge Storage Capacitor Calculation:

$$C_{ST} \geq \frac{Q_G}{V_{LOAD} - V_{CAP}} \quad \text{(FARADS)}$$

Q_G is the MOSFET's total gate charge; $V_{CAP} \geq 15V$.

Equation 1 shows that the storage capacitor needs to deliver enough charge to the gate without going below the 15V required for switching the MOSFET. The

CPC1580 can deliver adequate peak current to drive 32nC total gate charge at the rated operating speed, and will operate with much higher capacitive loads (<4μF), or larger gate charge, with a slower turn-on and turn-off time.

> ***Note:*** *Care must be taken to minimize any capacitor-to-ground leakage current path between pins 7 and 8, MOSFET gate current, and between pins 5 and 6. Leakage currents will discharge the storage capacitor, and, even though the device is already on, will become a load to the photocurrent which keeps the gate voltage on. The gate voltage will be reduced if >500nA of leakage is present, therefore the combined impedance from pin 8 to pin 7, pin 5 and pin 6, capacitor current, and MOSFET current must be >20MΩ over the temperature rating of the part.*

Figure 1   CPC1580 DC Application Circuit Diagram with Over-Voltage Protection
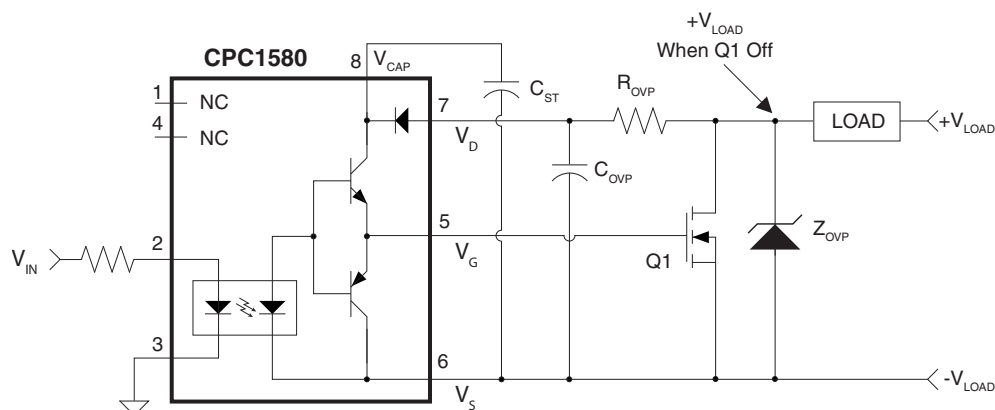
2.2   Transistor Selection

The CPC1580 charges and discharges an external MOSFET transistor. The selection of the MOSFET is determined by the user to meet the specific power requirements for the load. The CPC1580 output voltage is listed in the specification, but, as mentioned earlier, there must be little or no gate leakage.

Another parameter that plays a significant role in the determination of the transistor is the gate drive voltage available from the part. The CPC1580 uses photovoltaic cells to collect the optical energy generated by the LED, and, to generate more voltage, the photovoltaic diodes are stacked. As such, the voltage of the photovoltaic stack reduces with increased temperature. The user must select a transistor that will maintain the load current at the maximum temperature, given the V_{GS} in the CPC1580 specification.

The case studies below use "logic-level" MOSFETs for each design to maintain the load described.

2.2.1   Transistor Switching Characteristics

The primary characteristics of the application switching are t_{ON}, t_{OFF}, t_{RISE}, t_{FALL}, and the recovery time of the storage capacitor, t_{CHG}. These parameters are dependent on the MOSFET selection and need to be reviewed in light of the application requirements.

The CPC1580 turns on the MOSFET to the datasheet V_{GS} after the t_{ON} delay. Similarly the t_{OFF} delay is the amount of time until the LED is turned off and the capacitive load discharges to the level in the CPC1580 specification. For MOSFETs with larger or smaller required gate charge the t_{ON} and t_{OFF} will be proportionally faster and slower, but it is not a linear relationship.

To calculate the nominal rise and fall times of the MOSFET's drain voltage:

Equation 2: Rise Time Calculation

$$t_{RISE,VD} \approx \frac{V_{LOAD} \bullet C_{RSS}}{I_{G\_SINK}} \quad \text{(SECONDS)}$$

Equation 3: Fall Time Calculation

$$t_{FALL,VD} \approx \frac{V_{LOAD} \bullet C_{RSS}}{I_{G\_SOURCE}} \quad \text{(SECONDS)}$$

Where C_{RSS} is the MOSFET gate-drain capacitance (averaged over the switching voltage range) found in the MOSFET datasheet, I_{G_SINK} is the gate sinking current of the CPC1580, and I_{G_SOURCE} is the gate driving ability. The maximum value of t_{RISE} is limited by the CPC1580 unloaded discharge characteristic, and should be reviewed in light of the final application component selections, if critical.

To calculate the value for the charge time, t_{CHG}, which is due to external component selection:

Equation 4: Storage Capacitor Charge Recovery Time (seconds):

$$t_{CHG} \approx -(400 + R_{OVP}) \bullet (C_{ST} + C_{OVP}) \bullet \ln\left(\frac{(V_{LOAD} - V_{FINAL}) \bullet C_{ST}}{Q_G}\right)$$

where ($V_{LOAD} - V_{FINAL}$) is the difference in voltage between the required load voltage and the potential the capacitor will charge up to. The voltage at the storage capacitor is $V_{LOAD} - (Q_G/C_{ST})$ when the MOSFET is on, where charge, Q_G, is the amount of charge required to switch the MOSFET gate from 0V to the final voltage out of the CPC1580 (V_{GS} specification). V_{FINAL} is the capacitor voltage when it charges back up from when the MOSFET is off.

R_{OVP} and C_{OVP} form the overvoltage protection RC filter. The RC filter is used to reduce the peak power dissipation in the MOSFET by controlling the rate of rise of the drain voltage. Note that the RC circuit will reduce the switching speed of the MOSFET.

> *Note: Obviously, the logarithm doesn't work if $V_{FINAL} = V_{LOAD}$ because of the exponential nature of R-C charging. That subsequently affects the next cycle, so C_{ST} is more critical and should be larger if the switching frequency is faster. Selecting the term inside the logarithm to be 0.05 yields 3τ equivalent time-constants.*

Using this information, the maximum switching frequency will be calculated in each application case study below.

> *Note: The CPC1580 is ideal to use where remote power is otherwise unavailable. If the LED is also powered remotely, care must be taken to ensure that parasitic transient signals are reliably filtered from the input control signal. Large transient currents will mutually couple energy between cables and a simple R-C filtering of the CPC1580 input may be sufficient to suppress false turn-on.*

3   Application Switching Losses

During the transition intervals, the application and load components change energy states and during the process incur switching losses. These losses are manifested as heat in the application circuit, and must be addressed by the designer to ensure that no one component exceeds its power rating. The designer must understand the details of load behavior in order to adequately size and protect the application circuit. There are three general cases to observe: (1) purely resistive loads, (2) inductive/resistive loads, and (3) loads with significant capacitance. Inductors and capacitors are energy storage elements that require special consideration for switching.

During switching periods, the energy stored in the load inductor is discharged through the switching MOSFET, load capacitance and the over-voltage-protection circuitry.

At turn-on, the inductor energy is zero, and so the capacitive energy in the load and parasitic elements of the switching application must be dissipated by the MOSFET in order for the load to change state.

Equation 5: Stored Inductive Energy (Joules)

$$E_L = \frac{1}{2} \bullet L \bullet I_{LOAD}^2$$

3.1   Resistive Load Losses: The Ideal Case

For purely resistive loads, the energy dissipated by changing states occurs primarily in the MOSFET. The equation describing MOSFET energy dissipation is:

Equation 6: MOSFET Energy: E_{RISE} (Joules)

$$E_{MOSFET} \geq V_{LOAD}^2 \bullet \frac{C_{RSS}}{I_{G\_SINK}} \bullet \frac{I_{LOAD}}{6} = \frac{P_{LOAD}}{6} \bullet t_{RISE,VD}$$

The average power of the MOSFET for any load type is:

Equation 7: MOSFET Average Power (Watts)

$$P_{AVG} = I_{LOAD}^2 \bullet R_{DSAT} \bullet D + f_{SWITCH} \bullet (E_{RISE} + E_{FALL})$$

Where f_{SWITCH} is the application switching frequency, R_{DSAT} is the MOSFET's on-resistance, D is the switch's operational duty cycle: $D = t_{ON}/(t_{ON}+t_{OFF})$. E_{RISE} and E_{FALL} are the energy dissipated during the rise and fall times.

3.2   Inductive/Resistive Loads

If the load is resistive and inductive, and the inductance doesn't saturate, then the load current during turn-off is described by:

Equation 8: Resistive/Inductive Load Current during t_{RISE} (Amps)

$$I_{LOAD}(t) = \frac{V_{LOAD}}{R_{LOAD}} - \frac{I_{G\_SINK}}{L_{LOAD} \bullet C_{RSS}} \bullet \left(\frac{L_{LOAD}}{R_{LOAD}}\right)^2 \bullet \left[\frac{R_{LOAD}}{L_{LOAD}} \bullet t - 1 + e^{\frac{-R_{LOAD}}{L_{LOAD}} \bullet t}\right]$$

The drain voltage during turn-off is:

Equation 9: MOSFET Drain Voltage during t_{RISE} (V)

$$V_{DRAIN}(t) = \frac{I_{G\_SINK}}{C_{RSS}} \bullet t$$

The instantaneous power in the MOSFET will be the product of the two equations and the energy will be the integral of the power over time.

3.3   Capacitive Loads

The energy absorbed by the MOSFET for loads that are more capacitive in nature occurs during the MOSFET turn-on as opposed to the turn-off. The energy absorbed by the MOSFET will be a function of the load, the Transient Voltage Suppressor (TVS) or other protector, and the MOSFET drain capacitance.

Equation 10: MOSFET Energy: E_{FALL} (Joules)

$$E_{FALL} = \frac{1}{2} \bullet (C_{TVS} + C_{OSS} + C_{LOAD}) \bullet V_{LOAD}^2$$

C_{OSS} is the MOSFET output capacitance found in the datasheet. As mentioned earlier, the MOSFET switching losses occur at different times, either rising or falling, so loads with a combination of inductance and capacitance can also be calculated by the energy equations described above.

The MOSFET can dissipate the repeated avalanche energy, (E_{AR}), as specified in the datasheet. However that energy must be reduced for increased ambient temperature. For a 150°C MOSFET, the energy reduction at $T_{J,MAX}$ is:

Equation 11: MOSFET Energy Adjustment for Operating conditions (Joules):

$$E(T_{J,MAX}) \leq E(25°C) \bullet \frac{(150°C - T_{J,MAX})}{(150°C - 25°C)}$$

$T_{J,MAX}$ is the junction temperature of the die, so it must include the temperature increase caused by power dissipation of the load and the thermal impedance of the package/application. $E(25°C)$ is the E_{AR} specification found in the MOSFET datasheet at 25°C.

3.4 dV/dt Characteristics

The application shown in **Figure 1** and described in section **6.1** "**Case 1: 24 V Loading Application**" dissipates significant energy caused by large dV/dt events. Fault voltages across the MOSFET will turn it on for the same reason the part turns off slowly.

4 Design Switching Frequency

The over-voltage protection and storage capacitor play a significant role in determining the switching frequency. The maximum switching frequency is a function of the gate charge of the MOSFET, the storage capacitor (C_{ST}), and R_{OVP} The maximum switching frequency relationship is:

Equation 12: Maximum Switch Operation (Hz)

$$F_{MAX} \leq \frac{1}{M} \bullet (t_{ON} + t_{OFF} + t_{RISE,VD} \mid t_{CHG} + t_{FALL,VD})^{-1}$$

5 CPC1580 Over-Voltage Protection

Over-voltage protection is generally required for the CPC1580 because of parasitic inductance in the load, wires, board traces, and axial leads of protectors. Purely resistive loads or loads with low voltage switching may be able to rely on the transistor to handle any parasitic energy and thereby not require protection for the CPC1580. For very low-inductance loads and traces, over-voltage suppression may be handled with a simple RC filter consisting of R_{OVP} and C_{OVP} or by use of a free-wheeling diode. For more moderate load inductance, or remote switching of a load (i.e. through a long cable) a voltage suppressor can be used. For heavily inductive loads only a free-wheeling diode, D_{OVP} connected across the load element is recommended, see **Figure 2**.

For dV/dt events > I_{G_SINK}/C_{RSS} (from Equation 2) the application circuit will dissipate energy proportional to the C_{RSS} and g_{FS} (forward conductance) of the selected transistor. C_{RSS} is a function of the transistor's on-resistance and current/power capability, so higher load designs are more sensitive.

The CPC1580 provides an internal clamp to protect the gate of the MOSFET from damage during such an event. It can withstand 100mA for short periods, for instance, during dV/dt transients.

> *Note:* *The CPC1580 is ideal to use where remote power is otherwise unavailable. If the LED is also powered remotely, care must be taken to ensure that parasitic transient signals are reliably filtered from the input control signal. Large transient currents will mutually couple energy between cables and a simple R-C filtering of the CPC1580 input may be sufficient to suppress false turn-on.*

where M=3 (a multiplication factor for temperature and process variations); t_{ON} and t_{OFF} are CPC1580 datasheet parameters; $t_{RISE,VD}$ is the rise time of the drain voltage; t_{CHG} is the charge time of the storage capacitor (C_{ST}) and over-voltage protection circuitry (C_{OVP} and R_{OVP}); and $t_{FALL,VD}$ is the fall time across the transistor. For this calculation, choose the greater of $t_{RISE,VD}$ or t_{CHG}.

There is no minimum switching frequency because the CPC1580 uses photovoltaic diode current to keep the output charged as long as LED current flows.

The energy not consumed in switching losses must be absorbed by the over-voltage protection element. Most protective devices are designed to withstand certain peak power in the case of a TVS, or maximum avalanche energy in the case of a MOSFET. To reduce the amount of stored inductive energy, a larger capacitor can be added in parallel with the gate-drain connection of the MOSFET. However care must be taken so that the rise time and peak current do not exceed the Safe Operating Area (SOA) rating of the transistor. A consequence of increasing the gate-drain effective capacitance is reduced dV/dt tolerance.

Figure 2   CPC1580 Over-Voltage Protection for Inductive Loads
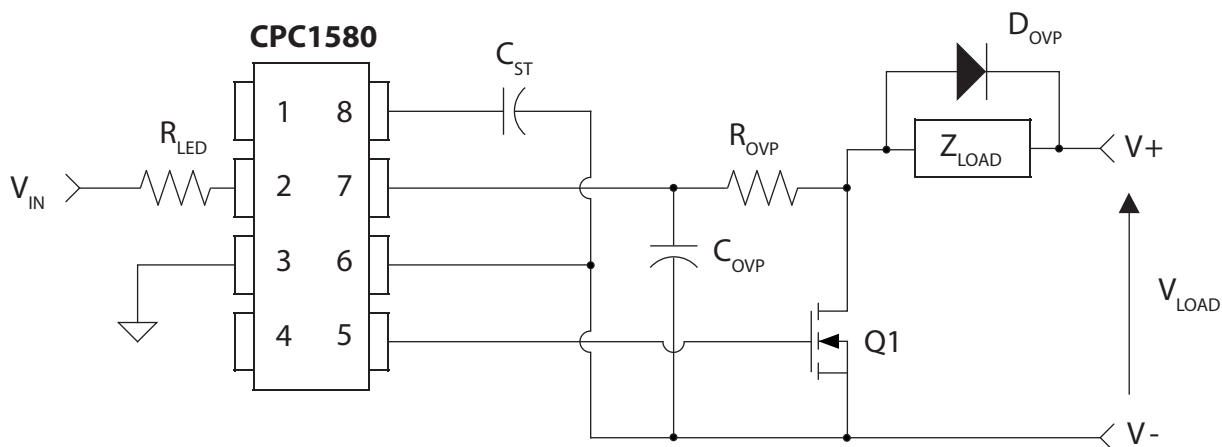
5.1   Other Protection Techniques [1, 2]

For applications in which higher inductance loads are switched, the designer must consider other circuit techniques, device ratings, or protector types. Of paramount importance is that the designer know the characteristics of the load being switched.

[1] An excellent source describing power electronic devices and switching behavior is: *Power Semiconductor Devices,* by B. Jayant Baliga, ISBN 0-543-94098-6

[2] For more over-voltage protection circuit techniques consult: *Switchmode Power Supply Handbook*, *2nd Edition*, Keith Billings, ISBN 0-07-006719-8, or *Power MOSFET Design*, B. E. Taylor, ISBN 0-471-93802-5.

6   Design Examples

Table 1: shows two sample application component selections each with different over-voltage protection strategies.

Table 1:   Sample Application Components

Device	Case 1: 24V/10A Value/Rating	Case 2: 48V/5A Value/Rating	Comment
Q1	SUD45N05-20L [3]	SUD23N06-31L [3]	MOSFET
C_{ST}	>0.01μF/100V	>0.01μF/100V	5% Ceramic Disk
Z_{OVP}	SA24A [3]	SA48A [3]	Littelfuse TVS-style protector
R_{OVP}	1KΩ	5.1KΩ	5%, 1/8 Watt (60Hz Switching Frequency or less)
C_{OVP}	0.001μF, 50V	0.001μF, 100V	5% Ceramic Disk
R_{LED}	680Ω, 1/8 Watt	680Ω, 1/8 Watt	0 - 5V Switching

[3] Use of the SUD45N05-20L, SUD23N06-31L, SA24A, and SA48A product datasheets is necessary to completely understand the examples given.

6.1   Case 1: 24V Load Switching

In this example, the over-voltage protection circuitry is quite simple. The CPC1580 is guaranteed for 60V operation and the protector is rated for 45.4V @ 11.2A peak pulse current, well below the 60V. The transistor (Q1) is a 50V MOSFET, which guarantees the TVS clamps before the transistor breakdown.   Assuming there will be load inductance in both the V_{LOAD+} and

V_{LOAD-} traces, a TVS is selected to clamp the residual 10A not otherwise dissipated in the turn-off of the MOSFET and parasitic TVS capacitance. R_{OVP} and C_{OVP} are optional for this load condition; however, their inclusion will ease layout and critical placement of the CPC1580.

Figure 3   Case 1 Application Circuit

For this test case, the maximum switching frequency for the design is $F_{MAX} = 0.333 \cdot (40μs + 600μs + (40μs | 42μs) + 0.87μs)^{-1} < {\sim}475Hz$. The components selected were used for in-lab testing. Other components with smaller package sizes and wattage will also work, if calculations are performed to meet component specifications.

Example:

- R_{LED}=680Ω
- Minimum voltage drop across the LED is 1.0V

- Switching voltage, SwV_{ON}, when on, is 5V
- I_F=Forward current of the LED

$$I_F = \frac{SwV_{ON} - \text{Min LED Volt}}{R_{LED}}$$

$$I_F = \frac{5V - 1V}{680\Omega}$$

$$I_F = 0.005882A = 5.9mA$$

The recommended I_F is between 2mA and 10mA. The I_F calculated above meets this requirement.

The power dissipated, P_D, is:

$$P_D = I_F^2 \bullet R$$
$$P_D = (5.9mA)^2 \bullet (680\Omega)$$
$$P_D = 0.024W = 24mW$$

These calculations show that a 0603 resistor, which is 1/16 Watt, can be selected. The 1/16 Watt still provides an adequate design margin: 0.0625W where only 0.024W is required.

6.1.1 Measured Results

Figure 4 shows the discharge of the storage capacitor due to the gate switching on. The calculated voltage drop (V_{LOAD} - V_{CAP}) using C_{ST} = 10 nF and (Q_G = 43nC from the Q1 datasheet) from **Equation 1** is 4.3 Volts.

From Equation 1: Charge Storage Capacitor Calculation:

$$C_{ST} \geq \frac{Q_G}{V_{LOAD} - V_{CAP}} \qquad (FARADS)$$

From Equation 2: Rise Time Calculation

$$t_{RISE,VD} \approx \frac{V_{LOAD} \bullet C_{RSS}}{I_{G\_SINK}} \qquad (SECONDS)$$

t_{RISE} ~ (24V-5V) • 190pF/.0036 A ~ 1μS

From Equation 3: Fall Time Calculation

$$t_{FALL,VD} \approx \frac{V_{LOAD} \bullet C_{RSS}}{I_{G\_SOURCE}} \qquad (SECONDS)$$

t_{FALL} ~ (24V-5V) • 190pF/0.00022 A ~ 16μS

All other calculated / measured data is summarized in **Table 2:**

Table 2: 24 Volt Load Switching Data

Parameter	Calculated	Measured
Voltage Drop C_{ST}	4.3V	3.7V
t_{FALL} **Figure 5**	16μS	2μS
t_{RISE} **Figure 8**	1μS	38μS [4]
t_{ON} **Figure 6**	16μS (**1580 spec**)	7.3μS
t_{OFF} **Figure 7**	175μS (**1580 spec**)	189μS

The energy in **Figure 9** rises to 3.3mJ, and the switching frequency can be as high as >475Hz which would make the average power

$(12A)^2 \bullet 0.02\Omega + 475/s \bullet 3.3mJ = 4.5$ Watts, assuming very high operational duty cycles.

This circuit load was modified to include an 800μH inductor that saturates at ~0.5A. This load condition may not represent the user's load but does serve to illuminate more about the switching characteristics of a non-linear load.

Again this assumes that the magnetics do not saturate, however for the graphs shown in **Figure 10** and **Figure 11**, the current equation above only applies after the magnetic flux leaves saturation and becomes inductive again. As such, the load current is dominated by V_{LOAD} and R_{LOAD} in **Figure 10**.

The power absorbed by the TVS can be calculated from the characteristic of the waveform shown in **Figure 10**:

Energy = ½ L • I^2 = [(V_{TVS}-V_{LOAD}) • t_{DSCHG}]^2/(2 • L)

which is ½ • 800μH • $(0.45A)^2$ = 81μJ. This current (0.45A) agrees well with the turn-off characteristic shown in the graph where the magnetics leave saturation at ~0.5A.

The example listed demonstrates the need to have an accurately characterized load so that the energy due to the switching event does not exceed the rating of the MOSFET or TVS protector.

[4] The calculated rise time relies on the manufacturer supplied graphs for C_{RSS}. The actual rise time during the interval shown in **Figure 8** is longer due to the non-linear nature of the capacitance C_{RSS}. From the datasheet graphs, the average capacitance is 190pF over the interval of 5V<V_{DS}<25V. During the initial turn-off the capacitance is much larger, affecting the total energy by ~30%. A second-order effect not used in Equation 2 is due to the gate-source capacitance C_{ISS}. That additional capacitance divided by the transistor's conductance and load resistance causes an additional delay of 5μs-10μs, so the calculated rise time is closer to 35μs.
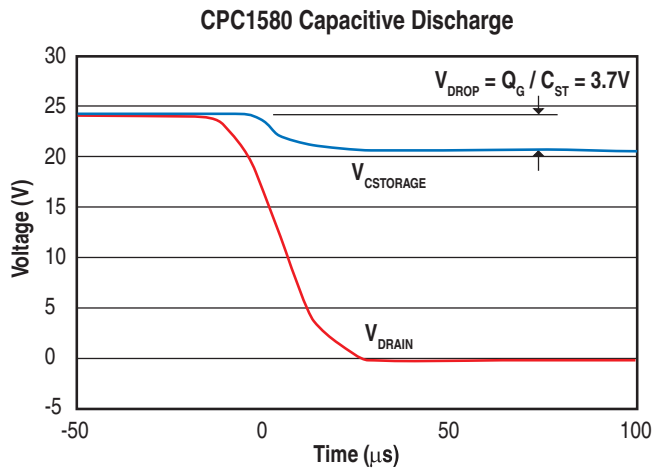
Figure 4   Discharge from Gate Turning On

CPC1580 Capacitive Discharge
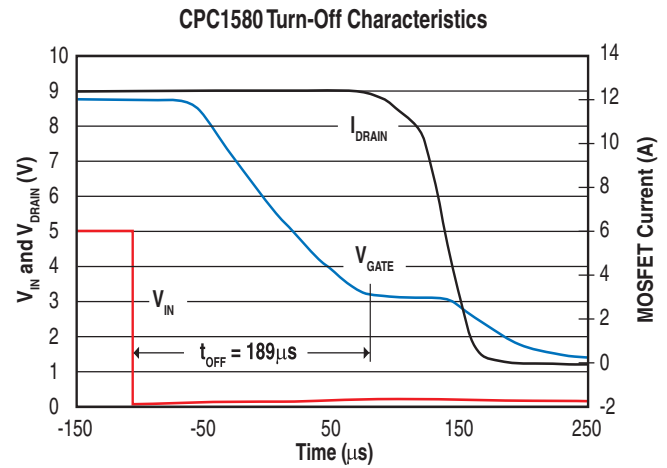
Figure 5   Load Current and t$_{FALL}$

CPC1580 Turn-On Characteristics
With Resistive Load (1.8Ω)

Figure 6   Turn-On Delay

CPC1580 Turn-On Characteristics

Figure 7   Turn-Off Delay

CPC1580 Turn-Off Characteristics
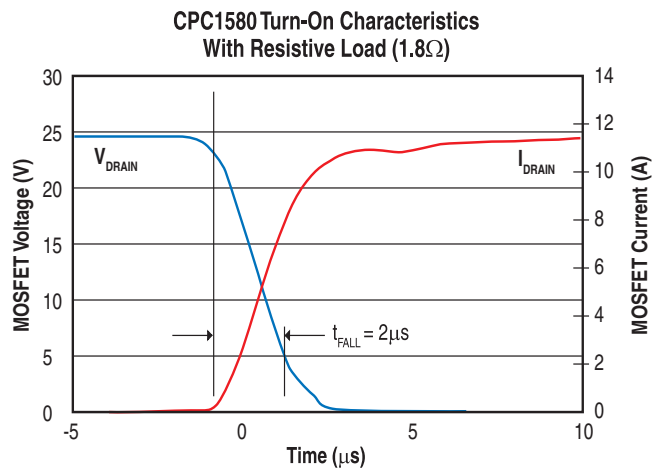
Figure 8   Load Current and t$_{RISE}$

CPC1580 Turn-Off Characteristics
With Resistive Load (1.8Ω)
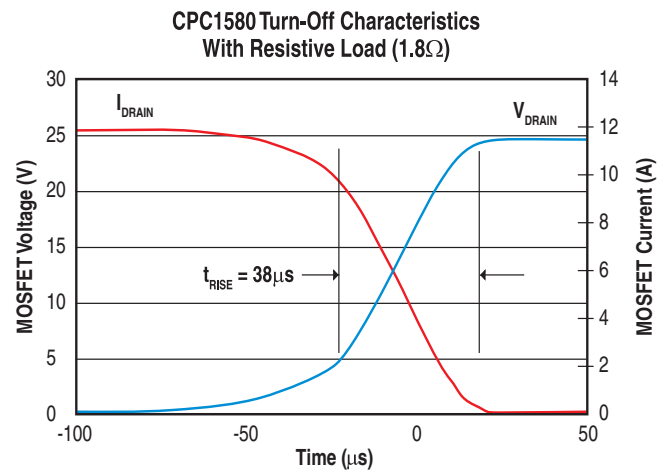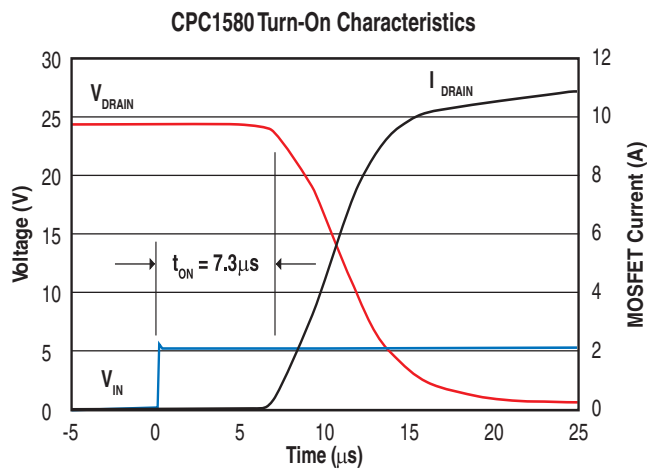
Figure 9   Discharge Power and Energy

CPC1580 Switching Losses
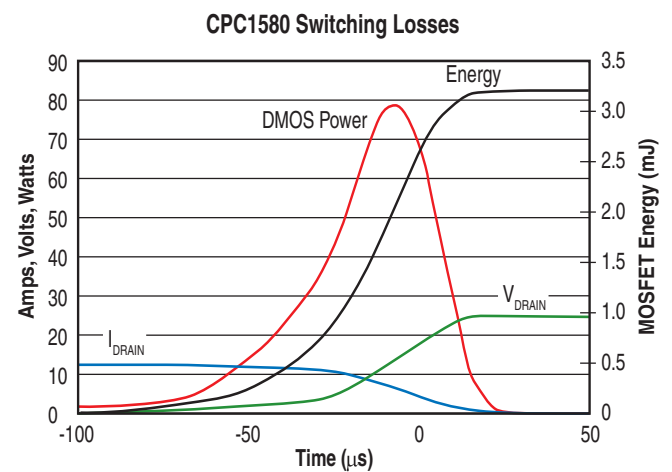
Figure 10 Moderate Inductive Current and t$_{RISE}$

**CPC1580 Switch Turn-Off
w / 800µH Inductance**
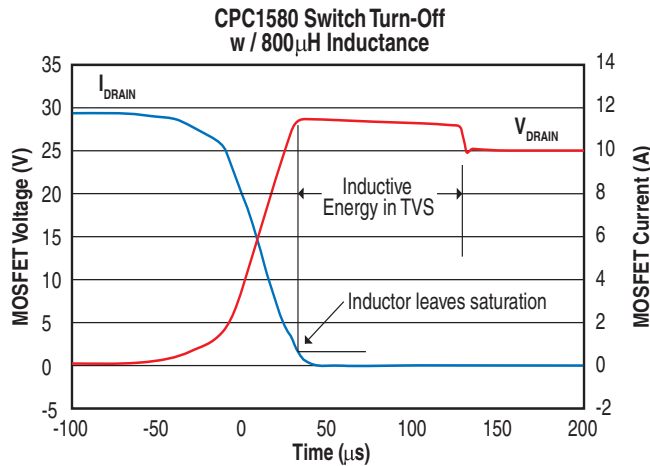
Figure 12 Turn-On with Modified Load

**CPC1580 Turn-On Characteristics
100µH / 10Ω Load**
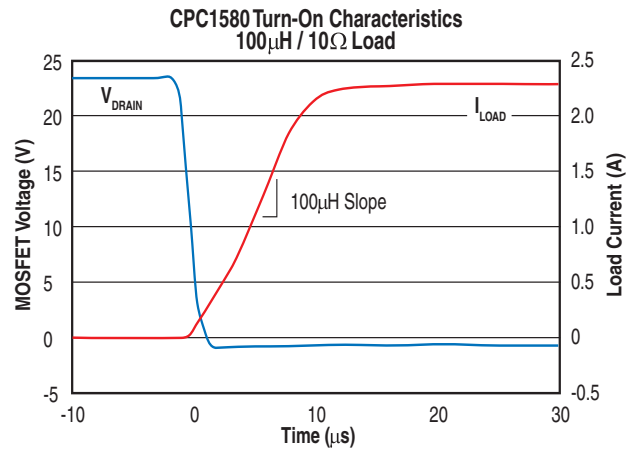
Figure 11 Inductive Turn-On

**CPC1580 Turn-On Characteristics
w / 800µH Inductance**

Figure 13 Turn-Off with Modified Load

**CPC1580 Turn-Off Characteristics
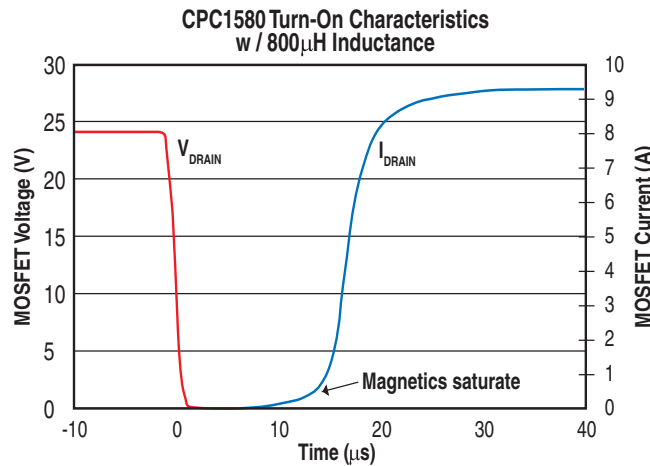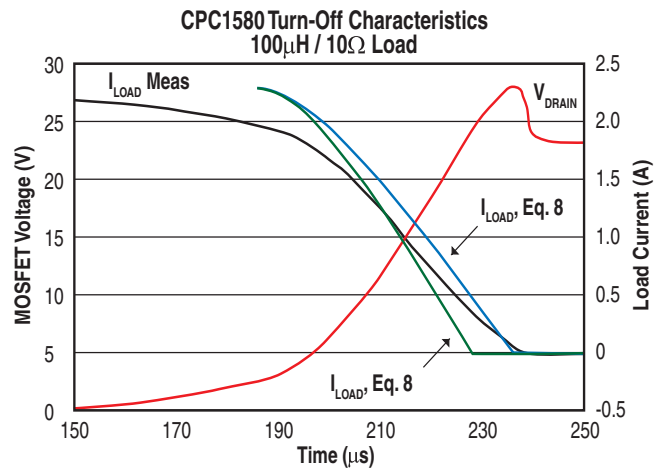100µH / 10Ω Load**

The load was modified to avoid saturating the magnetics allowing comparison of the expected load current (from Equation 8) versus the measured load current. The circuit changes were to increase the resistance to 10.2 Ohms and change the magnetic inductance to 113µH.

As seen in the turn-on characteristic is almost perfectly inductive where the di/dt forms a non-saturating V/L curve. The voltage applied remains at 24V.

Figure 13 shows the inductive nature of the turn-off as seen in the overshoot. In this case **Equation 8** was fit to the time-base and the resistance, inductance, and capacitance were plugged in. The slope of the line is steeper than expected, which is what has been observed in the previous example. **Equation 8** was then modified to include the C$_{ISS}$ factor

(C$_{RSS}$ + C$_{ISS}$/(g$_{FS}$ • R$_{LOAD}$)) and the resultant slope better approximates the actual slope as expected. It is worth restating that the slow change at the beginning of the transition is due to the large non-linearity in capacitance vs. voltage. While this interval is an important component of the total energy (~30%) the calculation is more complicated and not readily available from the component datasheets. Analysis described in the references listed will improve the characteristic to within 10%.

Equation 8 proves to be an accurate model for load current during the turn-off time, which can be subsequently used to consume inductive energy during the turn-off event. The equation can include second-order terms to more accurately model the transition region of switching.
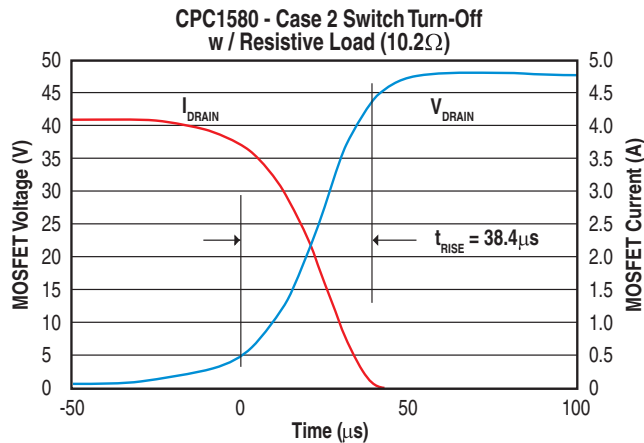
6.2   Case 2: 48V Load Switching

Voltages closer to the peak operating voltage of the CPC1580 can also be accommodated, but the over-voltage protection becomes more important. **Table 1:** shows a sample over-voltage protection component selection for a 48V/5A design requirement.

The design criteria are more complicated because the peak voltage at 5A for the TVS component is 77V which exceeds the voltage rating for the CPC1580 and MOSFET of 60 volts maximum. Two conditions must be met for using such a protector: (1) protecting the

CPC1580 from going above it's maximum voltage, and (2) ensuring the avalanche energy of the MOSFET is not exceeded. Since the MOSFET breakdown voltage will be nominally higher than the specification, (or if the user selects a higher voltage MOSFET), then C_{OVP} should be replaced with a zener diode/TVS to keep the voltage at pin 7 (V_D) to less than 60V but greater than 48V. (Until the parasitic inductance discharges to 1mA at which the TVS voltage is 59V.)

Figure 14   Case 2 Application Circuit

6.2.1   Measured Results

The design for Case 2 was implemented and the following characteristics observed. **Figure 15** shows the fall time for a resistive load. The calculated fall time is ~1µS. The rise time is shown in **Figure 16**. The calculated value is 34µS in the linear region shown on the graph. The peak energy during the transient is shown in **Figure 17**. The calculated Peak Energy, from Equation 6 is 1.36mJ. This value is consistent with the linear-region switching losses. The additional energy dissipation is due to the large non-linear capacitance at the beginning of the transition.

Figure 18 and **Figure 19** demonstrate the response with the inclusion of the inductive load. For the case shown, the MOSFET energy dissipation exceeds the stored inductive energy of 160µJ, so no energy is transferred to the TVS.

The charge time plays a significant role in the calculation of the maximum switching frequency for this case study. However, the charging voltage is very small so the resulting charge time can be reduced, knowing

that the voltage dropped across R_{OVP} will increase proportionally. The maximum switching frequency of the example in **Table 1:** is $F_{MAX} = 0.333 \bullet$ (40µs + 600µs + (34µs | 181µs) + 2µs)$^{-1}$ < ~400Hz.

Figure 15   48V Case Study t$_{FALL}$

Figure 16   48V Case Study t$_{RISE}$

CPC1580 - Case 2 Switch Turn-Off
w / Resistive Load (10.2Ω)

t$_{RISE}$ = 38.4μs

Figure 17   48V Case Study Peak Power and Energy

CPC1580 Switching Losses

DMOS Power
Energy
V$_{DRAIN}$
I$_{DRAIN}$

Figure 18   Inductive Turn-On Transition

CPC1580 - Case 2 Turn-On Characteristics
w / Modified Inductive Load (113μH / 25Ω)

V$_{DRAIN}$
I$_{LOAD}$
~ 113μH

Figure 19   Inductive Turn-Off Transition

CPC1580 - Case 2 Turn-Off Characteristics
w / Unsaturated Inductive Load

I$_{LOAD}$
V$_{DRAIN}$

For additional information please visit our website at: www.ixysic.com