

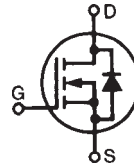
PolarHV™ HiPerFET IXFR 80N50P

Power MOSFET

ISOPLUS247™

(Electrically Isolated Back Surface)

N-Channel Enhancement Mode
Avalanche Rated
Fast Intrinsic Diode



$$V_{DSS} = 500 \text{ V}$$

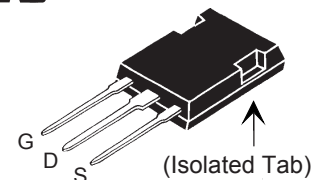
$$I_{D25} = 45 \text{ A}$$

$$R_{DS(on)} \leq 72 \text{ m}\Omega$$

$$t_{rr} \leq 200 \text{ ns}$$

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	500	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C ; $R_{GS} = 1 \text{ M}\Omega$	500	V
V_{GSM}	Transient	± 40	V
V_{GSM}	Continuous	± 30	V
I_{D25}	$T_C = 25^\circ\text{C}$	45	A
I_{DM}	$T_C = 25^\circ\text{C}$, pulse width limited by T_{JM}	200	A
I_{AR}	$T_C = 25^\circ\text{C}$	80	A
E_{AR}	$T_C = 25^\circ\text{C}$	80	mJ
E_{AS}	$T_C = 25^\circ\text{C}$	3.5	J
dv/dt	$I_S \leq I_{DM}$, $di/dt \leq 100 \text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ\text{C}$, $R_G = 2 \Omega$	20	V/ns
P_D	$T_C = 25^\circ\text{C}$	360	W
T_J		-55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		-55 ... +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering	300	$^\circ\text{C}$
F_C	Mounting force	20..120/4.5..25	N/lb
V_{ISOL}	50/60 Hz, RMS, 1 minute	2500	V~
Weight		5	g

ISOPLUS247 (IXFR)
E153432



G = Gate D = Drain
S = Source

Features

- 1 Silicon chip on Direct-Copper-Bond substrate
- High power dissipation
- Isolated mounting surface
- 2500V electrical isolation
- 1 Low drain to tab capacitance (<30pF)
- 1 Low $R_{DS(on)}$ HDMOS™ process
- 1 Rugged polysilicon gate cell structure
- 1 Rated for Unclamped Inductive Load Switching (UIS)
- 1 Fast intrinsic Rectifier

Applications

- 1 DC-DC converters
- 1 Battery chargers
- 1 Switched-mode and resonant-mode power supplies
- 1 DC choppers
- 1 AC motor control

Advantages

- 1 Easy assembly
- 1 Space savings
- 1 High power density

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0 \text{ V}$, $I_D = 500 \mu\text{A}$	500		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 8 \text{ mA}$	3.0		5.0 V
I_{GSS}	$V_{GS} = \pm 30 \text{ V}_{DC}$, $V_{DS} = 0$			$\pm 200 \text{ nA}$
I_{DSS}	$V_{DS} = V_{DSS}$, $V_{GS} = 0 \text{ V}$, $T_J = 125^\circ\text{C}$			25 μA 2 mA
$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$, $I_D = 40 \text{ A}$			72 m Ω

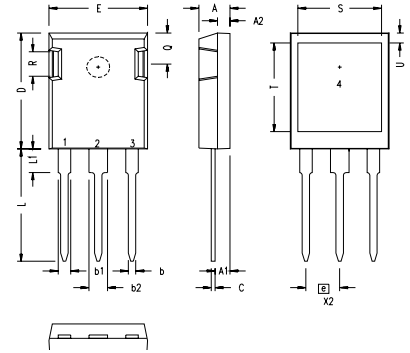
Symbol	Test Conditions	Characteristic Values		
		(T _J = 25° C unless otherwise specified)		
		Min.	Typ.	Max.
g_{fs}	V _{DS} = 20 V; I _D = 40 A, I _{D25} , Note 1	45	70	S
C_{iss}			12.7	nF
C_{oss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz		1280	pF
C_{rss}			120	pF
t_{d(on)}			25	ns
t_r	V _{GS} = 10 V, V _{DS} = 0.5 V _{DSS} , I _D = 40 A		27	ns
t_{d(off)}	R _G = 1 Ω (External)		70	ns
t_f			16	ns
Q_{g(on)}			197	nC
Q_{gs}	V _{GS} = 10 V, V _{DS} = 0.5 V _{DSS} , I _D = 40 A		70	nC
Q_{gd}			64	nC
R_{thJC}				0.35° C/W
R_{thCS}		0.15		° C/W

Source-Drain Diode

Symbol	Test Conditions	Characteristic Values		
		(T _J = 25° C unless otherwise specified)		
		Min.	Typ.	Max.
I_S	V _{GS} = 0 V			80 A
I_{SM}	Repetitive			200 A
V_{SD}	I _F = I _S , V _{GS} = 0 V,			1.5 V
t_{rr}	I _F = 25 A, -di/dt = 100 A/μs			200 ns
Q_{RM}	V _R = 100 V, V _{GS} = 0 V		0.6	μC
I_{RM}			6	A

Notes:

1. Pulse test, t ≤ 300 μs, duty cycle d ≤ 2 %

ISOPLUS247™ Outline


SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b1	.075	.084	1.91	2.13
b2	.115	.123	2.92	3.12
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
E	.620	.635	15.75	16.13
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.520	.540	13.21	13.72
T	.620	.640	15.75	16.26
U	.065	.080	1.65	2.03

- 1 - GATE
- 2 - DRAIN (COLLECTOR)
- 3 - SOURCE (EMITTER)
- 4 - NO CONNECTION

NOTE: This drawing will meet all dimensions requirement of JEDEC outline TO-247AD except screw hole.

Fig. 1. Output Characteristics @ 25°C

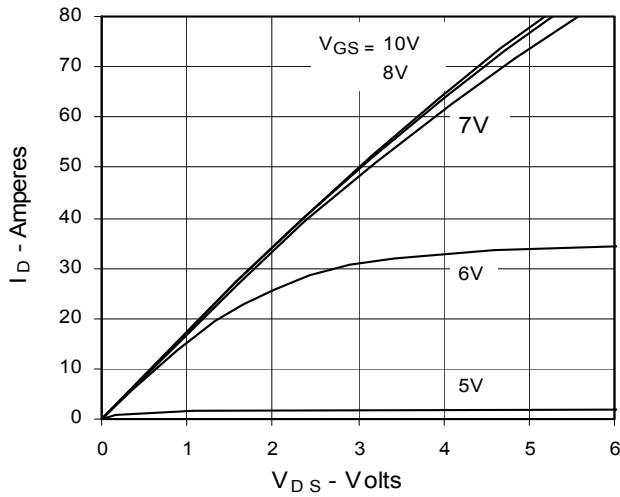


Fig. 2. Extended Output Characteristics @ 25°C

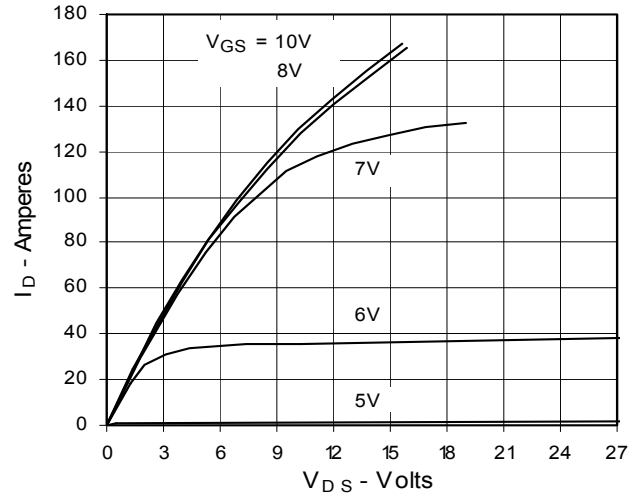


Fig. 3. Output Characteristics @ 125°C

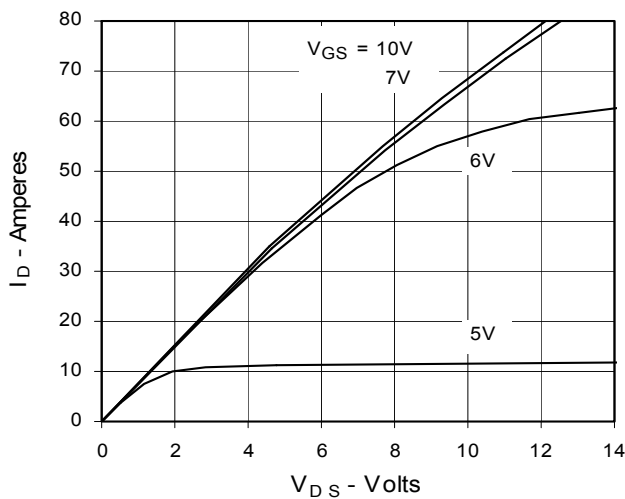


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 40$ A Value vs. Junction Temperature

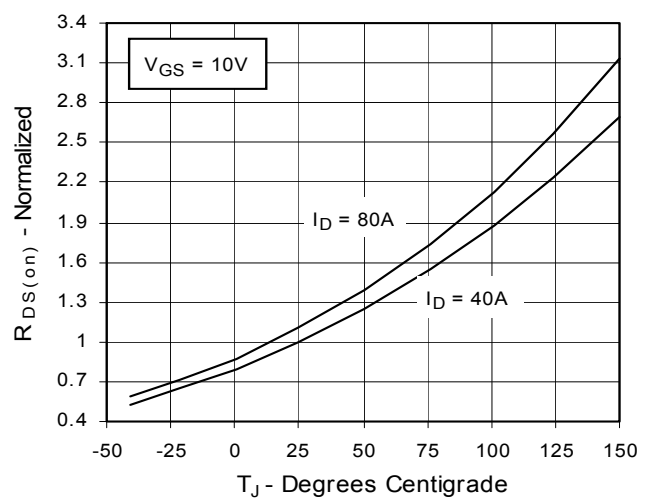


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 40$ A Value vs. I_D

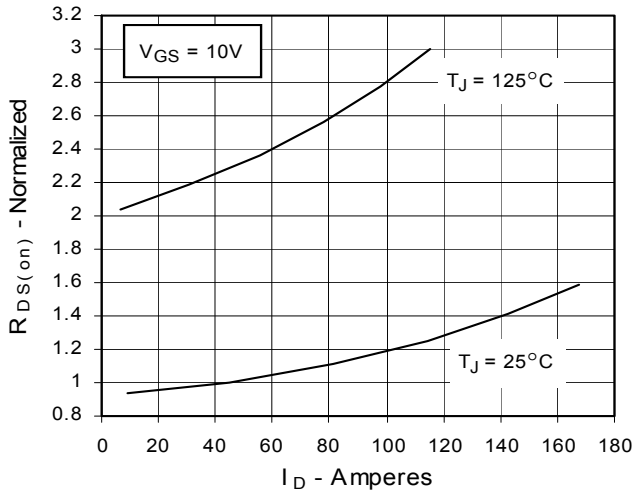


Fig. 6. Drain Current vs. Case Temperature

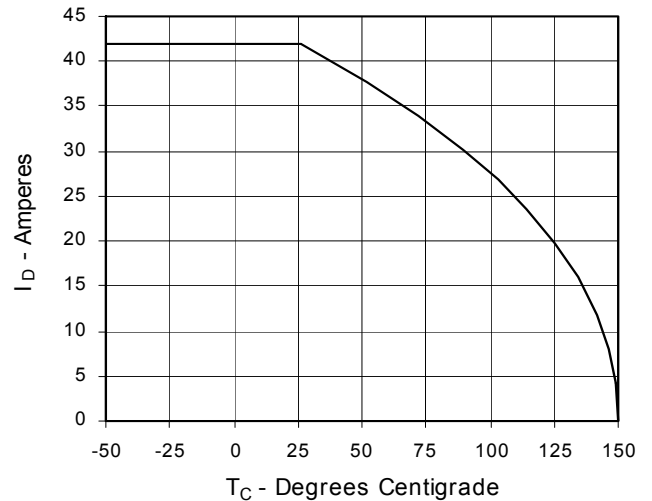


Fig. 7. Input Admittance

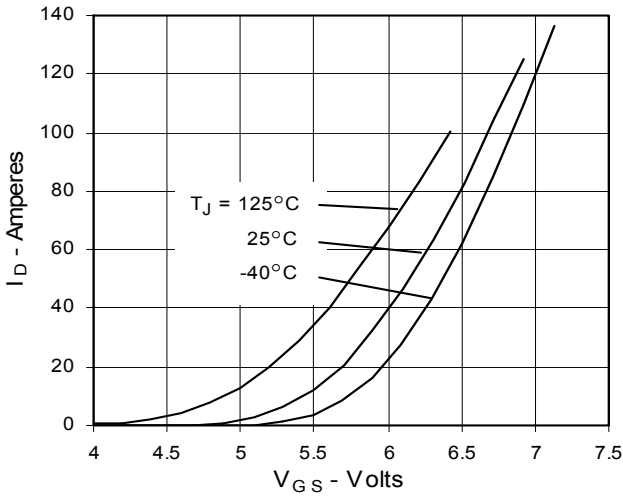


Fig. 8. Transconductance

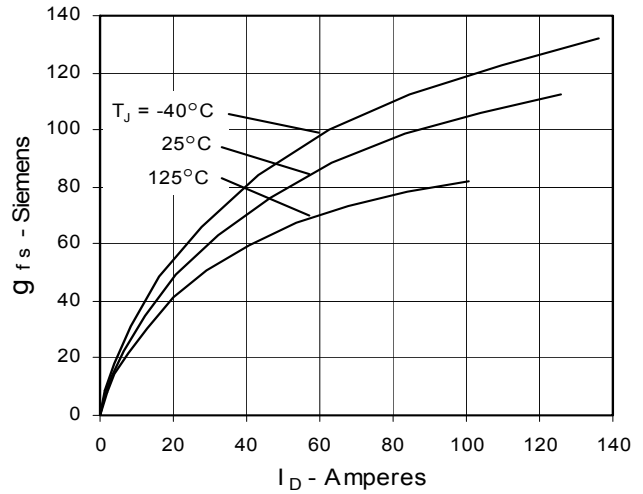


Fig. 9. Source Current vs. Source-To-Drain Voltage

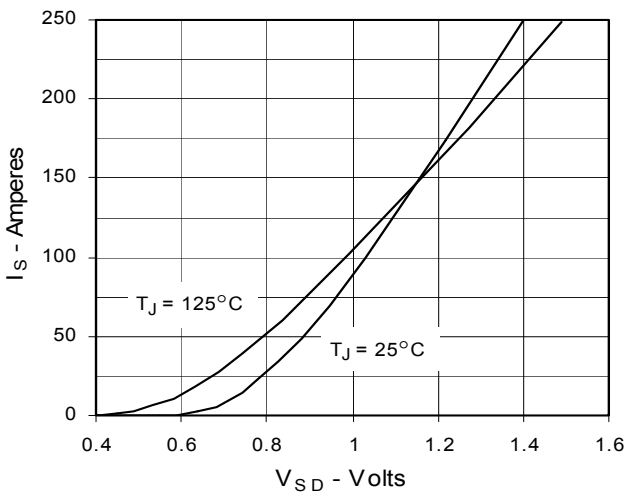


Fig. 10. Gate Charge

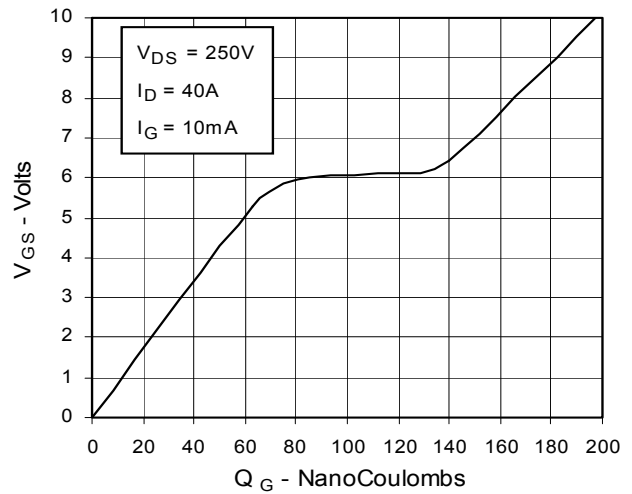


Fig. 11. Capacitance

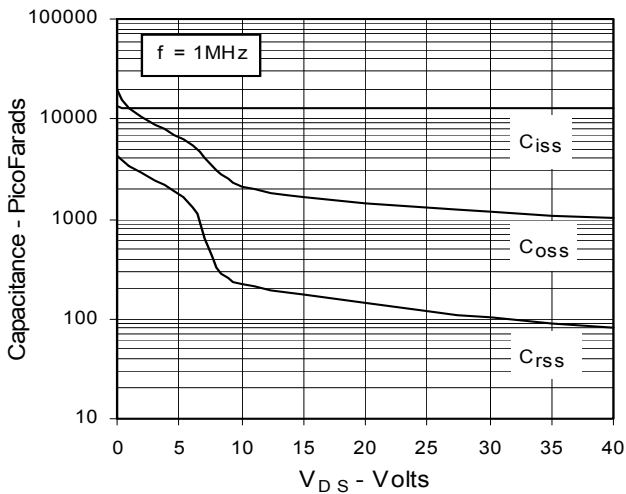


Fig. 12. Forward-Bias Safe Operating Area

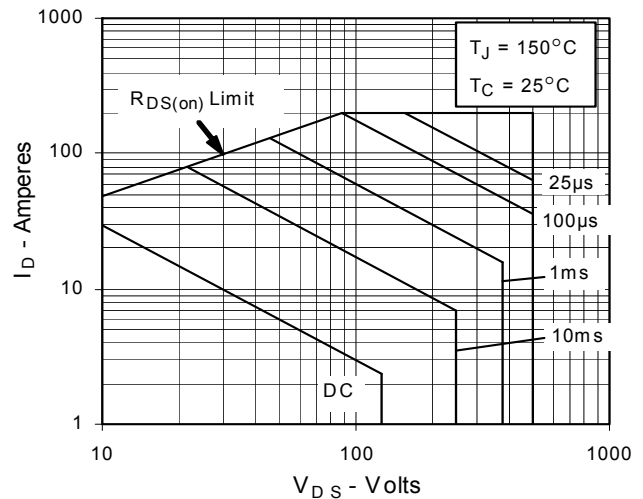
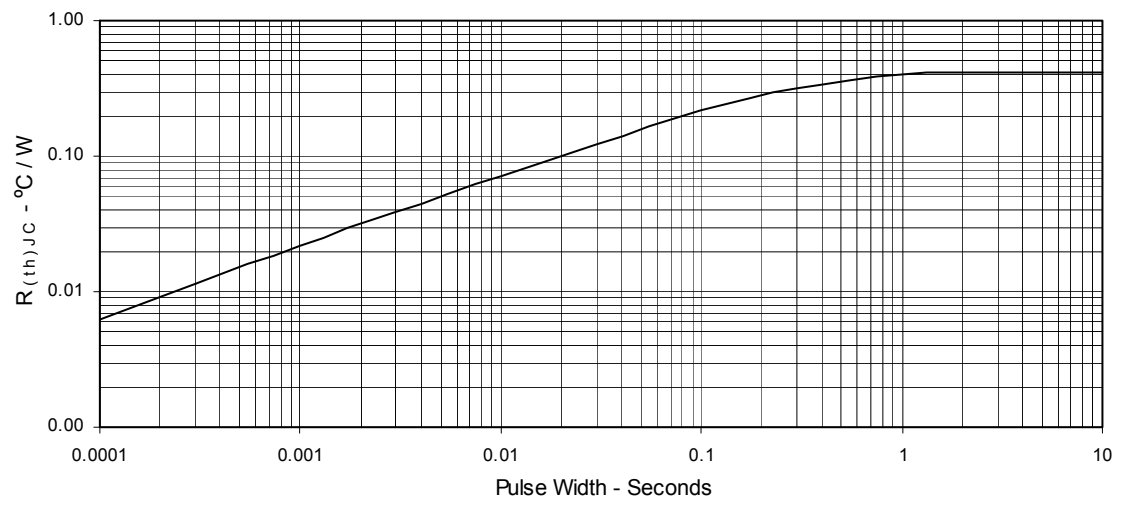


Fig. 13. Maximum Transient Thermal Resistance





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