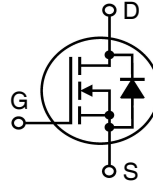


**Q3-Class
HiperFET™
Power MOSFET**

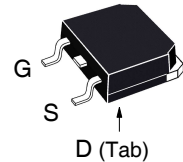
**IXFT15N100Q3
IXFH15N100Q3**

N-Channel Enhancement Mode
Avalanche Rated
Fast Intrinsic Rectifier

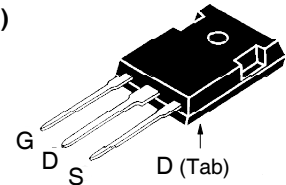


$V_{DSS} = 1000V$
 $I_{D25} = 15A$
 $R_{DS(on)} \leq 1.05\Omega$
 $t_{rr} \leq 250ns$

TO-268
(IXFT)



TO-247
(IXFH)



G = Gate D = Drain
S = Source Tab = Drain

| Symbol | Test Conditions | Maximum Ratings | |
|------------|--|-----------------|------------|
| V_{DSS} | $T_J = 25^\circ C$ to $150^\circ C$ | 1000 | V |
| V_{DGR} | $T_J = 25^\circ C$ to $150^\circ C$, $R_{GS} = 1M\Omega$ | 1000 | V |
| V_{GSS} | Continuous | ± 30 | V |
| V_{GSM} | Transient | ± 40 | V |
| I_{D25} | $T_C = 25^\circ C$ | 15 | A |
| I_{DM} | $T_C = 25^\circ C$, Pulse Width Limited by T_{JM} | 45 | A |
| I_A | $T_C = 25^\circ C$ | 7.5 | A |
| E_{AS} | $T_C = 25^\circ C$ | 1.0 | J |
| dv/dt | $I_S \leq I_{DM}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ C$ | 50 | V/ns |
| P_D | $T_C = 25^\circ C$ | 690 | W |
| T_J | | -55 ... +150 | $^\circ C$ |
| T_{JM} | | 150 | $^\circ C$ |
| T_{stg} | | -55 ... +150 | $^\circ C$ |
| T_L | Maximum Lead Temperature for Soldering | 300 | $^\circ C$ |
| T_{SOLD} | 1.6 mm (0.062in.) from Case for 10s | 260 | $^\circ C$ |
| M_d | Mounting Torque (TO-247) | 1.13 / 10 | Nm/lb.in. |
| Weight | TO-268 | 4.0 | g |
| | TO-247 | 6.0 | g |

| Symbol | Test Conditions ($T_J = 25^\circ C$ Unless Otherwise Specified) | Characteristic Values | | |
|--------------|---|-----------------------|------|----------------------|
| | | Min. | Typ. | Max. |
| BV_{DSS} | $V_{GS} = 0V$, $I_D = 1mA$ | 1000 | | V |
| $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D = 4mA$ | 3.5 | | 6.5 V |
| I_{GSS} | $V_{GS} = \pm 30V$, $V_{DS} = 0V$ | | | ± 100 nA |
| I_{DSS} | $V_{DS} = V_{DSS}$, $V_{GS} = 0V$ $T_J = 125^\circ C$ | | | 25 μA 1.5 mA |
| $R_{DS(on)}$ | $V_{GS} = 10V$, $I_D = 0.5 \cdot I_{D25}$, Note 1 | | | 1.05 Ω |

Features

- Low Intrinsic Gate Resistance
- International Standard Packages
- Low Package Inductance
- Fast Intrinsic Rectifier
- Low $R_{DS(on)}$ and Q_G

Advantages

- High Power Density
- Easy to Mount
- Space Savings

Applications

- DC-DC Converters
- Battery Chargers
- Switch-Mode and Resonant-Mode Power Supplies
- DC Choppers
- Temperature and Lighting Controls

| Symbol | Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified) | Characteristic Values | | |
|--------------|--|-----------------------|------|-------------------------|
| | | Min. | Typ. | Max. |
| g_{fs} | $V_{DS} = 20\text{V}, I_D = 0.5 \cdot I_{D25}$, Note 1 | 7.5 | 12.5 | S |
| C_{iss} | } $V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$ | | 3250 | pF |
| C_{oss} | | | 265 | pF |
| C_{rss} | | | 24 | pF |
| R_{Gi} | Gate Input Resistance | | 0.20 | Ω |
| $t_{d(on)}$ | } Resistive Switching Times $V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 \cdot I_{D25}$ $R_G = 2\Omega$ (External) | | 28 | ns |
| t_r | | | 10 | ns |
| $t_{d(off)}$ | | | 30 | ns |
| t_f | | | 8 | ns |
| $Q_{g(on)}$ | } $V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 \cdot I_{D25}$ | | 64 | nC |
| Q_{gs} | | | 23 | nC |
| Q_{gd} | | | 27 | nC |
| R_{thJC} | | | | 0.18 $^\circ\text{C/W}$ |
| R_{thCS} | TO-247 | | 0.21 | $^\circ\text{C/W}$ |

Source-Drain Diode

| Symbol | Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified) | Characteristic Values | | |
|----------|--|-----------------------|------|--------|
| | | Min. | Typ. | Max. |
| I_S | $V_{GS} = 0\text{V}$ | | | 15 A |
| I_{SM} | Repetitive, Pulse Width Limited by T_{JM} | | | 60 A |
| V_{SD} | $I_F = I_S, V_{GS} = 0\text{V}$, Note 1 | | | 1.4 V |
| t_{rr} | } $I_F = 7.5\text{A}, -di/dt = 100\text{A}/\mu\text{s}$ $V_R = 100\text{V}, V_{GS} = 0\text{V}$ | | | 250 ns |
| I_{RM} | | | 7.6 | A |
| Q_{RM} | | | 660 | nC |

Note 1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

| | | | | | | | | | | |
|---|-----------|-----------|-----------|-----------|--------------|--------------|--------------|--------------|--------------|-------------|
| IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: | 4,835,592 | 4,931,844 | 5,049,961 | 5,237,481 | 6,162,665 | 6,404,065 B1 | 6,683,344 | 6,727,585 | 7,005,734 B2 | 7,157,338B2 |
| | 4,860,072 | 5,017,508 | 5,063,307 | 5,381,025 | 6,259,123 B1 | 6,534,343 | 6,710,405 B2 | 6,759,692 | 7,063,975 B2 | |
| | 4,881,106 | 5,034,796 | 5,187,117 | 5,486,715 | 6,306,728 B1 | 6,583,505 | 6,710,463 | 6,771,478 B2 | 7,071,537 | |

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

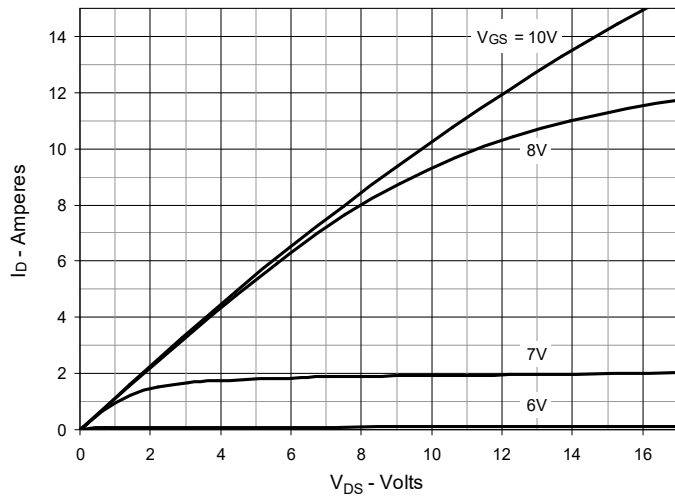


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

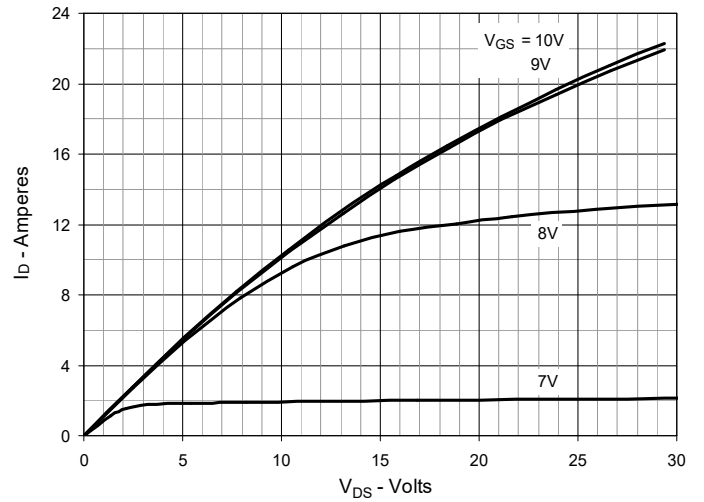


Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

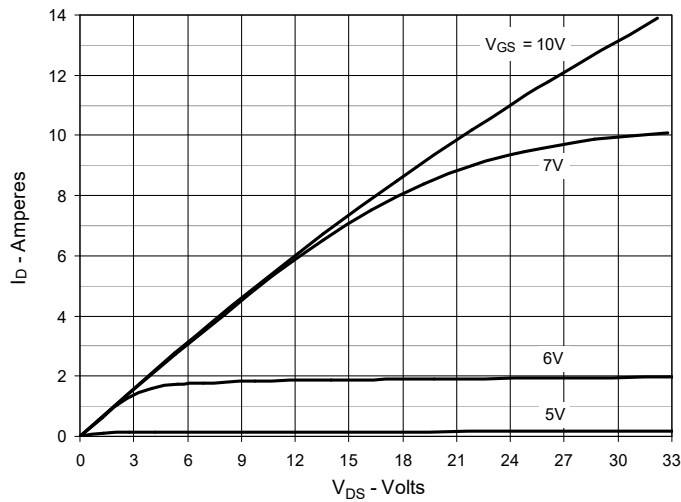


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 7.5\text{A}$ Value vs. Junction Temperature

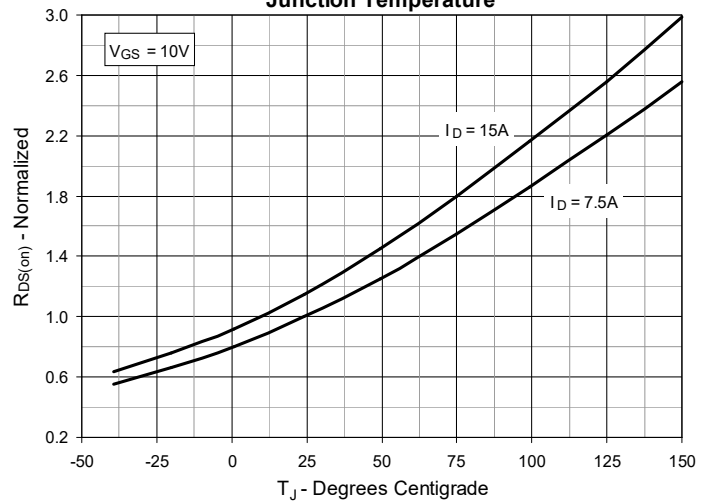


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 7.5\text{A}$ Value vs. Drain Current

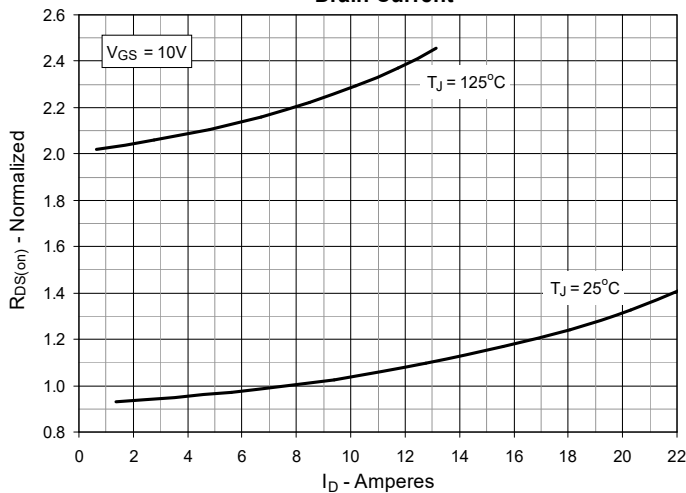


Fig. 6. Maximum Drain Current vs. Case Temperature

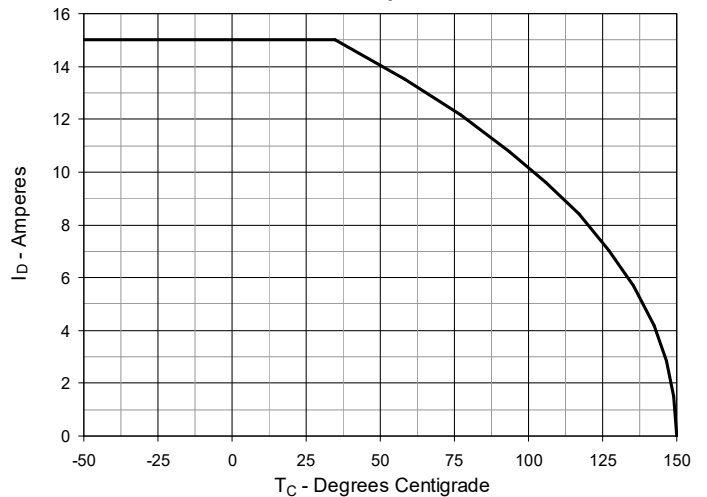


Fig. 7. Input Admittance

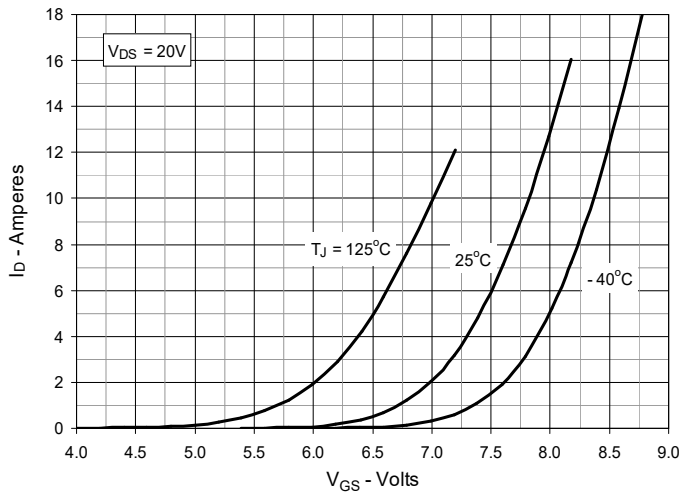


Fig. 8. Transconductance

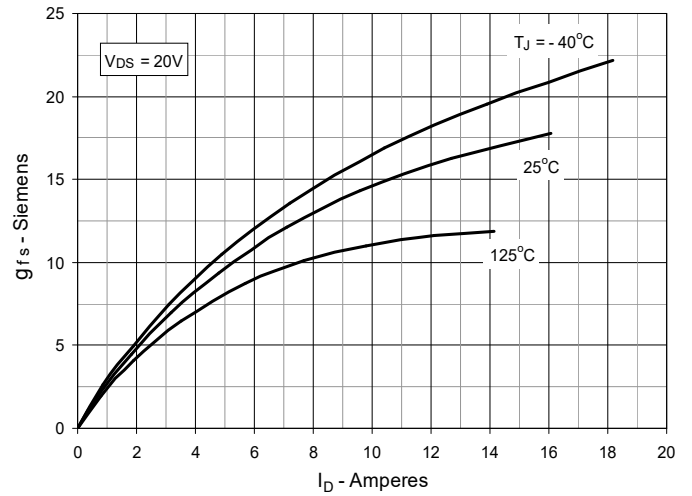


Fig. 9. Forward Voltage Drop of Intrinsic Diode

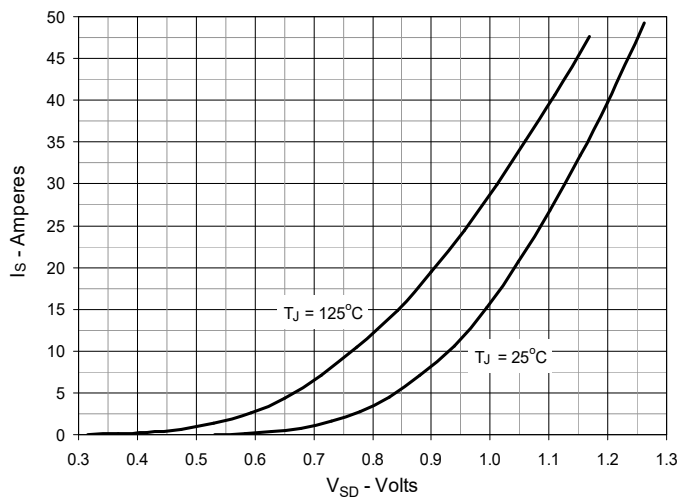


Fig. 10. Gate Charge

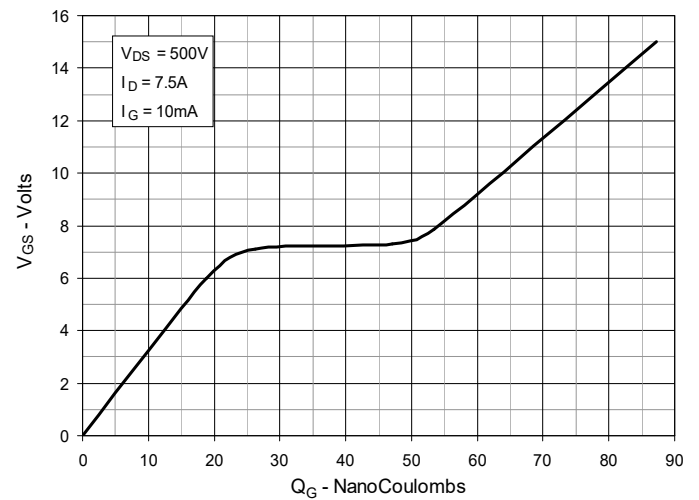


Fig. 11. Capacitance

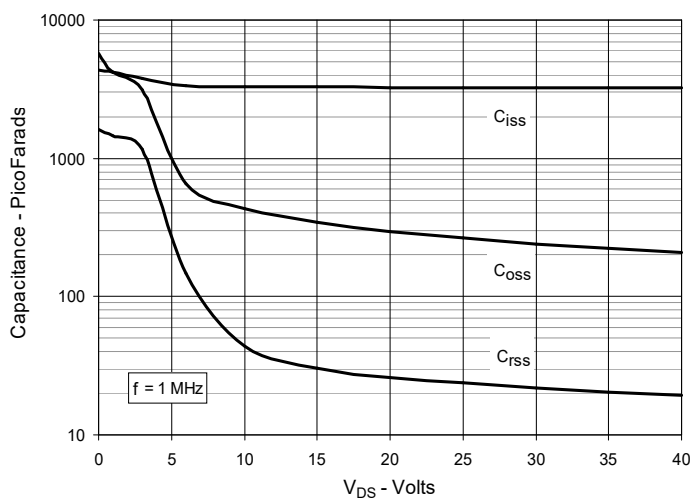


Fig. 12. Forward-Bias Safe Operating Area

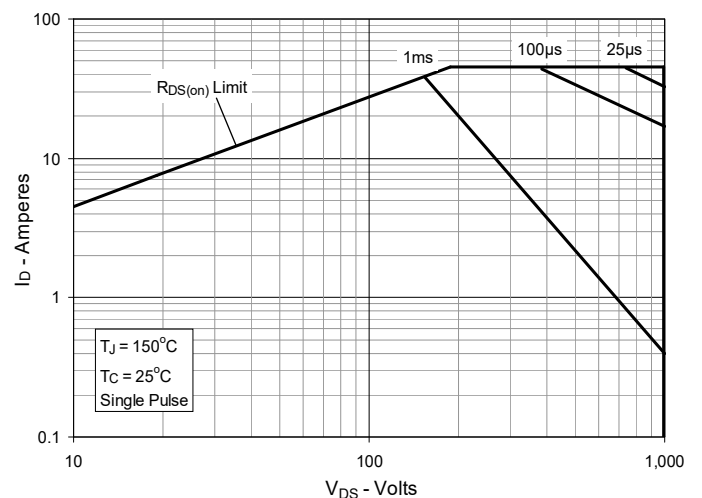
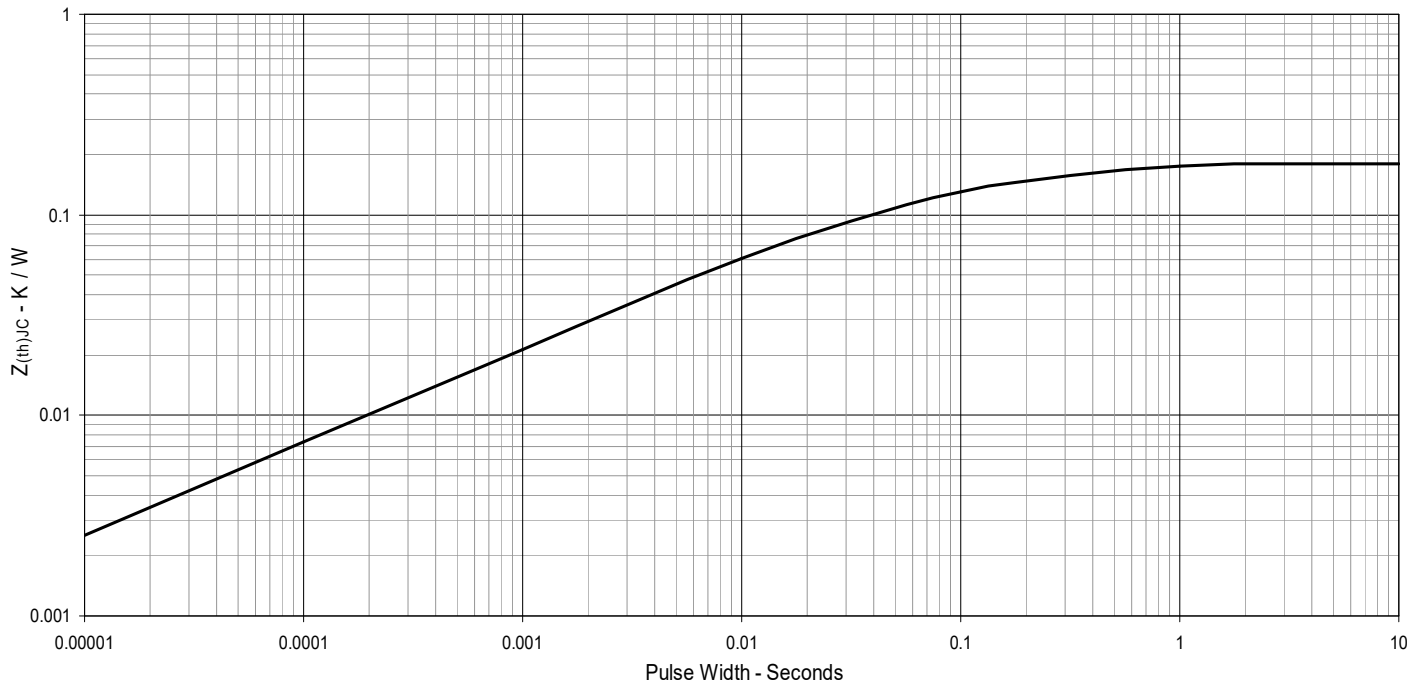
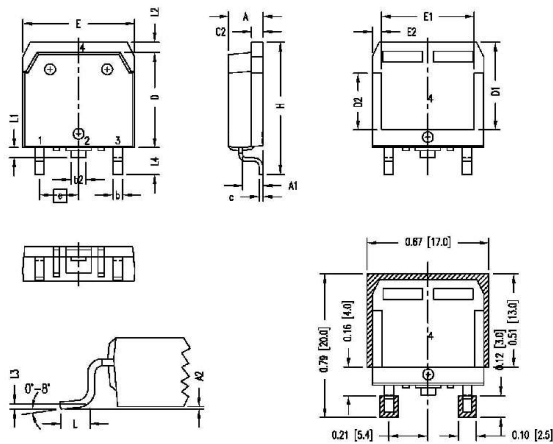


Fig. 13. Maximum Transient Thermal Impedance



TO-268 Outline

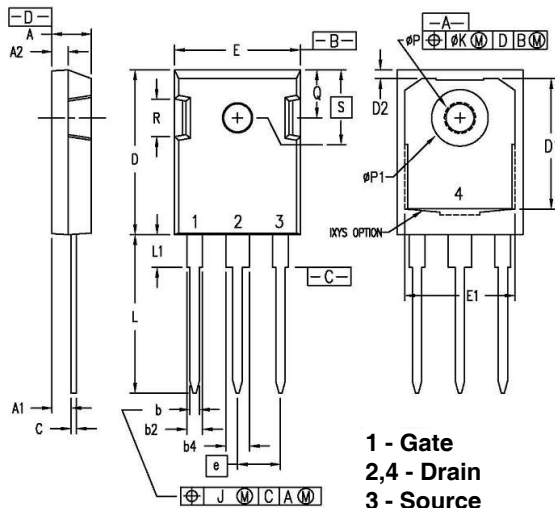


- 1 - Gate
- 2,4 - Drain
- 3 - Source

| SYMBOL | INCHES | | MILLIMETERS | |
|--------|----------|------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | .193 | .201 | 4.90 | 5.10 |
| A1 | .106 | .114 | 2.70 | 2.90 |
| A2 | .001 | .010 | 0.02 | 0.25 |
| b | .045 | .057 | 1.15 | 1.45 |
| b2 | .075 | .083 | 1.90 | 2.10 |
| C | .016 | .026 | 0.40 | 0.65 |
| C2 | .057 | .063 | 1.45 | 1.60 |
| D | .543 | .551 | 13.80 | 14.00 |
| D1 | .488 | .500 | 12.40 | 12.70 |
| D2 | .320 | .335 | 8.13 | 8.50 |
| E | .624 | .632 | 15.85 | 16.05 |
| E1 | .524 | .535 | 13.30 | 13.60 |
| E2 | .045 | .055 | 1.14 | 1.39 |
| e | .215 BSC | | 5.45 BSC | |
| H | .736 | .752 | 18.70 | 19.10 |
| L | .094 | .106 | 2.40 | 2.70 |
| L1 | .047 | .055 | 1.20 | 1.40 |
| L2 | .039 | .045 | 1.00 | 1.15 |
| L3 | .010 BSC | | 0.25 BSC | |
| L4 | .150 | .161 | 3.80 | 4.10 |

NOTE: ALL METAL SURFACE ARE MATTE PURE TIN PLATED EXCEPT TRIM AREA
Pb PLATING THICKNESS (4 - 20 um)

TO-247 Outline



- 1 - Gate
- 2,4 - Drain
- 3 - Source

| SYM | INCHES | | MILLIMETERS | |
|-----|----------|------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | .190 | .205 | 4.83 | 5.21 |
| A1 | .090 | .100 | 2.29 | 2.54 |
| A2 | .075 | .085 | 1.91 | 2.16 |
| b | .045 | .055 | 1.14 | 1.40 |
| b2 | .075 | .087 | 1.91 | 2.20 |
| b4 | .115 | .126 | 2.92 | 3.20 |
| C | .024 | .031 | 0.61 | 0.80 |
| D | .819 | .840 | 20.80 | 21.34 |
| D1 | .650 | .690 | 16.51 | 17.53 |
| D2 | .035 | .050 | 0.89 | 1.27 |
| E | .620 | .635 | 15.75 | 16.13 |
| E1 | .545 | .565 | 13.84 | 14.35 |
| e | .215 BSC | | 5.45 BSC | |
| J | -- | .010 | -- | 0.25 |
| K | -- | .025 | -- | 0.64 |
| L | .780 | .810 | 19.81 | 20.57 |
| L1 | .150 | .170 | 3.81 | 4.32 |
| øP | .140 | .144 | 3.55 | 3.65 |
| øP1 | .275 | .290 | 6.99 | 7.37 |
| R | .170 | .190 | 4.32 | 4.83 |
| S | .242 BSC | | 6.15 BSC | |

NOTE: This drawing will meet all dimensions requirement of JEDEC outlines TO-247 AD (R-PSIP-F3)



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