

HiPerFET™

Power MOSFETs

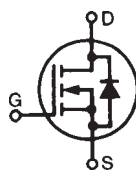
Single Die MOSFET

N-Channel Enhancement Mode

Avalanche Rated

High dV/dt, Low t_{rr}

IXFN280N07

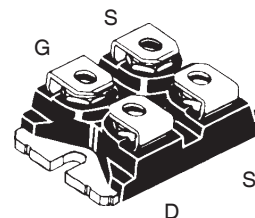


$$\begin{aligned} V_{DSS} &= 70V \\ I_{D25} &= 280A \\ R_{DS(on)} &\leq 5m\Omega \\ t_{rr} &\leq 250ns \end{aligned}$$

miniBLOC, SOT-227 B (IXFN)



E153432



G = Gate
S = Source

D = Drain

Either Source terminal S can be used as the Source terminal or the Kelvin Source (gate return) terminal.

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	70	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C , $R_{GS} = 1M\Omega$	70	V
V_{GSS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_C = 25^\circ\text{C}$	280	A
$I_{L(RMS)}$	Terminal current limit	100	A
I_{DM}	$T_C = 25^\circ\text{C}$, pulse width limited by T_{JM}	1120	A
I_{AR}	$T_C = 25^\circ\text{C}$	180	A
E_{AR}	$T_C = 25^\circ\text{C}$	60	mJ
E_{AS}	$T_C = 25^\circ\text{C}$	3	J
dV/dt	$I_S \leq I_{DM}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ\text{C}$	20	V/ns
P_D	$T_C = 25^\circ\text{C}$	600	W
T_J		-55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		-55 ... +150	$^\circ\text{C}$
T_L	1.6mm (0.062 in.) from case for 10s	300	$^\circ\text{C}$
V_{ISOL}	50/60Hz, RMS $t = 1\text{min}$	2500	V~
	$I_{ISOL} \leq 1\text{mA}$ $t = 1\text{s}$	3000	V~
M_d	Mounting torque	1.5/13	Nm/lb.in.
	Terminal connection torque	1.3/ 11.5	Nm/lb.in.
Weight		30	g

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V$, $I_D = 3\text{mA}$	70		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 8\text{mA}$	2.0		4.0 V
I_{GSS}	$V_{GS} = \pm 20V$, $V_{DS} = 0V$			± 200 nA
I_{DSS}	$V_{DS} = V_{DSS}$ $V_{GS} = 0V$ $T_J = 125^\circ\text{C}$			100 μA 2 mA
$R_{DS(on)}$	$V_{GS} = 10V$, $I_D = 120A$, Note 1			5 m Ω

Features

- International standard package
- miniBLOC with Aluminium nitride isolation
- Low $R_{DS(on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped inductive switching (UIS) rated
- Low package inductance
- Fast intrinsic Rectifier

Advantages

- Easy to mount
- Space savings
- High power density

Applications

- DC-DC converters
- Synchronous rectification
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- Temperature and lighting controls
- Low voltage relays

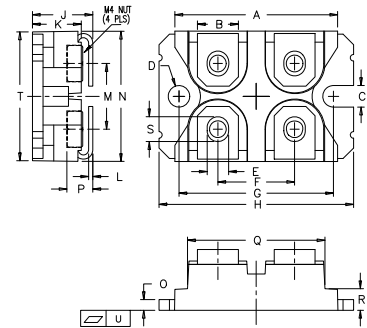
Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 15\text{V}$, $I_D = 60\text{A}$, Note 1	47	78	S
C_{iss}	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$		11.5	nF
C_{oss}			4800	pF
C_{rss}			2650	pF
R_{Gi}	Gate input resistance		0.74	Ω
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 90\text{A}$ $R_G = 1\Omega$ (External)		40	ns
t_r			90	ns
$t_{d(off)}$			85	ns
t_f			50	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}$, $V_{DS} = 35\text{V}$, $I_D = 100\text{A}$		360	nC
Q_{gs}			60	nC
Q_{gd}			182	nC
R_{thJC}			0.22	$^\circ\text{C/W}$
R_{thCS}			0.05	$^\circ\text{C/W}$

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
I_S	$V_{GS} = 0\text{V}$			280 A
I_{SM}	Repetitive, pulse width limited by T_{JM}			1120 A
V_{SD}	$I_F = 100\text{A}$, $V_{GS} = 0\text{V}$, Note 1			1.3 V
t_{rr}	$I_F = 50\text{A}$, $-di/dt = 100\text{A}/\mu\text{s}$, $V_R = 50\text{V}$		1.2	250 ns
Q_{RM}				μC
I_{RM}				A

Note 1: Pulse test, $t \leq 300\mu\text{s}$; duty cycle, $d \leq 2\%$.

SOT-227B Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.240	1.255	31.50	31.88
B	.307	.323	7.80	8.20
C	.161	.169	4.09	4.29
D	.161	.169	4.09	4.29
E	.161	.169	4.09	4.29
F	.587	.595	14.91	15.11
G	1.186	1.193	30.12	30.30
H	1.496	1.505	38.00	38.23
J	.460	.481	11.68	12.22
K	.351	.378	8.92	9.60
L	.030	.033	0.76	0.84
M	.496	.506	12.60	12.85
N	.990	1.001	25.15	25.42
O	.078	.084	1.98	2.13
P	.195	.235	4.95	5.97
Q	1.045	1.059	26.54	26.90
R	.155	.174	3.94	4.42
S	.186	.191	4.72	4.85
T	.968	.987	24.59	25.07
U	-.002	.004	-0.05	0.1

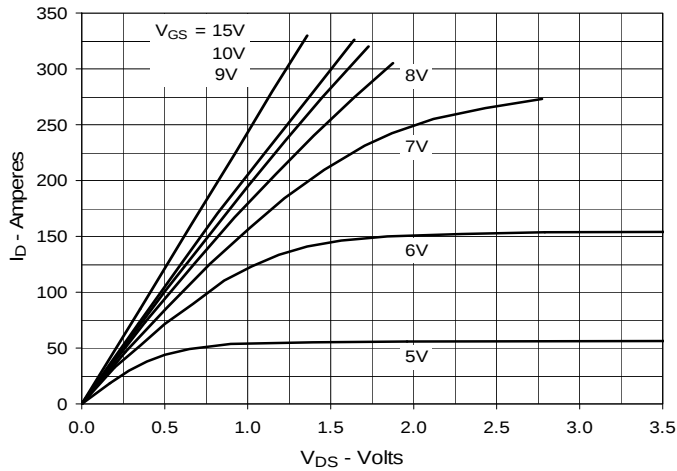
PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

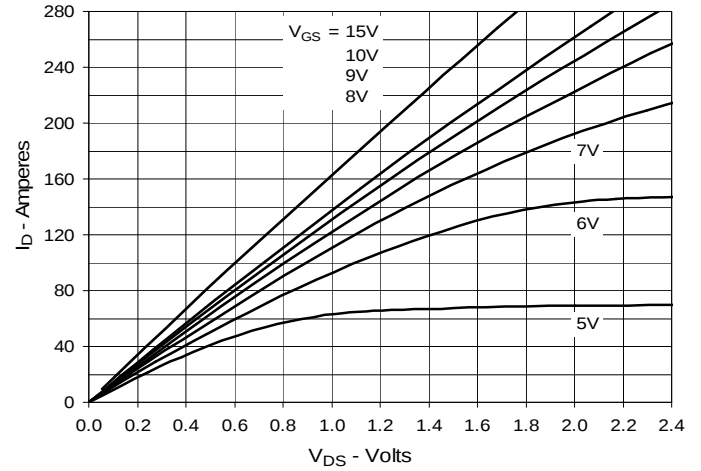
IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
	4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

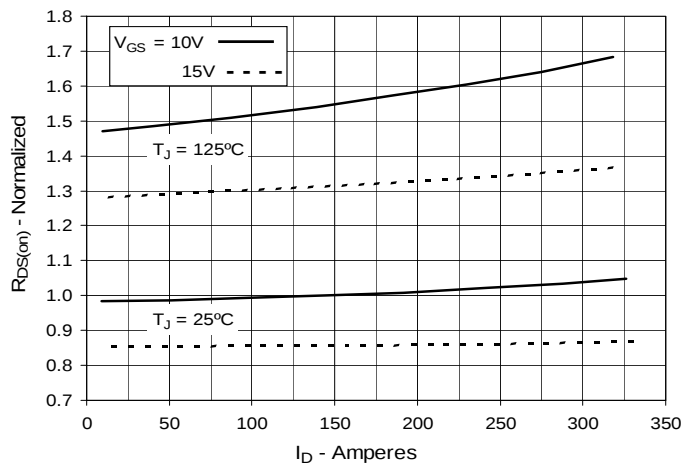
**Fig. 1. Extended Output Characteristics
@ 25°C**



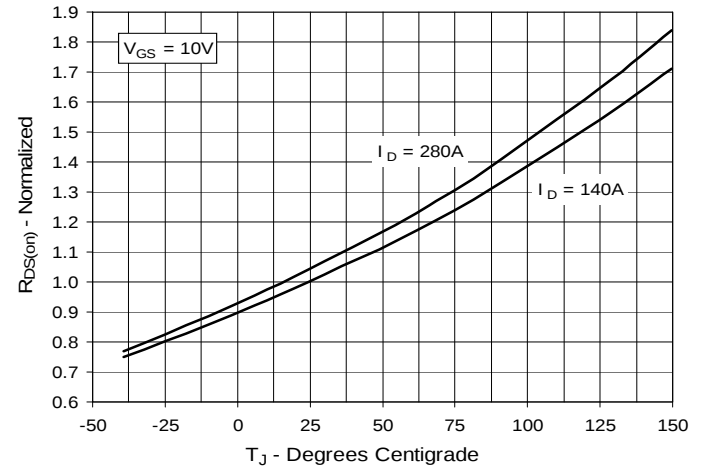
**Fig. 2. Output Characteristics
@ 125°C**



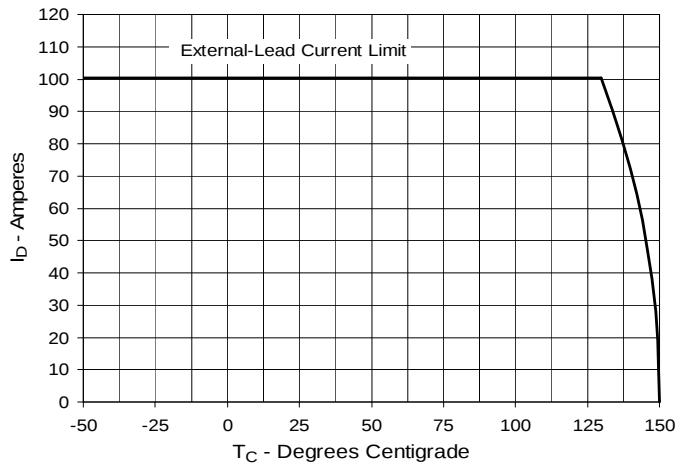
**Fig. 3. $R_{DS(on)}$ Normalized to $I_D = 140\text{A}$ Value
vs. Drain Current**



**Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 140\text{A}$ Value
vs. Junction Temperature**



**Fig. 5. Maximum Drain Current vs.
Case Temperature**



**Fig. 6. Forward Voltage Drop of
Intrinsic Diode**

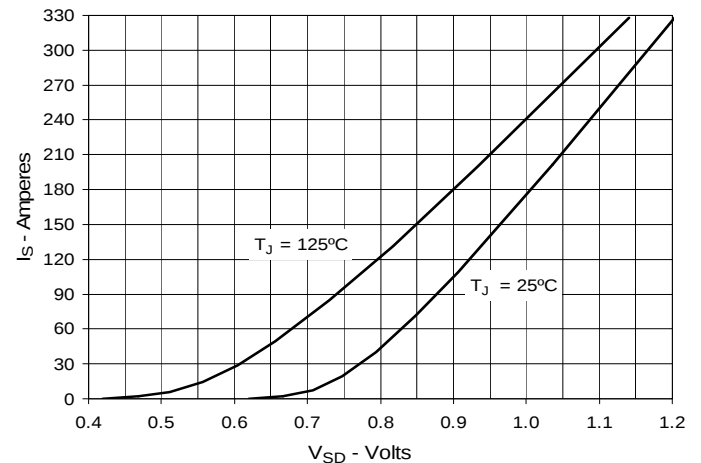
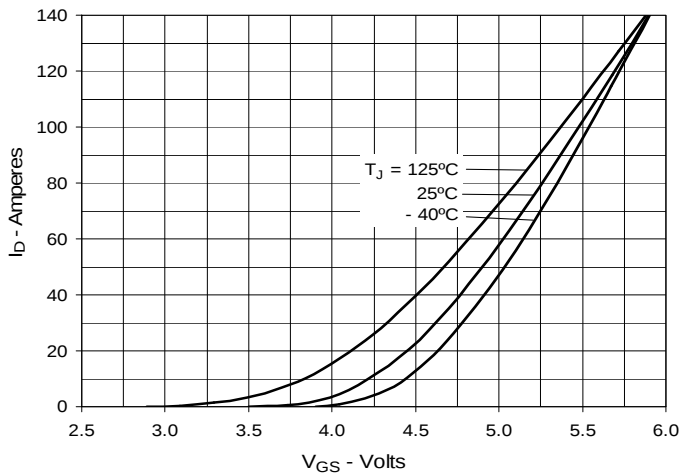
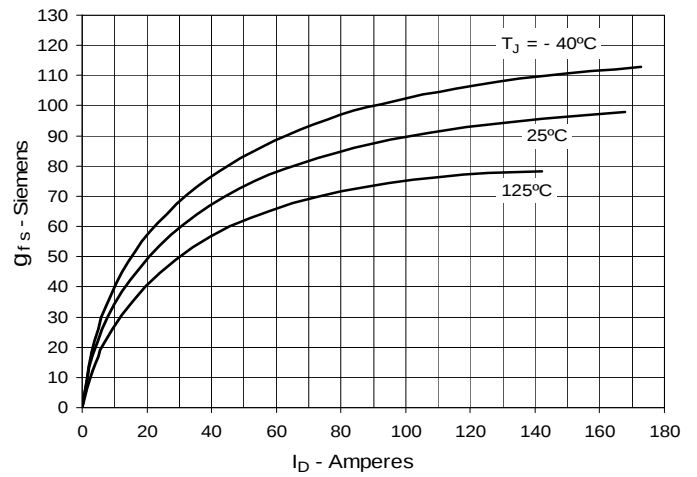
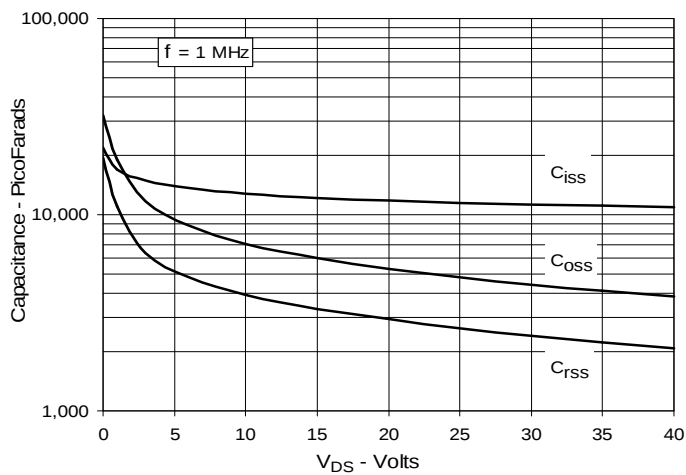
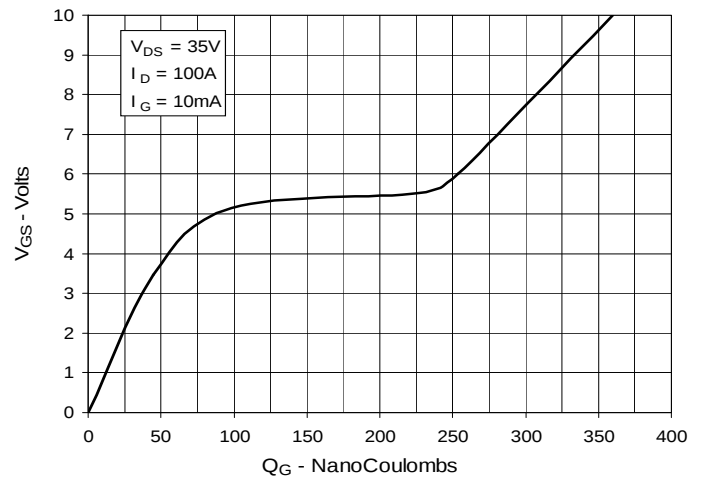
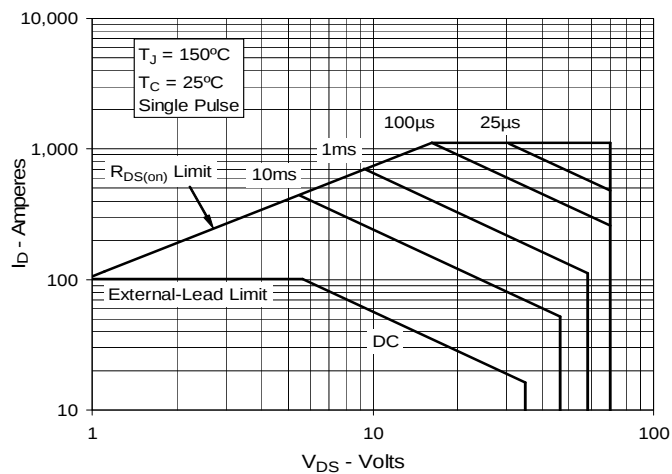
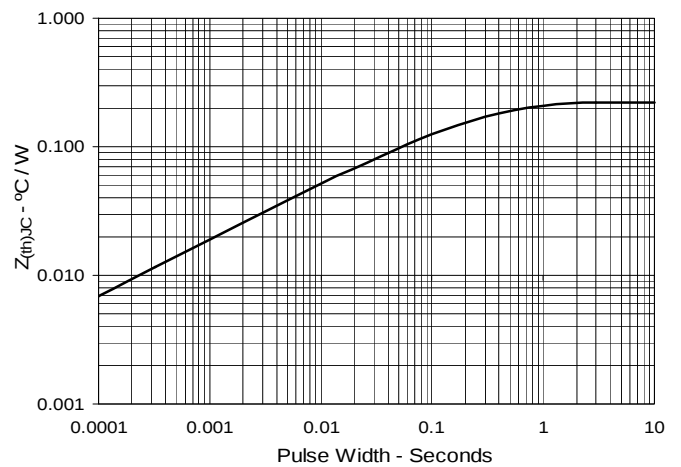


Fig. 7. Input Admittance

Fig. 8. Transconductance

Fig. 9. Capacitance

Fig. 10. Gate Charge

Fig. 11. Forward-Bias Safe Operating Area

Fig. 12. Maximum Transient Thermal Impedance




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