

Thyristor \ Diode Module

$$V_{RRM} = 2 \times 1800 \text{ V}$$

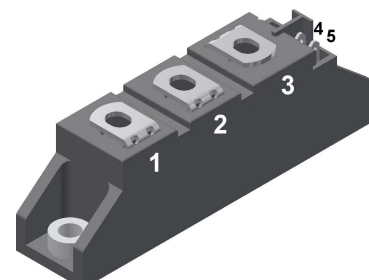
$$I_{TAV} = 85 \text{ A}$$

$$V_T = 1.34 \text{ V}$$

Phase leg

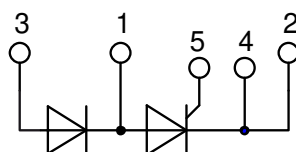
Part number

MCD72-18io1B



Backside: isolated

 E72873



Features / Advantages:

- Thyristor for line frequency
- Planar passivated chip
- Long-term stability
- Direct Copper Bonded Al₂O₃-ceramic

Applications:

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

Package: TO-240AA

- Isolation Voltage: 4800 V~
- Industry standard outline
- RoHS compliant
- Soldering pins for PCB mounting
- Base plate: DCB ceramic
- Reduced weight
- Advanced power cycling

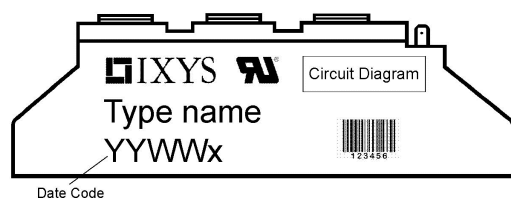
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Rectifier				Ratings			
Symbol	Definition	Conditions		min.	typ.	max.	Unit
$V_{RSM/DSM}$	max. non-repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}\text{C}$				1900	V
$V_{RRM/DRM}$	max. repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}\text{C}$				1800	V
$I_{R/D}$	reverse current, drain current	$V_{R/D} = 1800\text{ V}$	$T_{VJ} = 25^{\circ}\text{C}$			200	μA
		$V_{R/D} = 1800\text{ V}$	$T_{VJ} = 125^{\circ}\text{C}$			5	mA
V_T	forward voltage drop	$I_T = 150\text{ A}$	$T_{VJ} = 25^{\circ}\text{C}$			1.34	V
		$I_T = 300\text{ A}$				1.74	V
		$I_T = 150\text{ A}$	$T_{VJ} = 125^{\circ}\text{C}$			1.34	V
		$I_T = 300\text{ A}$				1.82	V
I_{TAV}	average forward current	$T_C = 85^{\circ}\text{C}$	$T_{VJ} = 125^{\circ}\text{C}$			85	A
$I_{T(RMS)}$	RMS forward current	180° sine				133	A
V_{T0}	threshold voltage	for power loss calculation only	$T_{VJ} = 125^{\circ}\text{C}$			0.85	V
r_T	slope resistance					3.2	m Ω
R_{thJC}	thermal resistance junction to case					0.3	K/W
R_{thCH}	thermal resistance case to heatsink				0.2		K/W
P_{tot}	total power dissipation		$T_C = 25^{\circ}\text{C}$			333	W
I_{TSM}	max. forward surge current	$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}\text{C}$			1.70	kA
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$			1.84	kA
		$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 125^{\circ}\text{C}$			1.45	kA
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$			1.56	kA
I^2t	value for fusing	$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}\text{C}$			14.5	kA ² s
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$			14.0	kA ² s
		$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 125^{\circ}\text{C}$			10.4	kA ² s
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$			10.1	kA ² s
C_J	junction capacitance	$V_R = 400\text{ V}$ $f = 1\text{ MHz}$	$T_{VJ} = 25^{\circ}\text{C}$		119		pF
P_{GM}	max. gate power dissipation	$t_p = 30\text{ }\mu\text{s}$	$T_C = 125^{\circ}\text{C}$			10	W
		$t_p = 300\text{ }\mu\text{s}$				5	W
P_{GAV}	average gate power dissipation					0.5	W
$(di/dt)_{cr}$	critical rate of rise of current	$T_{VJ} = 125^{\circ}\text{C}; f = 50\text{ Hz}$ repetitive, $I_T = 250\text{ A}$				150	A/ μs
		$t_p = 200\text{ }\mu\text{s}; di_G/dt = 0.45\text{ A}/\mu\text{s};$ $I_G = 0.45\text{ A}; V = \frac{2}{3} V_{DRM}$ non-repet., $I_T = 85\text{ A}$				500	A/ μs
$(dv/dt)_{cr}$	critical rate of rise of voltage	$V = \frac{2}{3} V_{DRM}$	$T_{VJ} = 125^{\circ}\text{C}$			1000	V/ μs
		$R_{GK} = \infty$; method 1 (linear voltage rise)					
V_{GT}	gate trigger voltage	$V_D = 6\text{ V}$	$T_{VJ} = 25^{\circ}\text{C}$			2.5	V
			$T_{VJ} = -40^{\circ}\text{C}$			2.6	V
I_{GT}	gate trigger current	$V_D = 6\text{ V}$	$T_{VJ} = 25^{\circ}\text{C}$			150	mA
			$T_{VJ} = -40^{\circ}\text{C}$			200	mA
V_{GD}	gate non-trigger voltage	$V_D = \frac{2}{3} V_{DRM}$	$T_{VJ} = 125^{\circ}\text{C}$			0.2	V
I_{GD}	gate non-trigger current					10	mA
I_L	latching current	$t_p = 10\text{ }\mu\text{s}$	$T_{VJ} = 25^{\circ}\text{C}$			450	mA
		$I_G = 0.45\text{ A}; di_G/dt = 0.45\text{ A}/\mu\text{s}$					
I_H	holding current	$V_D = 6\text{ V}$ $R_{GK} = \infty$	$T_{VJ} = 25^{\circ}\text{C}$			200	mA
t_{gd}	gate controlled delay time	$V_D = \frac{1}{2} V_{DRM}$	$T_{VJ} = 25^{\circ}\text{C}$			2	μs
		$I_G = 0.45\text{ A}; di_G/dt = 0.45\text{ A}/\mu\text{s}$					
t_q	turn-off time	$V_R = 100\text{ V}; I_T = 150\text{ A}; V = \frac{2}{3} V_{DRM}$ $T_{VJ} = 100^{\circ}\text{C}$ $di/dt = 10\text{ A}/\mu\text{s}$ $dv/dt = 20\text{ V}/\mu\text{s}$ $t_p = 200\text{ }\mu\text{s}$			185		μs

Package TO-240AA				Ratings			
Symbol	Definition	Conditions		min.	typ.	max.	Unit
I_{RMS}	RMS current	per terminal				200	A
T_{VJ}	virtual junction temperature			-40		125	°C
T_{op}	operation temperature			-40		100	°C
T_{stg}	storage temperature			-40		125	°C
Weight					81		g
M_D	mounting torque			2.5		4	Nm
M_T	terminal torque			2.5		4	Nm
$d_{Spp/Apb}$	creepage distance on surface striking distance through air	terminal to terminal	13.0	9.7			mm
$d_{Spb/Apb}$		terminal to backside	16.0	16.0			mm
V_{ISOL}	isolation voltage	t = 1 second	50/60 Hz, RMS; $I_{ISOL} \leq 1$ mA	4800			V
		t = 1 minute		4000			V

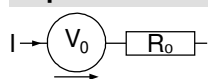


Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	MCD72-18io1B	MCD72-18io1B	Box	36	494194

Equivalent Circuits for Simulation

* on die level

 $T_{VJ} = 125^{\circ}\text{C}$

				Thyristor
$V_{0\max}$	threshold voltage	0.85		V
$R_{0\max}$	slope resistance *	2		mΩ

Technical drawing of a mechanical component (Fig. 1) showing a side view with dimensions and a cross-section view (A-A) showing internal features.

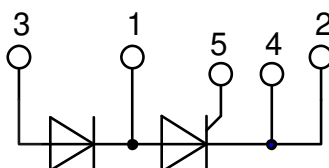
Dimensions:

- Overall length: 92 ± 0.5
- Distance from left end to center of first hole: 80 ± 0.3
- Distance from center of first hole to center of second hole: 10
- Distance from center of second hole to center of third hole: 10
- Distance from center of third hole to center of fourth hole: 10
- Distance from center of fourth hole to center of fifth hole: 10
- Distance from center of fifth hole to right end: 6
- Overall width: 20.8 ± 0.25
- Distance from top edge to center of first hole: 14.8
- Distance from center of first hole to center of second hole: 10 ± 0.1
- Distance from center of second hole to center of third hole: 5.5 ± 0.1
- Distance from center of third hole to center of fourth hole: 5.5 ± 0.1
- Distance from center of fourth hole to center of fifth hole: 5.5 ± 0.1
- Distance from center of fifth hole to right end: 5.5 ± 0.1
- Distance from left end to center of first hole: 14.8
- Distance from center of first hole to center of second hole: 10 ± 0.1
- Distance from center of second hole to center of third hole: 5.5 ± 0.1
- Distance from center of third hole to center of fourth hole: 5.5 ± 0.1
- Distance from center of fourth hole to center of fifth hole: 5.5 ± 0.1
- Distance from center of fifth hole to right end: 5.5 ± 0.1
- Distance from left end to center of first hole: 14.8
- Distance from center of first hole to center of second hole: 10 ± 0.1
- Distance from center of second hole to center of third hole: 5.5 ± 0.1
- Distance from center of third hole to center of fourth hole: 5.5 ± 0.1
- Distance from center of fourth hole to center of fifth hole: 5.5 ± 0.1
- Distance from center of fifth hole to right end: 5.5 ± 0.1

Internal Features (Cross-section A-A):

- Internal hole diameter: $\varnothing 4.4$
- Internal hole length: 25 ± 0.3
- Internal hole position: 45 ± 0.3 from left end
- Internal hole diameter: $\varnothing 4.4$
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- Internal hole position: 45 ± 0.3 from left end
- Internal hole diameter: $\varnothing 4.4$
- Internal hole length: 25 ± 0.3
- Internal hole position: 45 ± 0.3 from left end
- Internal hole diameter: $\varnothing 4.4$
- Internal hole length: 25 ± 0.3
- Internal hole position: 45 ± 0.3 from left end

Keyed gate/cathode twin plugs with wire length = 350 mm, gate = white, cathode = red
Type ZY 200L (L = Left for pin pair 4/5) UL 758, style 3751



Thyristor

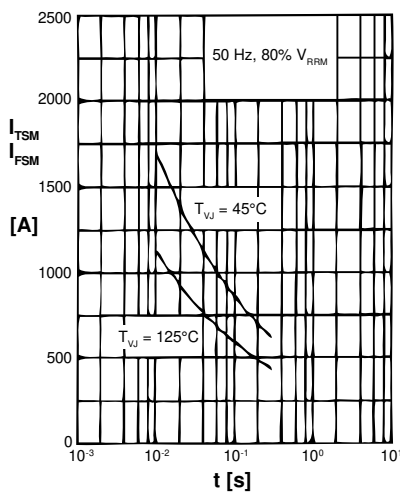


Fig. 1 Surge overload current
 I_{TSM} , I_{FSM} : Crest value, t: duration

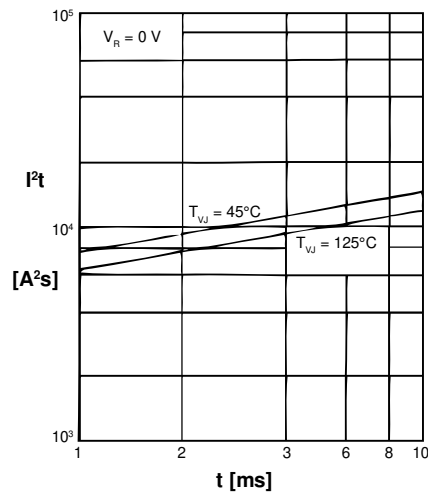


Fig. 2 I^2t versus time (1-10 ms)

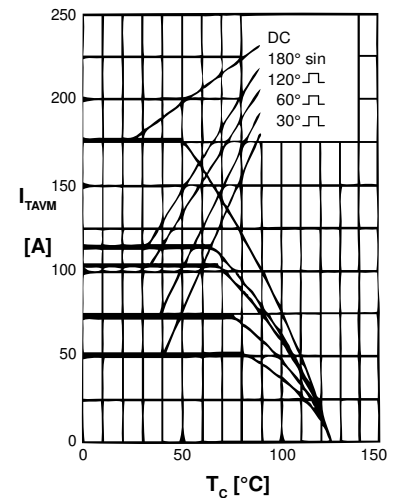


Fig. 3 Maximum forward current
 at case temperature

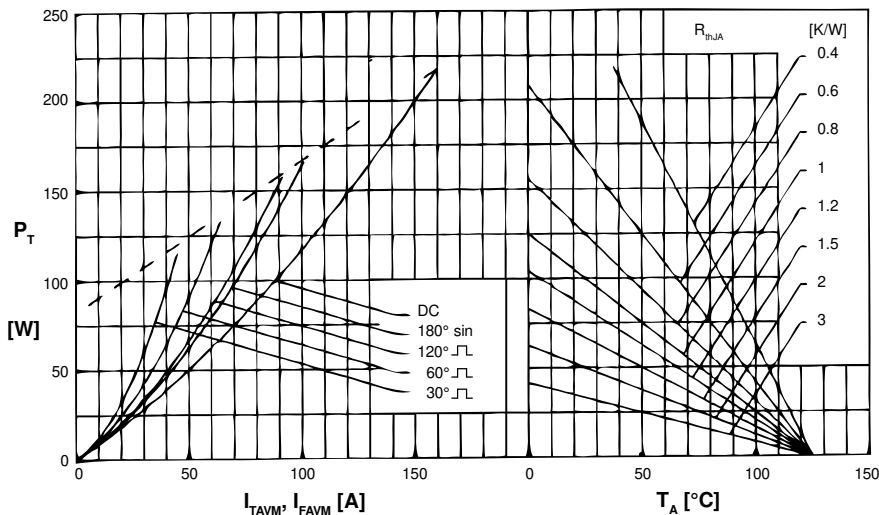


Fig. 4 Power dissipation vs. onstate current and ambient temperature (per thyristor/diode)

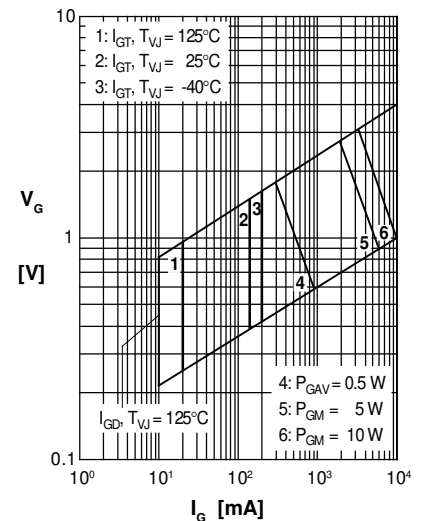


Fig. 5 Gate trigger characteristics

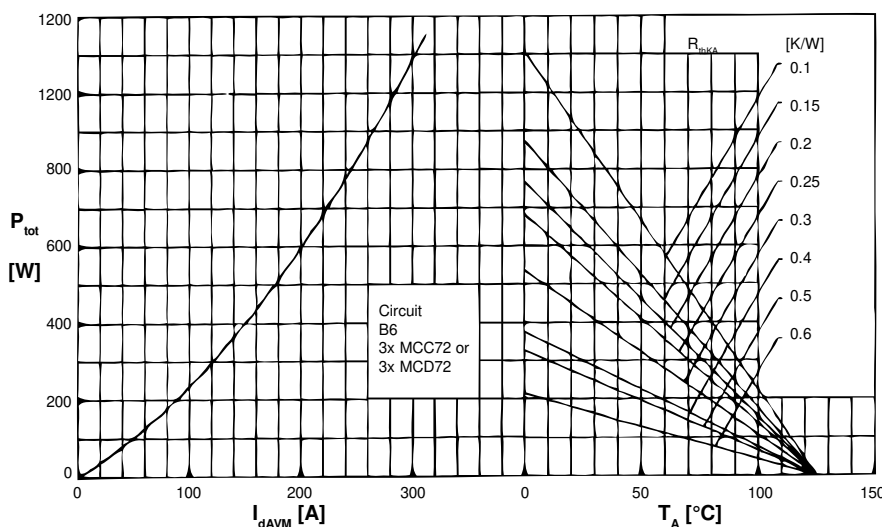


Fig. 6 Three phase rectifier bridge: Power dissipation versus direct output current and ambient temperature

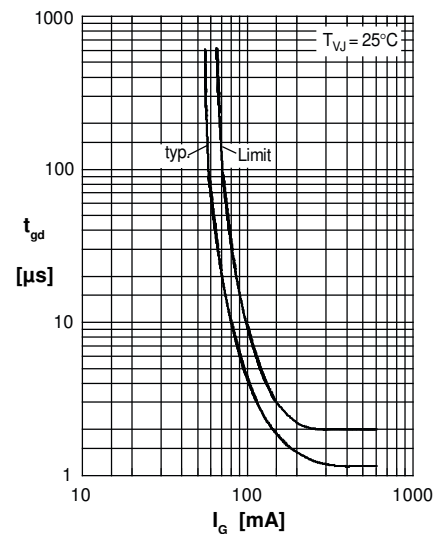


Fig. 7 Gate trigger delay time

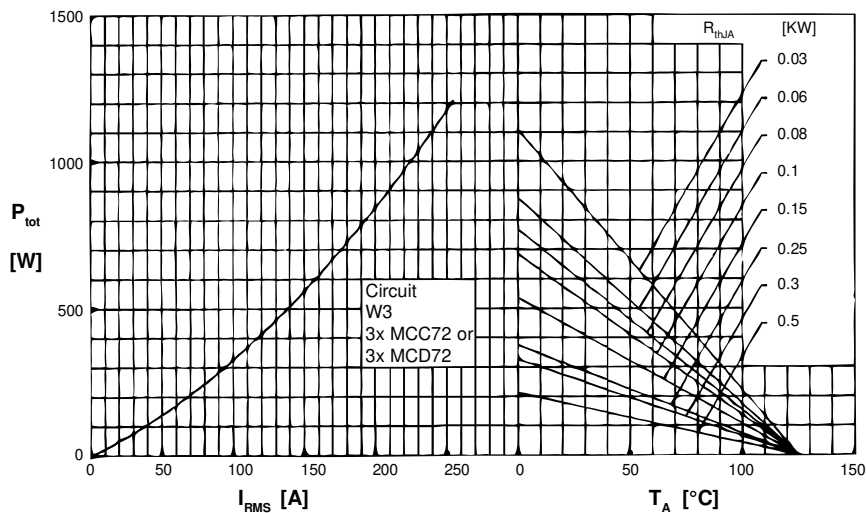
Rectifier


Fig. 8 Three phase AC-controller: Power dissipation versus RMS output current and ambient temperature

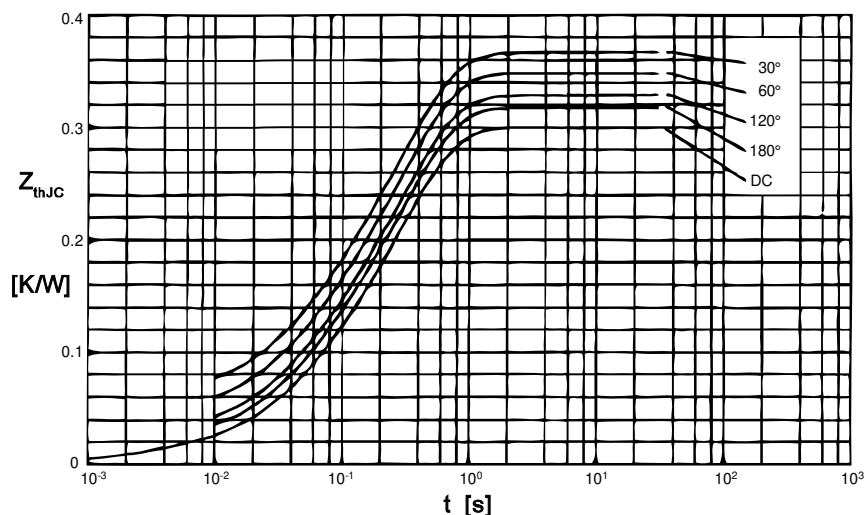


Fig. 9 Transient thermal impedance junction to case (per thyristor)

R_{thJC} for various conduction angles d :

d	R_{thJC} [K/W]
DC	0.30
180°	0.31
120°	0.33
60°	0.35
30°	0.37

Constants for Z_{thJC} calculation:

i	R_{thi} [K/W]	t_i [s]
1	0.008	0.0019
2	0.054	0.0470
3	0.238	0.3000

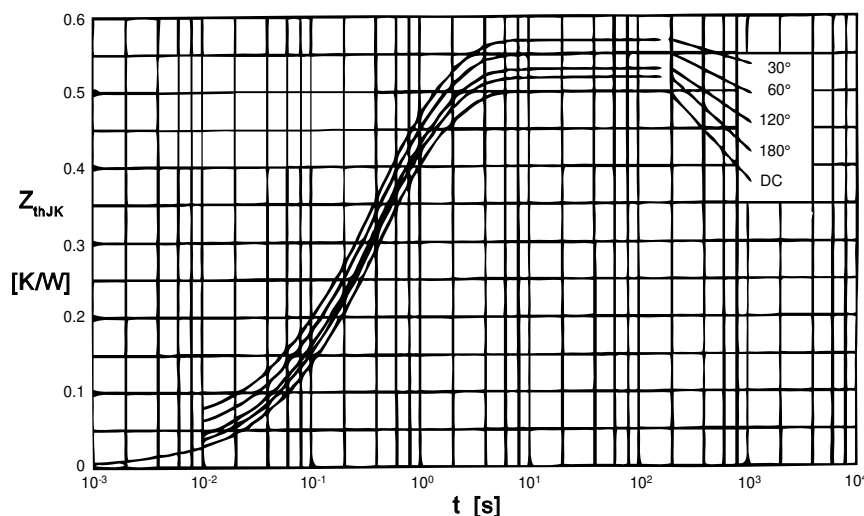


Fig. 10 Transient thermal impedance junction to heatsink (per thyristor)

R_{thJK} for various conduction angles d :

d	R_{thJK} [K/W]
DC	0.50
180°	0.51
120°	0.53
60°	0.55
30°	0.57

Constants for Z_{thJK} calculation:

i	R_{thi} [K/W]	t_i [s]
1	0.008	0.0019
2	0.054	0.0470
3	0.238	0.3000
4	0.200	1.2500