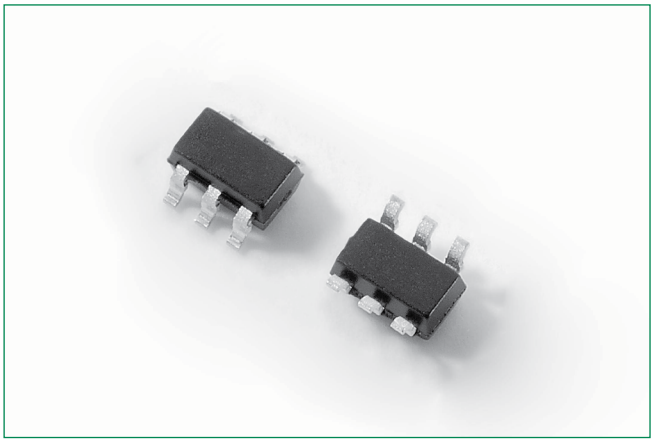
SDP Biased Series - SOT23-6

Broadband Optimized™ Protection



Description

This new SDP Biased series provides overvoltage protection for applications such as VDSL2, ADSL2, and ADSL2+ with minimal effect on data signals. This silicon design innovation results in a capacitive loading characteristic that is compatible with these high bandwidth applications. This surface mount SOT23-6 package provides a surge capability that exceeds most worldwide standards and recommendations for lightning surge withstand capability of tertiary protectors.

Features & Benefits

- Compatible with VDSL2 (30MHz) and with G.fast (106MHz)
- Balanced overvoltage protection
- Low distortion
- Low insertion loss
- Low profile
- Response time under 500ns
- RoHS Compliant
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

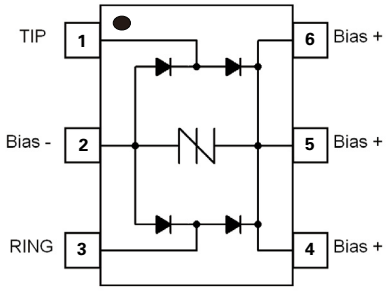
Additional Information

Resources | Accessories | Samples

Applicable Global Standards

- ANSI C62.41
- IEC 61000-4-12
- IEC 61000-4-5, 30A (tP=8/20µs) 2nd edition
- IEC 61000-4-2 level 4
  - 15kV (air discharge)
  - 8kV (contact discharge)

Pinout Designation & Schematic Symbol



Agency Approvals

Agency	Agency File Number
	E133083

Absolute Maximum Ratings between pin1 and pin 3, Ta= 25°C (Unless otherwise noted)

Part Number	Marking	Maximum Junction Temperature	Storage Temperature Range	I_{PP} 8/20µs
		°C	°C	A Max
SDP0240T023G6RP	P24	150	-65 to 150	30 [1]

Notes: 1. The device must be in thermal equilibrium at 25°C

Electrical Characteristics between pin 1 and pin 3, Ta = 25°C

Part Number	Marking	V_{DRM} @I_{DRM}=100nA	I_{DRM} @V_{DRM}=19V	V_S@1V/µs	I_H	I_S	Co@f=1MHz,2V	Delta Co@ Line Bias = 1 V to 19 V
		V min	pA typ	V max	mA typ	mA min	pF max	pF max
SDP0240T023G6RP	P24	19	300	29	40	10	3.0	0.5

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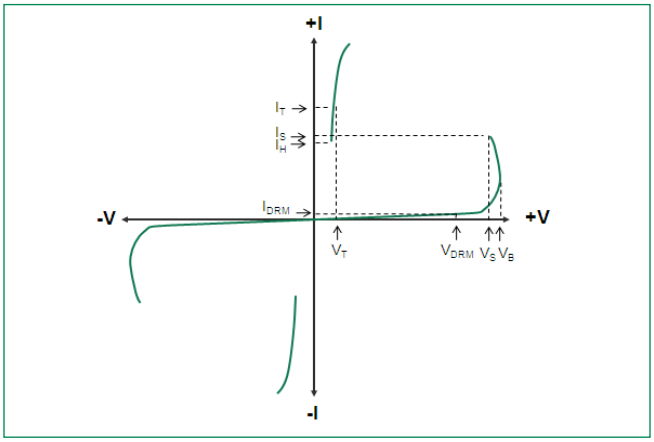
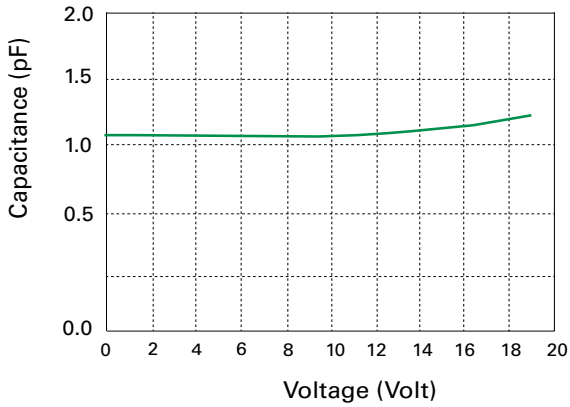
V-I: Characteristics



Typical capacitance against line voltage (without external bias)



Surge Ratings

Series	I_{PP}
	1.2/50µs [1] / 8/20µs [2]
	A min
G	30

Notes:

1. Voltage waveform in µs
2. Current waveform in µs

- Peak pulse current rating (I_{pp}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- The component must be in thermal equilibrium at 25°C.

Thermal Information

Parameter	Rating	Units
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 10s)	260	°C

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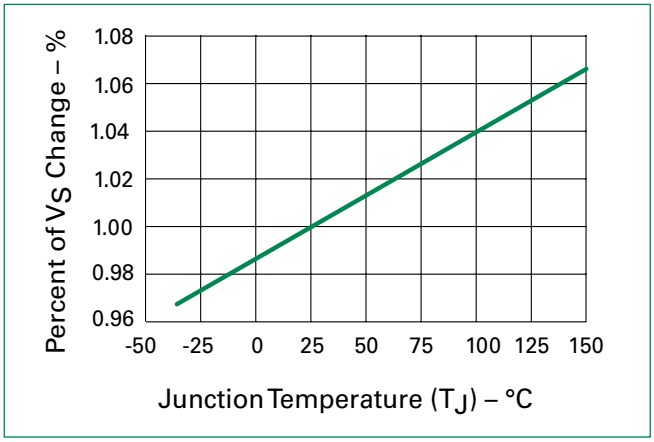
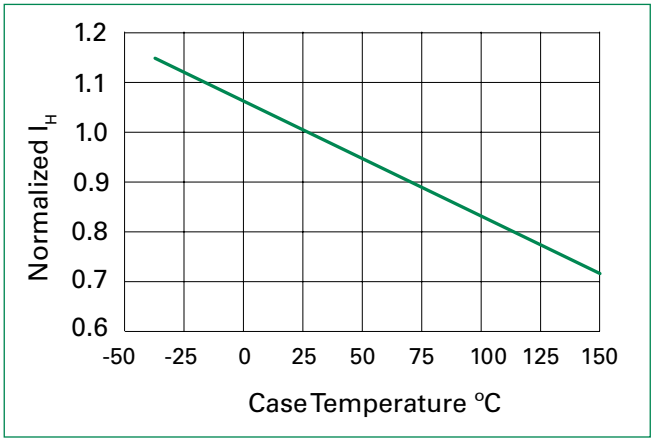
Normalized VS Change vs. Junction Temperature

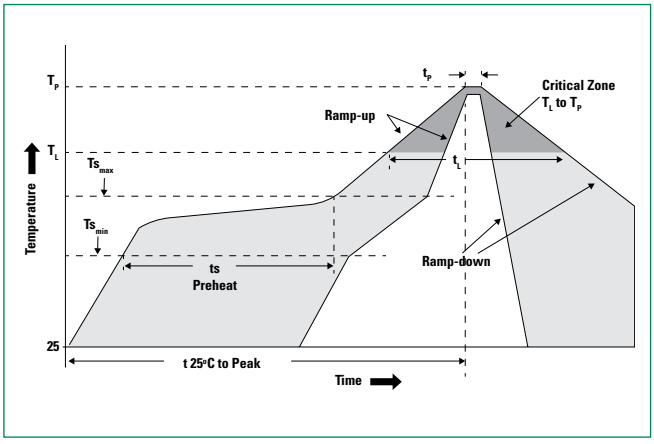


Normalized Holding Current vs. Case Temperature



Soldering Parameters

Reflow Condition		Pb-Free assembly
Pre Heat	**- Temperature Min ($T_{s(min)}$)**	150°C
	- Temperature Max ($T_{s(max)}$)	200°C
	- Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	**- Temperature (T_L) (Liquidus)**	+217°C
	- Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		250(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		20-40 secs.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		260°C



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Physical Specifications

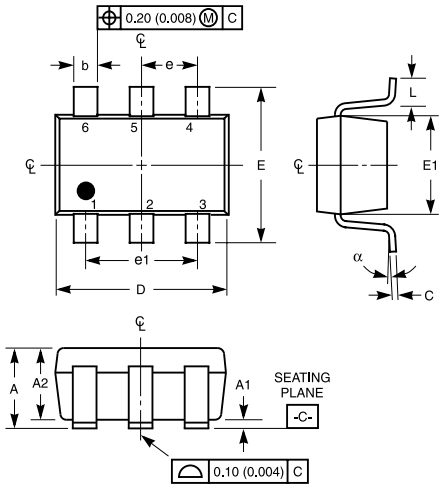
Lead Plating	SOT23: Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	V-0

Notes:
1. All dimensions are in millimeters.
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC MO-178
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte tine

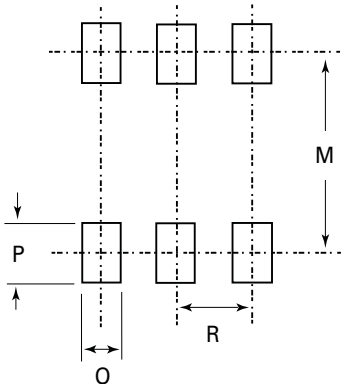
Environmental Specifications

Temp Cycling	Mil-STD-883, Method 1010.8 Condition C, -65°C to +150°C 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
Bias Humidity	JESD 22-A101 85°C , 85°CRH. 50V 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
Pressure Cooker	JEDEC 22-A102 No Bias, 121°C, 100%RH 96Hrs/192Hrs. 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
High Temp Storage	JESD 22-A103 Con B. 150°C, no bias 1000Hrs
HTRB	JESD 22-108 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
Thermal Shock	Mil-STD-883, Method 1011.9 Condition A, 0°C to 100°C 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
C-SAM	As per flow, JSTD-020 pre&post preconditioning test.
Wet Humidity (Tin only)	JESD 201 standard: 55°C/85%RH

Dimensions - SOT23-6



Recommended Solder Pad Layout



Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.041	0.057	1.050	1.450
A1	0.000	0.006	0.000	0.150
A2	0.035	0.051	0.900	1.300
b	0.012	0.020	0.300	0.500
C	0.003	0.008	0.080	0.220
D	0.110	0.118	2.800	3.000
E	0.102	0.118	2.600	3.000
E1	0.057	0.069	1.450	1.750
e	0.037 (BSC)		0.950 (BSC)	
e1	0.074(BSC)		1.900(BSC)	
L (note 4.5)	0.012	0.023	0.300	0.600
N (note 6)	6		6	
α	0°C	8°C	0°C	8°C
M	-	0.102	-	2.590
O	-	0.027	-	0.690
P	-	0.039	-	0.990
R	-	0.038	-	0.950

Notes:
1. Dimensioning and tolearances per ANSI 14.5M-1982.
2. Package conforms to JEDEC MO-178
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Foot lenth L measured at reference to seatng plane.
5. "L" is the length of flat foot surface for soldering to substrate.
6. "N" is the number of terminal positions.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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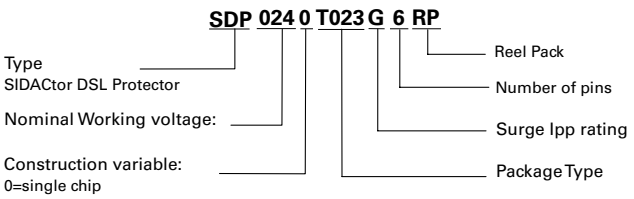
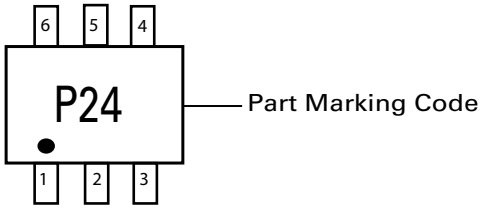
Part Numbering



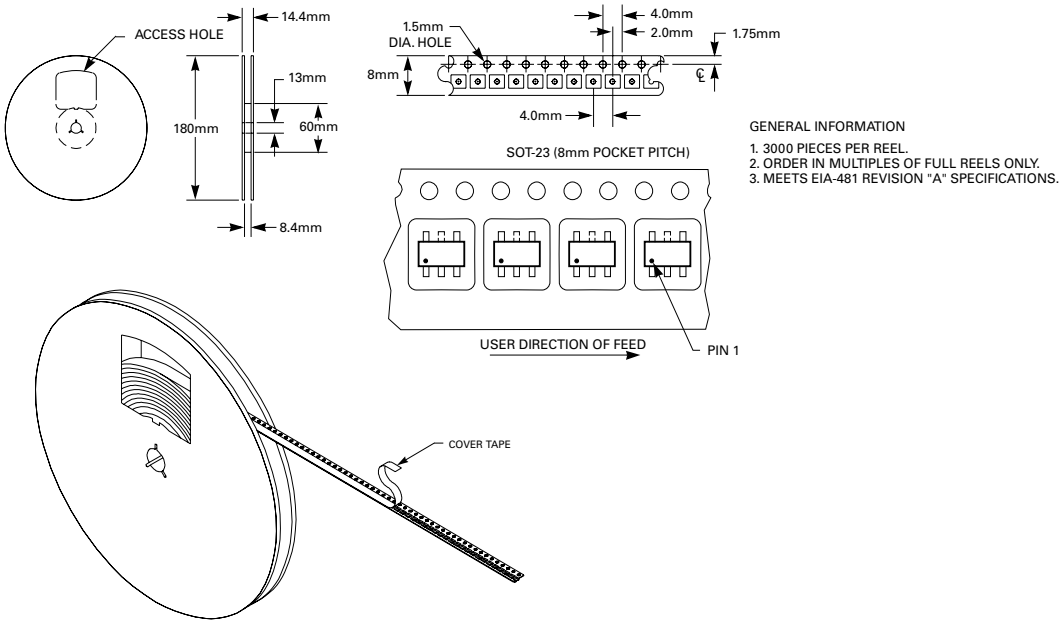
Part Marking



Packing Options

Package Type	Description	Quantity
SOT23-6	Tape and Reel	3000

Embossed Carrier Tape & Reel Specification - SOT23-6



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