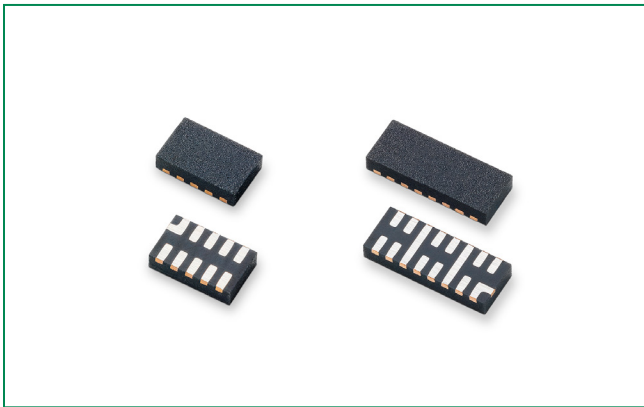


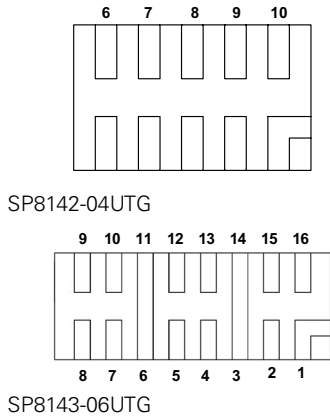
# SP814x Series 1.0pF 22KV Diode Array



**OBSOLETE** DATE: 06/10th/2020 PCN/ECN# ESU270-51  
REPLACED BY: \_\_\_\_\_



## Pinout



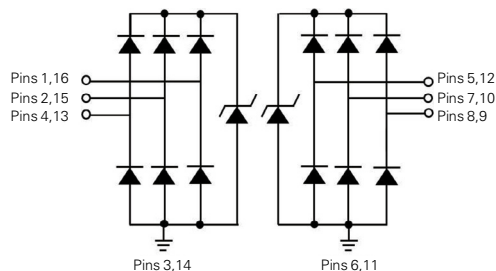
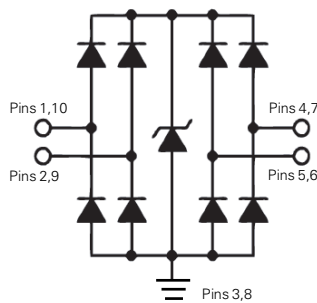
## Description

The SP814x series integrates 4 or 6 channels of ultra low capacitance rail-to-rail diodes and an additional zener diode to provide protection for electronic equipment that may experience destructive electrostatic discharges (ESD). This robust component can safely absorb repetitive ESD strikes above the maximum level specified in IEC 61000-4-2 international standard ( $\pm 8\text{kV}$  contact discharge) without performance degradation. The extremely low loading capacitance also makes it ideal for protecting high speed signal pins such as HDMI2.0, USB3.0, USB2.0, and IEEE 1394.

## Features

- ESD, IEC 61000-4-2,  $\pm 22\text{kV}$  contact,  $\pm 22\text{kV}$  air
- EFT, IEC 61000-4-4, 40A ( $t_p=5/50\text{ns}$ )
- Lightning, IEC 61000-4-5 2<sup>nd</sup> edition, 2.5A ( $t_p=8/20\mu\text{s}$ )
- Low capacitance of 1.0pF (TYP) per I/O
- Low leakage current of 25nA (TYP) at 5V
- Small form factor  $\mu\text{DFN}$  packages (JEDEC MO-229) saves board space
- AEC-Q101 qualified
- Moisture Sensitivity Level (MSL -1)
- Halogen free, lead free and RoHS compliant

## Functional Block Diagram



## Applications

- LCD/PDP TVs
- External Storage
- DVD/ Blue-Ray Players
- Desktops/Servers
- Notebooks/Tablets
- Set Top Boxes
- Mobile Phones
- Flash Memory Cards
- Digital Cameras

### Absolute Maximum Ratings

Symbol	Parameter	Value	Units
$I_{PP}$	Peak Current ( $t_p=8/20\mu s$ )	2.5	A
$T_{OP}$	Operating Temperature	-40 to 125	°C
$T_{STOR}$	Storage Temperature	-55 to 150	°C

**Note:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the component. This is a stress only rating and operation of the component at these or any other conditions above those indicated in the operational sections of this specification is not implied.

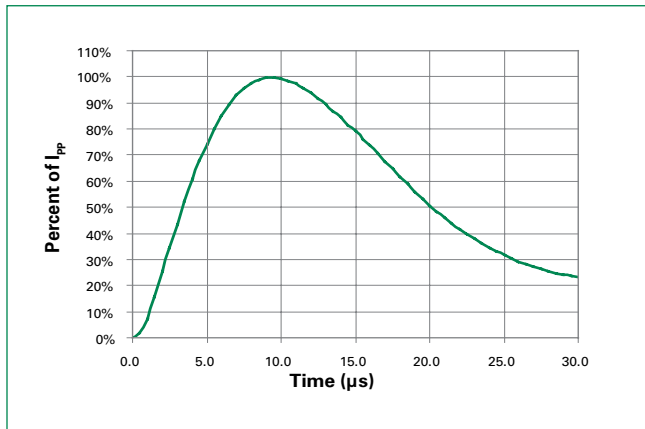
### Electrical Characteristics ( $T_{OP}=25^\circ C$ )

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	$V_{RWM}$	$I_R \leq 1\mu A$			5.0	V
Reverse Leakage Current	$I_{LEAK}$	$V_R=5V$ , Any I/O to GND		25	50	nA
Channel Resistance	$R_{CH}$	Pins 1-10, 2-9, 4-7 and 5-6, SP8142 Pins 1-16, 2-15, 4-13, 5-12, 7-10 and 8-9, SP8143		0.5		$\Omega$
Clamp Voltage <sup>1</sup>	$V_C$	$I_{PP}=1A$ , $t_p=8/20\mu s$ , Fwd		9.2		V
		$I_{PP}=2A$ , $t_p=8/20\mu s$ , Fwd		10.3		V
Dynamic Resistance <sup>2</sup>	$R_{DYN}$	TLP, $t_p=100ns$ , I/O to GND		0.3		$\Omega$
ESD Withstand Voltage <sup>1</sup>	$V_{ESD}$	IEC 61000-4-2 (Contact)	$\pm 22$			kV
		IEC 61000-4-2 (Air)	$\pm 22$			kV
Diode Capacitance <sup>1</sup>	$C_{I/O-GND}$	Reverse Bias=0V, $f=1$ MHz		1.0		pF

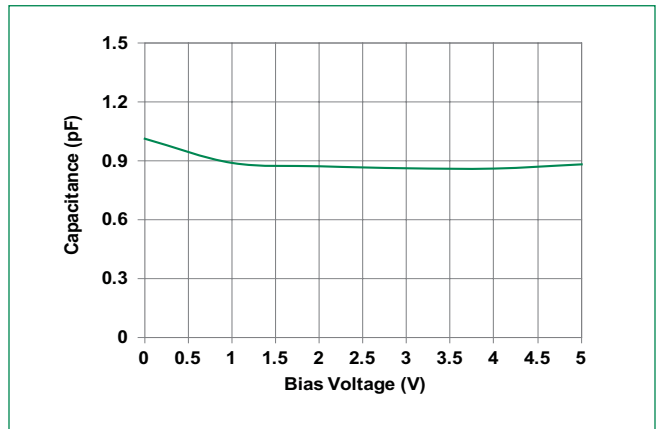
**Note:** <sup>1</sup> Parameter is guaranteed by design and/or component characterization.

<sup>2</sup> Transmission Line Pulse (TLP) with 100ns width, 2ns rise time, and average window  $t_1=70ns$  to  $t_2=90ns$

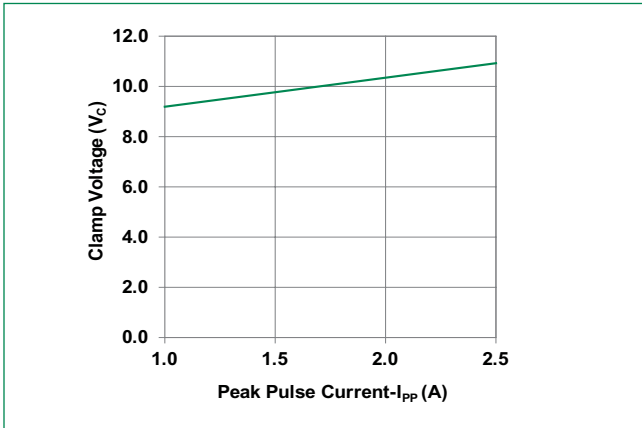
### 8/20 $\mu s$ Pulse Waveform



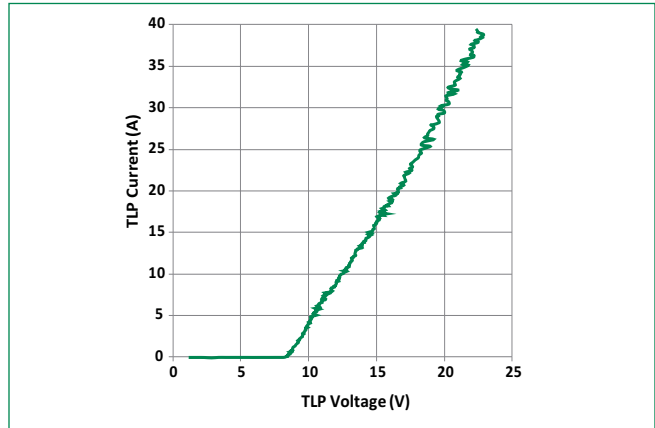
### Capacitance vs. Reverse Bias



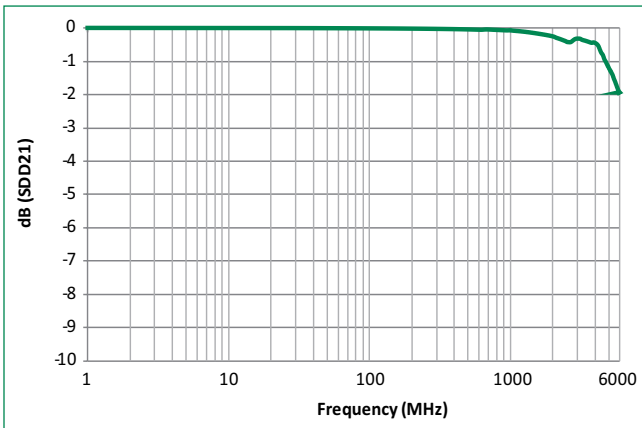
**Clamping Voltage vs  $I_{pp}$**



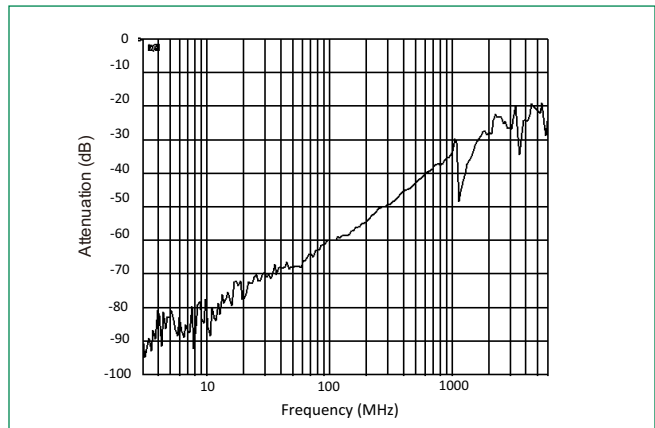
**Transmission Line Pulsing(TLP) Plot**



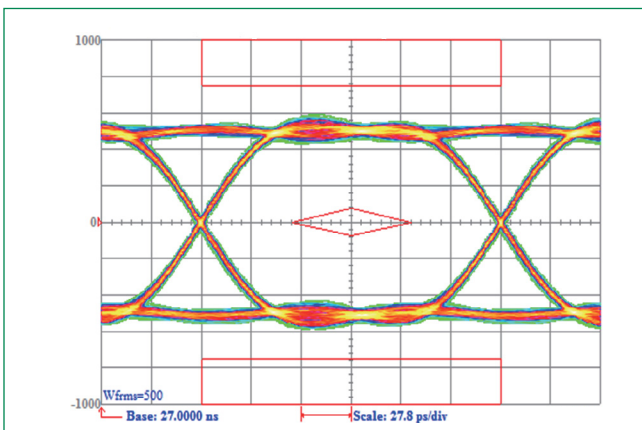
**Differential Mode Attenuation SDD21 vs. Frequency**



**Analog Crosstalk (S41)**

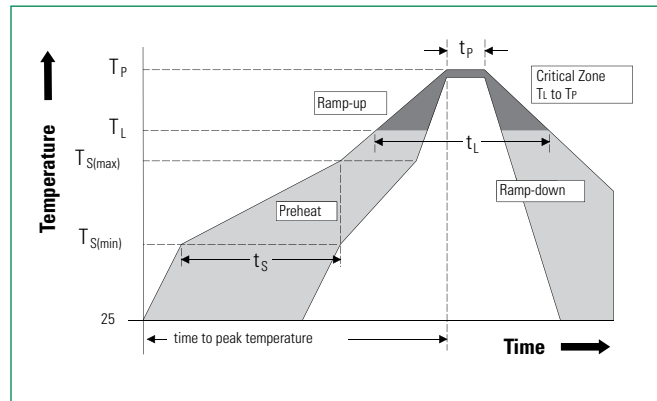


**HDMI2.0 Eye Diagram**

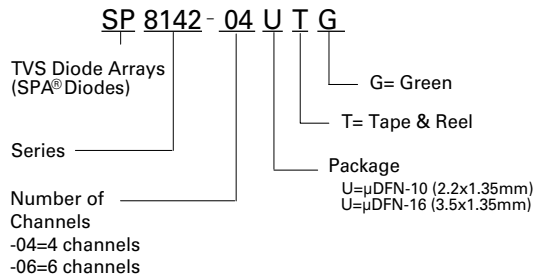


### Soldering Parameters

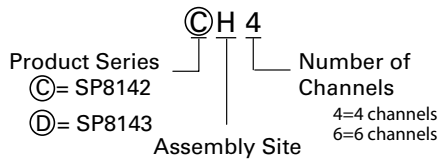
<b>Reflow Condition</b>		Pb – Free assembly
<b>Pre Heat</b>	- Temperature Min ( $T_{s(min)}$ )	150°C
	- Temperature Max ( $T_{s(max)}$ )	200°C
	- Time (min to max) ( $t_s$ )	60 – 180 secs
<b>Average ramp up rate (Liquidus) Temp (<math>T_L</math>) to peak</b>		3°C/second max
<b><math>T_{s(max)}</math> to <math>T_L</math> - Ramp-up Rate</b>		3°C/second max
<b>Reflow</b>	- Temperature ( $T_L$ ) (Liquidus)	217°C
	- Temperature ( $t_L$ )	60 – 150 seconds
<b>Peak Temperature (<math>T_p</math>)</b>		260 <sup>+0/-5</sup> °C
<b>Time within 5°C of actual peak Temperature (<math>t_p</math>)</b>		20 – 40 seconds
<b>Ramp-down Rate</b>		6°C/second max
<b>Time 25°C to peak Temperature (<math>T_p</math>)</b>		8 minutes Max.
<b>Do not exceed</b>		260°C



### Part Numbering System



### Part Marking System



### Product Characteristics

<b>Lead Plating</b>	Pre-Plated Frame
<b>Lead Material</b>	Copper Alloy
<b>Substrate material</b>	Silicon
<b>Body Material</b>	Molded Compound
<b>Flammability</b>	UL Recognized compound meeting flammability rating V-0.

**Notes :**

1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.

### Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SP8142-04UTG	μDFN-10	©H4	3000
SP8143-06UTG	μDFN-16	ⒹH6	3000

**Application Information**

**Alternatives to Semiconductor-based Common Mode Filtering**

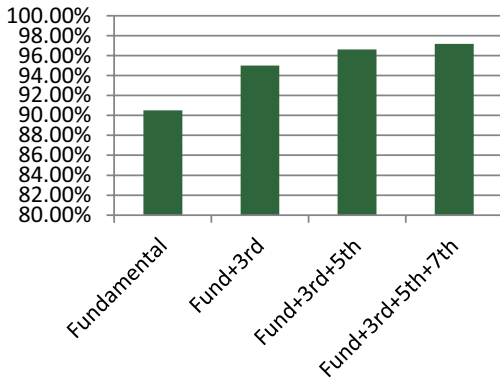
Conventional Semiconductor-based common mode filters' performance has been proven to be lacking. While excellent ESD components, the tradeoffs that designers encounter for signal integrity prove to be insurmountable.

Fundamentally, the common mode filters do not filter the unwanted signals (noise) fast enough, and create problems with resistive and inductive loading as signals pass through the components.

Odd harmonics add to signal strength, and create squarer waves, which are easier for the downstream components to detect either legal zero's or one's. Successive odd harmonics in the passband make the signal stronger. Noise generated from the fundamental frequencies does not get attenuated fast enough to meaningfully improve signal integrity, or lower the noise signature.

There are two options available (4 channel and 6 channel) and both are housed in leadless  $\mu$ DFN packages so the data lines can pass directly underneath the component to reduce discontinuities and maintain signal integrity.

Figure 1: Signal Strength of Fundamental



**Signal Compression**

Semiconductor-based components which this product are designed to replace have at least 6 ohms resistance, contributing to signal amplitude compression which negatively affect the eye height, and negatively affect Signal Integrity and compliance testing.

**Alternatives to Semiconductor-based Common Mode Filtering**

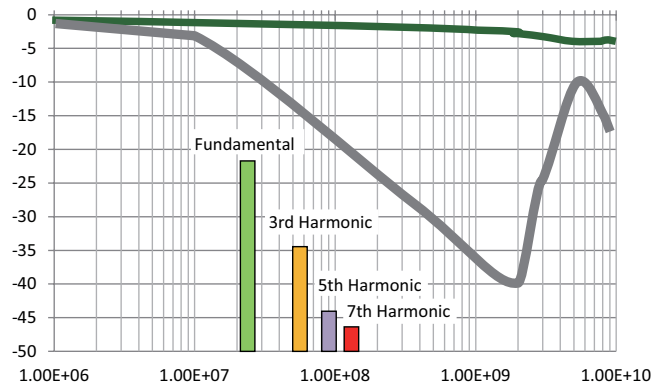
Using robust ESD protection, along with Signal Integrity best layout practices, including burying the high speed signals between two ground planes within the board permit excellent Signal Integrity, at a lower total solution cost. The SP8142/SP8143 are designed to be footprint compatible with existing solutions offering filtering, and can be used in the test scheme of testing without filtering ( using SP8142/8143) and with filtering (other solutions) and comparing the results.

If the PCB layout is good, the engineer should expect to see higher levels of Signal Integrity and equal levels of radiated and conducted noise, at a lower pricepoint using the ESD only solutions.

Figure 2: Typical multilayer PCB stack up, best to route data between ground planes to eliminate radiated noise and improve Signal Integrity.

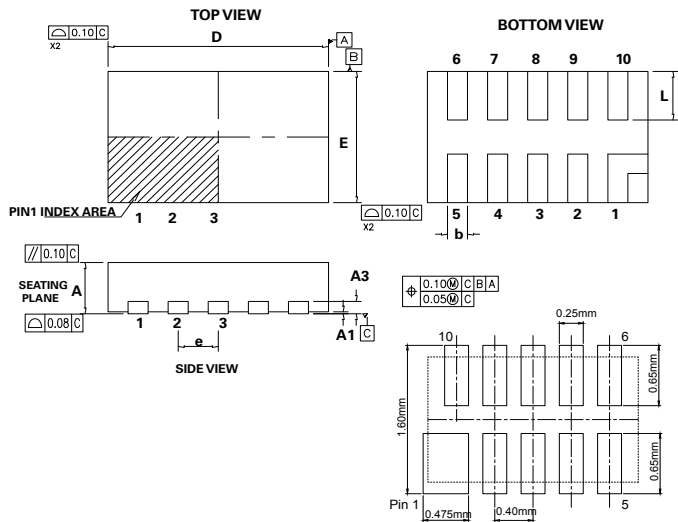


Figure 3: Suppressing the odd harmonics off of the most popular interfaces Representation of Semiconductor-based Filter (Differential Mode and Common Mode)



Interface	Fundamental	3rd Harmonic	3rd Harmonic Strength (% orig.)	5th Harmonic	5th Harmonic Strength (% orig.)
MIPI External	208 MHz	724 MHz	4.5%	1040 MHz	1.6%
HDMI 1.4a	248 MHz	744 MHz	4.5%	1240 MHz	1.6%
HDMI 2.0	600 MHz	1800 MHz	4.5%	3000 MHz	1.6%

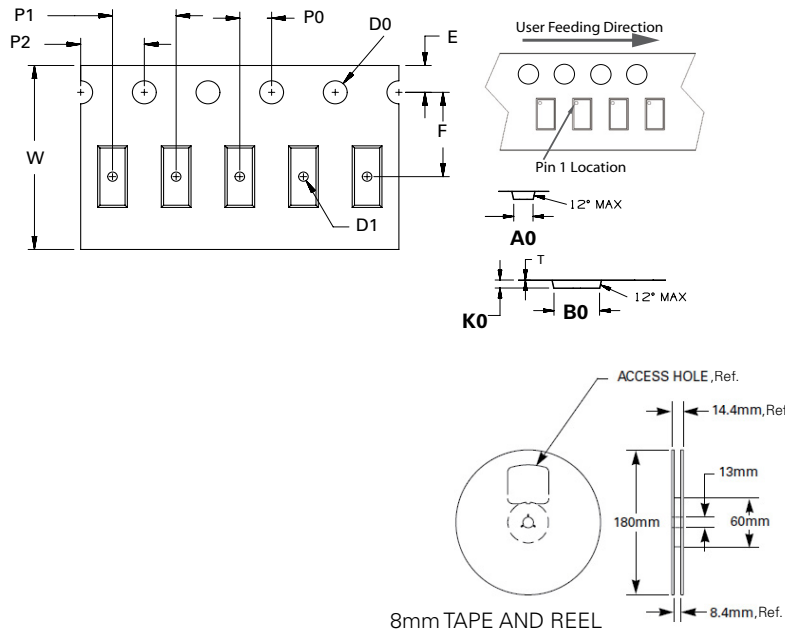
**Package Dimensions —  $\mu$ DFN-10**



Recommended Soldering Footprint

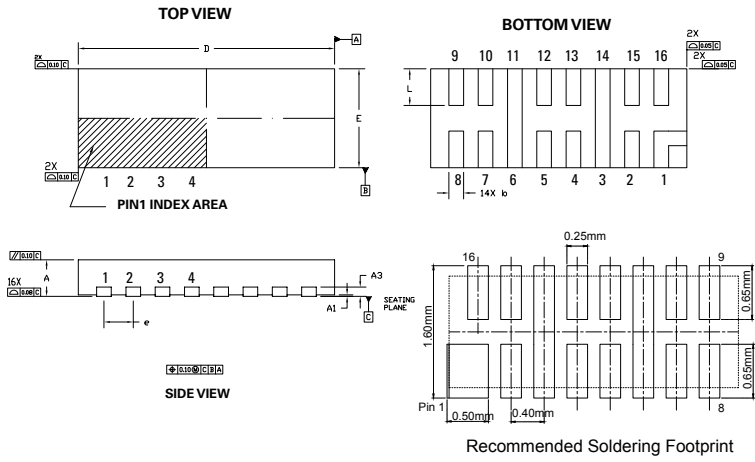
$\mu$ DFN-10 (2.2x1.35)						
JEDEC MO-229						
Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
<b>A</b>	0.45	0.52	0.55	0.018	0.020	0.022
<b>A1</b>	0.00	0.02	0.05	0.000	0.001	0.002
<b>A3</b>	0.127 Ref			0.005 Ref		
<b>b</b>	0.15	0.20	0.25	0.006	0.008	0.010
<b>D</b>	2.10	2.20	2.30	0.083	0.087	0.091
<b>E</b>	1.25	1.35	1.45	0.049	0.053	0.057
<b>e</b>	0.40 BSC			0.016 BSC		
<b>L</b>	0.40	0.50	0.60	0.016	0.020	0.024

**Embossed Carrier Tape & Reel Specification —  $\mu$ DFN-10**



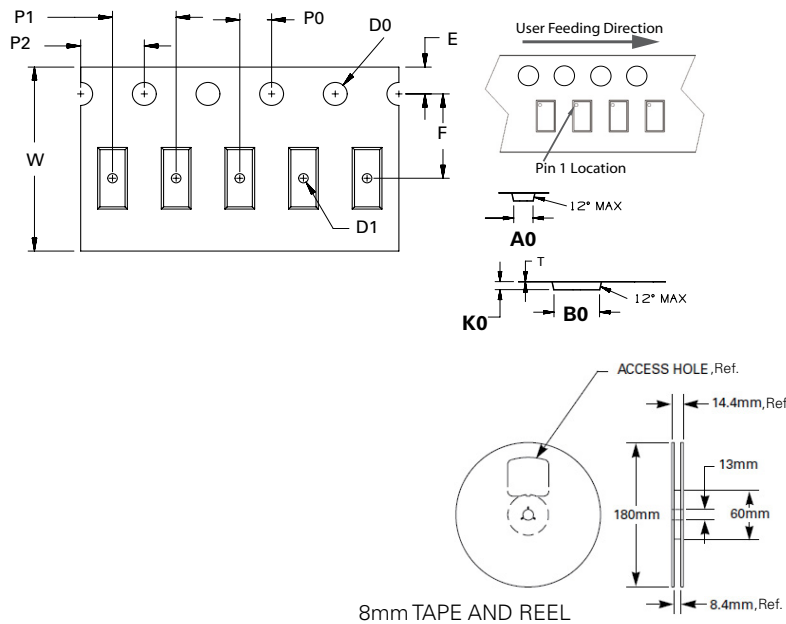
Symbol	Millimeters
<b>A0</b>	1.59 +/- 0.05
<b>B0</b>	2.45 +/- 0.05
<b>D0</b>	Ø1.50 + 0.10
<b>D1</b>	Ø 0.50 + 0.05
<b>E</b>	1.75 +/- 0.10
<b>F</b>	3.50 +/- 0.05
<b>K0</b>	0.69 +/- 0.05
<b>P0</b>	2.00 +/- 0.05
<b>P1</b>	4.00 +/- 0.10
<b>P2</b>	4.00 +/- 0.10
<b>T</b>	0.25 +/- 0.02
<b>W</b>	8.00 + 0.30 /- 0.10

**Package Dimensions —  $\mu$ DFN-16**



$\mu$ DFN-16 (3.5x1.35mm)						
JEDEC MO-229						
Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
<b>A</b>	0.45	0.52	0.55	0.018	0.020	0.022
<b>A1</b>	0.00	0.02	0.05	0.000	0.001	0.002
<b>A3</b>	0.127 Ref			0.005 Ref		
<b>b</b>	0.15	0.20	0.25	0.006	0.008	0.010
<b>D</b>	3.40	3.50	3.60	0.134	0.138	0.142
<b>E</b>	1.25	1.35	1.45	0.049	0.053	0.057
<b>e</b>	0.40 BSC			0.016 BSC		
<b>L</b>	0.40	0.50	0.60	0.016	0.020	0.024

**Embossed Carrier Tape & Reel Specification —  $\mu$ DFN-16**



Symbol	Millimeters
<b>A0</b>	1.58 +/- 0.10
<b>B0</b>	3.73 +/- 0.10
<b>D0</b>	$\varnothing 1.50 + 0.10$
<b>D1</b>	$\varnothing 0.60 + 0.05$
<b>E</b>	1.75 +/- 0.10
<b>F</b>	5.50 +/- 0.05
<b>K0</b>	0.68 +/- 0.10
<b>P0</b>	2.00 +/- 0.05
<b>P1</b>	4.00 +/- 0.10
<b>P2</b>	4.00 +/- 0.10
<b>T</b>	0.28 +/- 0.02
<b>W</b>	12.00 + 0.30 /- 0.10