IXYS

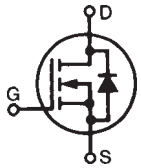
HiPerFET™ Power MOSFETs

N-Channel Enhancement Mode
High dv/dt, Low t_{rr}, HDMOS™ Family

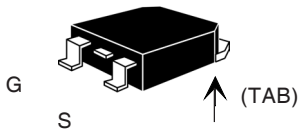
Preliminary data sheet

	V_{DSS}	I_{D25}	$R_{DS(on)}$
IXFT 10 N100	**1000 V**	**10 A**	**1.20 Ω**
IXFT12 N100	**1000 V**	**12 A**	**1.05 Ω**

$t_{rr} \leq 250$ ns



TO-268 Case Style



G = Gate, TAB = Drain
S = Source,

Symbol	Test Conditions		Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C		1000	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ		1000	V
V_{GS}	Continuous		±20	V
V_{GSM}	Transient		±30	V
I_{D25}	T_C = 25°C	10N100	10	A
		12N100	12	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}	10N100	40	A
		12N100	48	A
I_{AR}	T_C = 25°C	10N100	10	A
		12N100	12	A
E_{AR}	T_C = 25°C	30	mJ	
dv/dt	$I_S \leq I_{DM}$, di/dt ≤ 100 A/μs, $V_{DD} \leq V_{DSS}$, $T_J \leq 150°C$, R_G = 2 Ω		5	V/ns
P_D	T_C = 25°C		300	W
T_J			-55 ... +150	°C
T_{JM}			150	°C
T_{stg}			-55 ... +150	°C
T_L	1.6 mm (0.062 in.) from case for 10 s		300	°C
M_d	Mounting torque		1.13/10	Nm/lb.in.
Weight			TO-268 = 6 g	

Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
V_{DSS}	V_{GS} = 0 V, I_D = 3 mA		1000			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 4 mA		2.0		4.5	V
I_{GSS}	V_{GS} = ±20 V_{DC}, V_{DS} = 0				±100	nA
I_{DSS}	$V_{DS} = 0.8 \cdot V_{DSS}$	T_J = 25°C			250	μA
	V_{GS} = 0 V	T_J = 125°C			1	mA
$R_{DS(on)}$	V_{GS} = 10 V, $I_D = 0.5 \cdot I_{D25}$	10N100			1.20	Ω
		12N100			1.05	Ω
	Pulse test, t ≤ 300 μs, duty cycle d ≤ 2 %					

Features

- International standard package
- Low $R_{DS\ (on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
  - easy to drive and to protect
- Fast intrinsic Rectifier

Applications

- DC-DC converters
- Synchronous rectification
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- AC motor control
- Temperature and lighting controls
- Low voltage relays

Advantages

- Surface mountable, high power package
- Space savings
- High power density

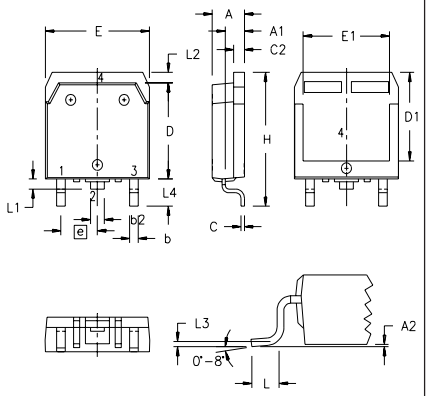
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Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
g_{fs}	V_{DS} = 10 V; I_D = 0.5 • I_{D25}, pulse test	6	10		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		4000		pF
C_{oss}			310		pF
C_{rss}			70		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25} R_G = 2 Ω (External),		21	50	ns
t_r			33	50	ns
$t_{d(off)}$			62	100	ns
t_f			32	50	ns
$Q_{g(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25}		122	155	nC
Q_{gs}			30	45	nC
Q_{gd}			50	80	nC
R_{thJC}				0.42	K/W

Source-Drain Diode

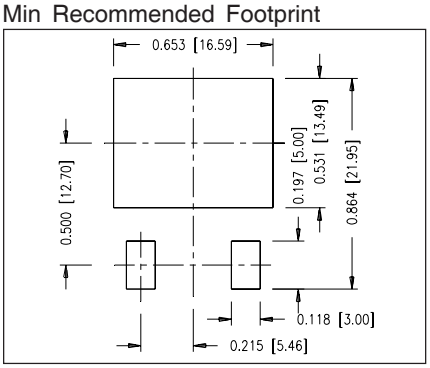
Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
I_S	V_{GS} = 0 V	10N100			10	A
		12N100			12	A
I_{SM}	Repetitive; pulse width limited by T_{JM}	10N100			40	A
		12N100			48	A
V_{SD}	$I_F = I_S$, V_{GS} = 0 V, Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %				1.5	V
t_{rr}	$I_F = I_S$ -di/dt = 100 A/µs, V_R = 100 V	T_J = 25°C			250	ns
		T_J = 125°C			400	ns
Q_{RM}		T_J = 25°C		1		µC
		T_J = 125°C		2		µC
I_{RM}		T_J = 25°C		10		A
		T_J = 125°C		15		A

TO-268 Outline



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.193	.201	4.90	5.10
A1	.106	.114	2.70	2.90
A2	.001	.010	0.02	0.25
b	.045	.057	1.15	1.45
b2	.075	.083	1.90	2.10
C	.016	.026	0.40	0.65
C2	.057	.063	1.45	1.60
D	.543	.551	13.80	14.00
D1	.488	.500	12.40	12.70
E	.624	.632	15.85	16.05
E1	.524	.535	13.30	13.60
e	.215 BSC		5.45 BSC	
H	.736	.752	18.70	19.10
L	.094	.106	2.40	2.70
L1	.047	.055	1.20	1.40
L2	.039	.045	1.00	1.15
L3	.010 BSC		0.25 BSC	
L4	.150	.161	3.80	4.10

Min Recommended Footprint



IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,881,106 5,017,508 5,049,961 5,187,117 5,486,715 6,306,728B1 6,259,123B1 6,306,728B1 4,850,072 4,931,844 5,034,796 5,063,307 5,237,481 5,381,025 6,404,065B1 6,162,665 6,534,343 6,583,505

Fig. 1. Output Characteristics

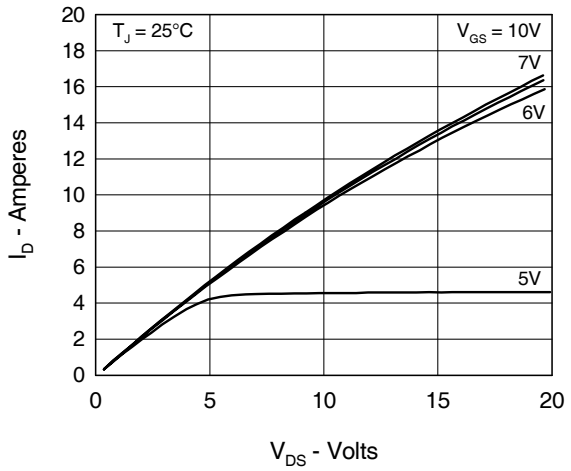


Fig. 2. Input Admittance

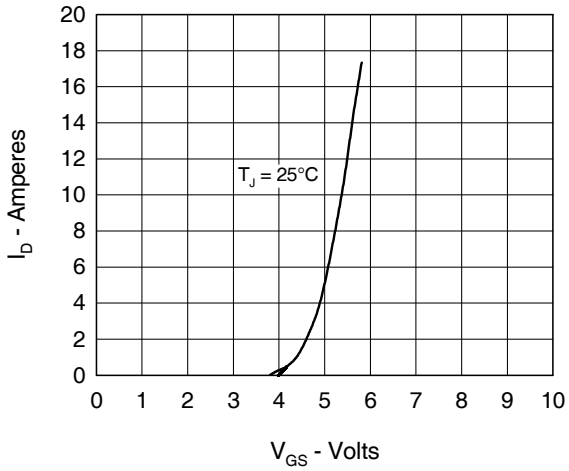


Fig. 3. $R_{DS(on)}$ vs. Drain Current

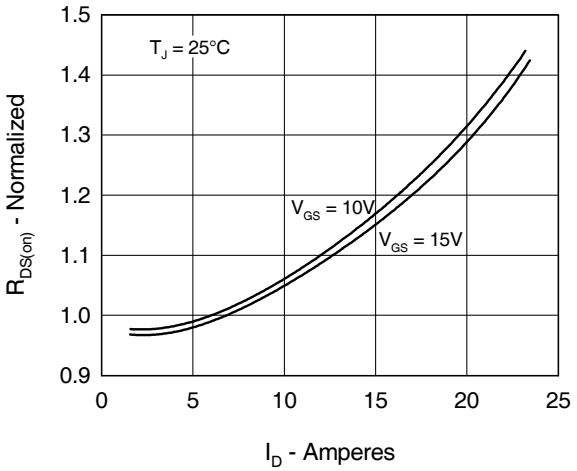


Fig. 4. Temperature Dependence of Drain to Source Resistance

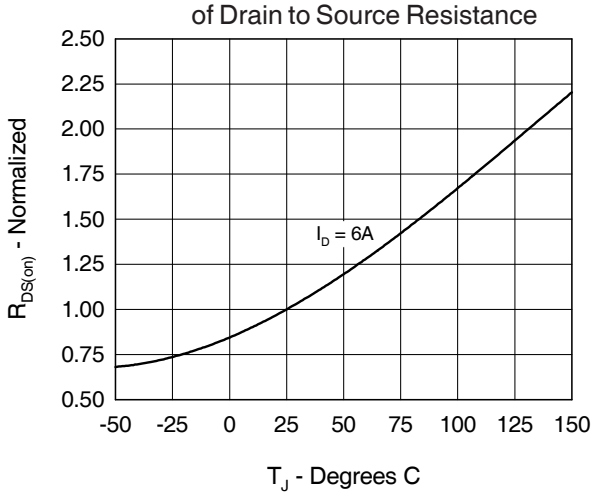


Fig. 5. Drain vs. Case Temperature

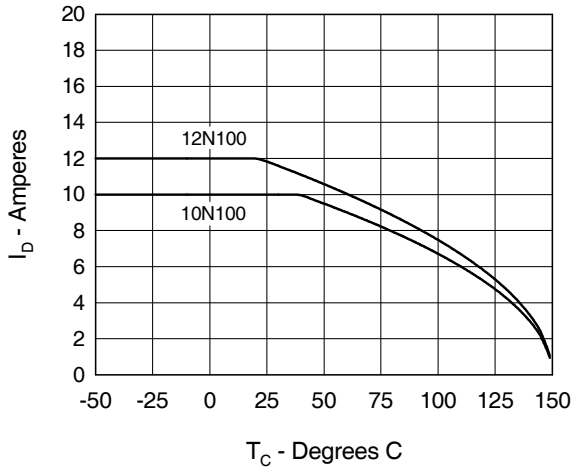
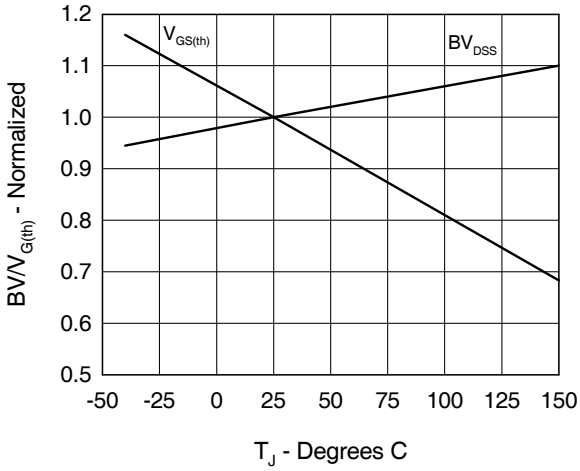


Fig. 6. Temperature Dependence of Breakdown and Threshold Voltage



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Fig. 7. Gate Charge Characteristic Curve

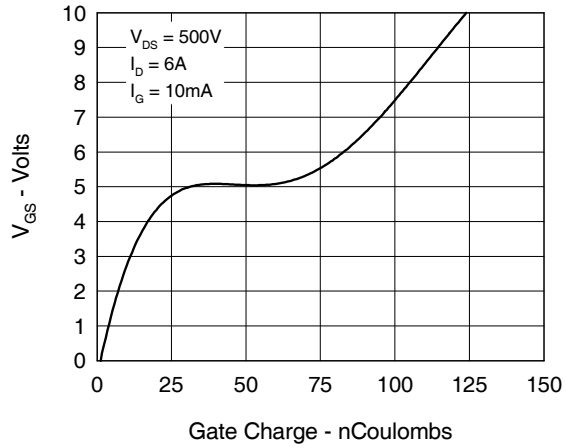


Fig. 8. Capacitance Curves

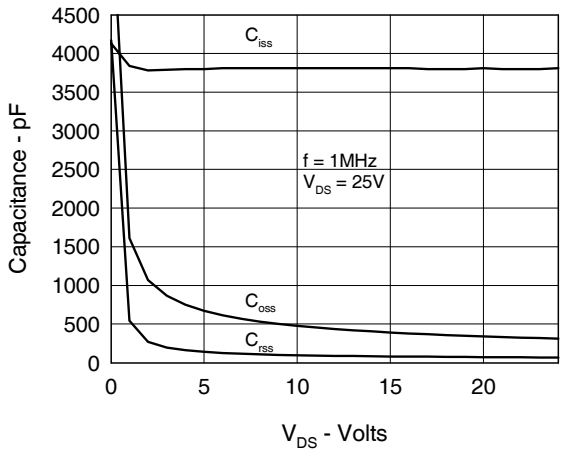


Fig. 9. Source Current vs. Source to Drain Voltage

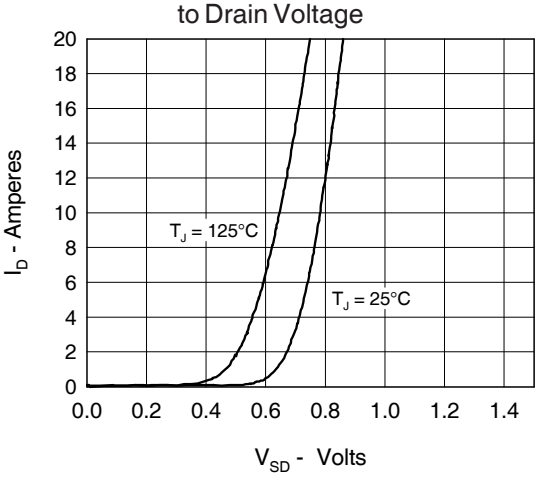
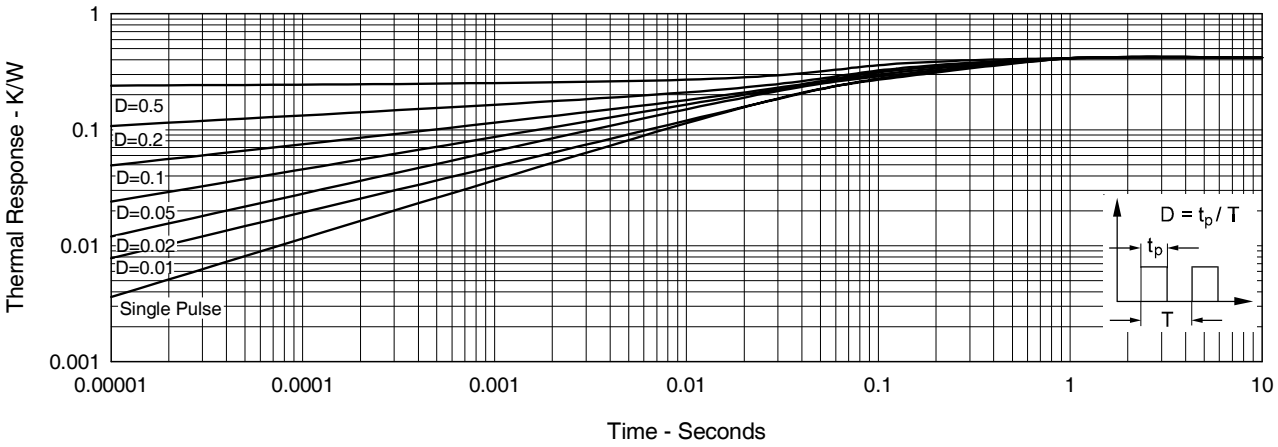


Fig.10. Transient Thermal Impedance



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