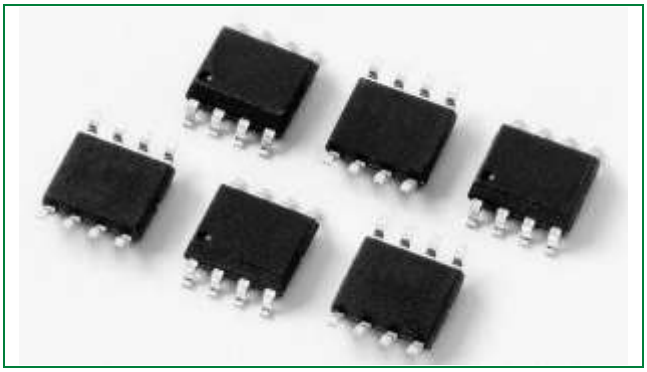
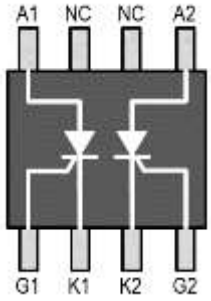
STP802U2SRP
1.5 A Sensitive Dual SCRs



Agency Approvals and Environmental

Environmental Approvals
RoHS HF

Circuit Diagram



STP Type

Product Summary

Characteristic	Value	Unit
$I_{T(RMS)}$	1.5	A
V_{DRM} / V_{RRM}[1]	800	V
I_{GT}	100	µA

Note 1: V_{DRM}, V_{RRM}, V_{DSM}, V_{RSM} are defined for A1-K1 with G1 open, and A2-K2 with G2 open.

Product Description

This 1.5 A Dual SCR part offers a high static dv/dt with a low turn off (t_q) time. It is specifically designed for Ground Fault Circuit Interrupter (GFCI) and Arc Fault Circuit Interrupter (AFCI), Residual Current Device (RCD) and Residual Current Circuit Breaker with Overload Protection (RCBO) applications.

Features

- Glass-passivated junctions
- Surge capability up to 20 A
- Non-repetitive forward direction peak off-state voltage, V_{DSM}, up to 1150 V
- Non-repetitive reverse blocking voltage, V_{RSM}, up to 900 V
- High dv/dt noise immunity
- Sensitive gate for direct microprocessor interface
- Halogen-free and RoHS compliant

Applications

- GFCI
- AFCI
- Circuit breaker

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1. Maximum Ratings

Symbol	Characteristic	Conditions	Value	Unit
$I_{T(RMS)}$	RMS On-state Current (Full Sine Wave)	Single SCR, T_C = 53°C	1.5	A
		Dual SCR, T_C = 53°C	0.6	
I_{TSM}	Non-repetitive Surge Peak On-state Current (Full Cycle, T_J Initial = 25 °C)	f = 50 Hz, t = 20 ms	20	A
		f = 60 Hz, t = 16.7 ms	24	
I^2t	I^2t Value for Fusing	t_p = 8.3 ms	2	A^2s
di/dt	Critical Rate of Rise of On-state Current	f = 60 Hz, T_J =125°C	80	A/µs
I_{GTM}	Peak Gate Trigger Current	t_p = 20 µs, T_J =125°C	0.5	A
$P_{G(AV)}$	Average Gate Power Dissipation	T_J =125°C	0.2	W
T_{STG}	Storage Temperature	-	-40 to 150	°C
T_J	Operating Junction Temperature	-	-40 to 125	°C
V_{DSM}	Non-repetitive Peak Off-state Voltage	T_J = 25°C, R_{GK} = 1 KΩ, K1 to A1 and K2 to A2	1150	V
V_{RSM}	Non-repetitive Reverse Blocking Voltage	T_J = 25°C, R_{GK} = 1 KΩ, K1 to A1 and K2 to A2	900	V
V_{ISO}	Isolation Voltage	SCR1 to SCR2	800	V

2. Thermal Characteristics

Symbol	Characteristic	Value	Unit
$R_{th(JC)}$	Thermal Resistance, junction-to-case, I_T = 1A, Single SCR	45	°C/W
$R_{th(JA)}$	Thermal Resistance, junction-to-ambient, I_T = 1A, Single SCR	120	°C/W

3. Electrical Characteristics (T_J = 25 °C unless otherwise specified)

Symbol	Description	Conditions		Value			Unit
				Min	Typ	Max	
I_{GT}	DC Gate Trigger Current	V_D = 6 V, R_L = 100 Ω		20	-	100	µA
V_{GT}	DC Gate Trigger Voltage	V_D = 6 V, R_L = 100 Ω		-	-	0.8	V
V_{GRM}	Peak Reverse Gate Voltage	I_{RG} = 10 µA		8	-	-	V
I_H	Holding Current	R_{GK} = 1 kΩ, I_T = 20 mA		-	-	3	mA
dv/dt	Critical Rate-of-rise of Off-stage Voltage	V_D = 2/3 V_{DRM}, T_J = 125 °C	RGK = 1 kΩ	40	-	-	V/µs
			RGK = 220 Ω	250	-	-	
V_{GD}	Gate Non-trigger Voltage	V_D = V_{DRM}, R_L = 3.3 kΩ, T_J = 125 °C		0.2	-	-	V
t_q	Turn-off Time	I_T = 0.5 A		-	-	35	µs
t_{gt}	Turn-on Time	I_G = 2 x IGT, P_W = 15 µs, I_T = 1.6 $A_{(PK)}$		-	3	-	µs

4. Static Characteristics (T_J = 25 °C unless otherwise specified)

Symbol	Description	Conditions	Maximum Value	Unit
V_{TM}	Peak On-state Voltage	I_{TM} = 4 A, t_P = 380 µs	1.8	V
VT0	Threshold Voltage	-	1.1	V
RD	Dynamic Resistance	-	133	mΩ
I_{DRM}/I_{RRM}	Off-state Current, Peak Repetitive	T_J = 25 °C	3	µA
		T_J = 125 °C	500	µA

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5. Performance Curves

Figure 1. Normalized DC Gate Trigger Current vs. Junction Temperature

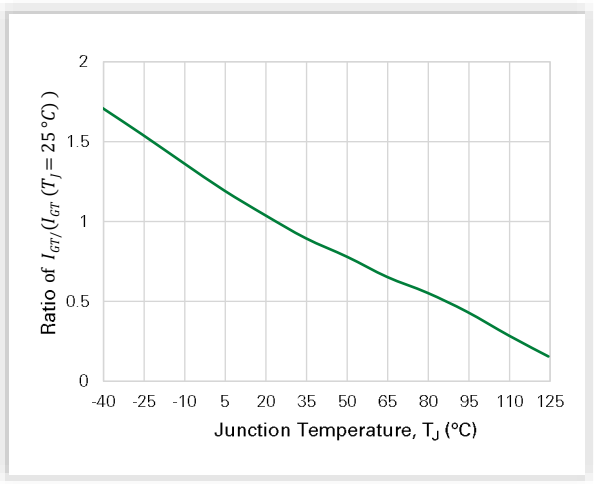


Figure 2. Normalized DC Holding Current vs. Junction Temperature

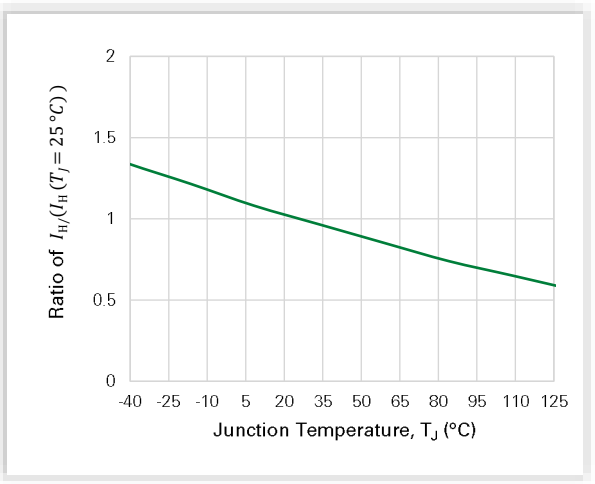


Figure 3. Normalized DC Gate Trigger Voltage vs. Junction Temperature

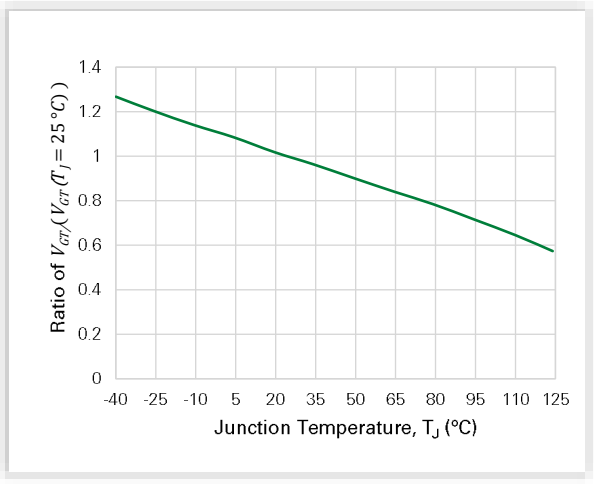


Figure 4. On-state Current vs. Typical On-state Voltage

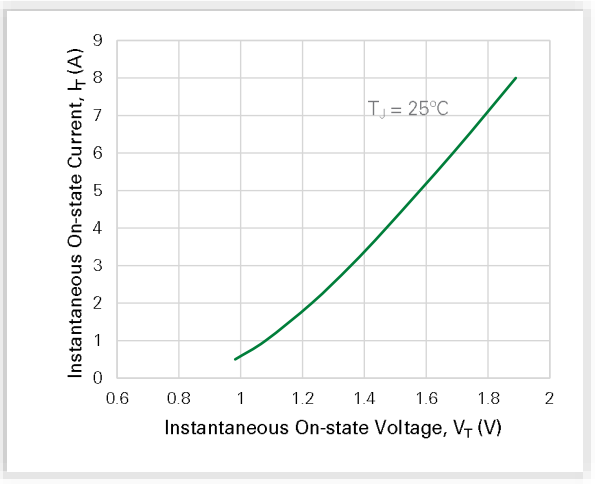


Figure 5. Typical Power Dissipation vs. RMS On-state Current

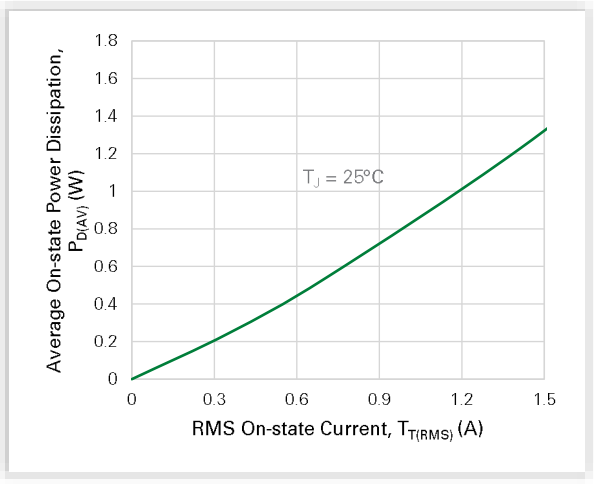
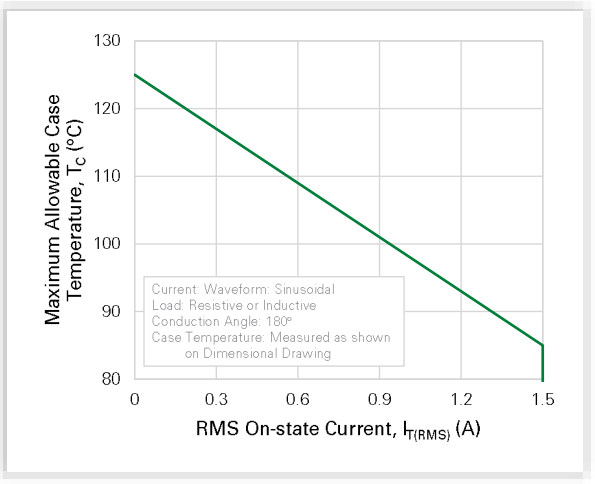
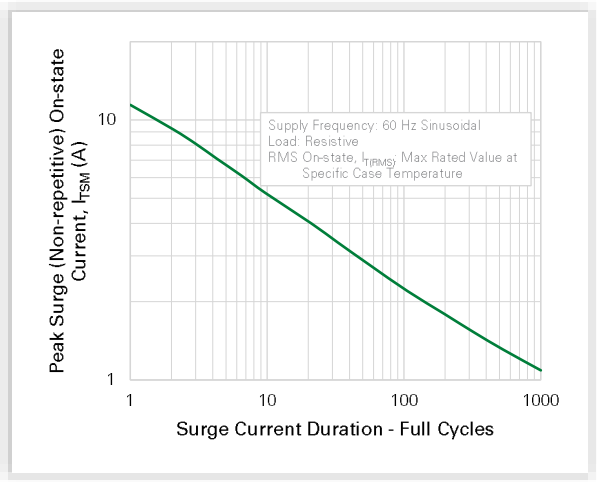


Figure 6. Maximum Allowable Case Temperature vs. On-state Current



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Figure 7. Surge Peak On-state Current vs. Number of Cycles



Notes:

1. Gate control may be lost during and immediately following surge current interval.

2. Overload may not be repeated until junction temperature has returned to steady-state rated value.

Figure 8. Typical Static dv/dt vs. R_{GK} vs. Junction Temperature

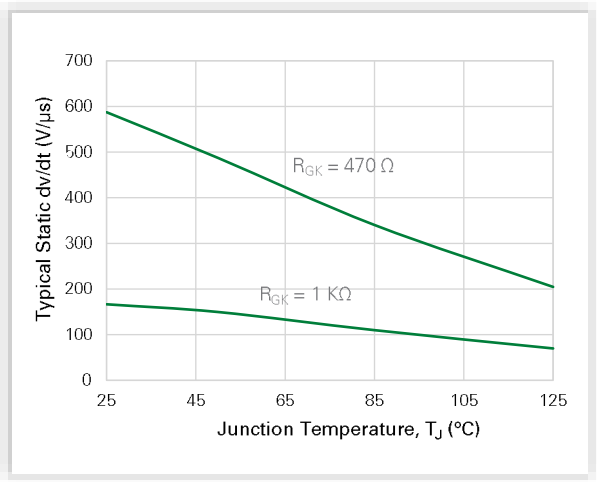


Figure 9. Typical Static dv/dt vs. C_{GK}

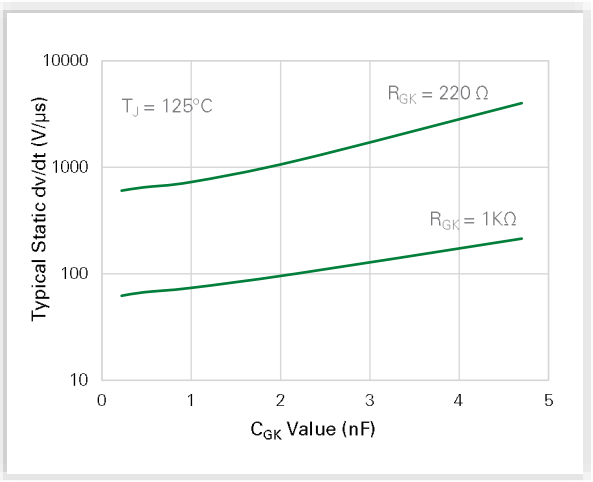


Figure 10. Typical Turn-off Time vs. R_{GK}

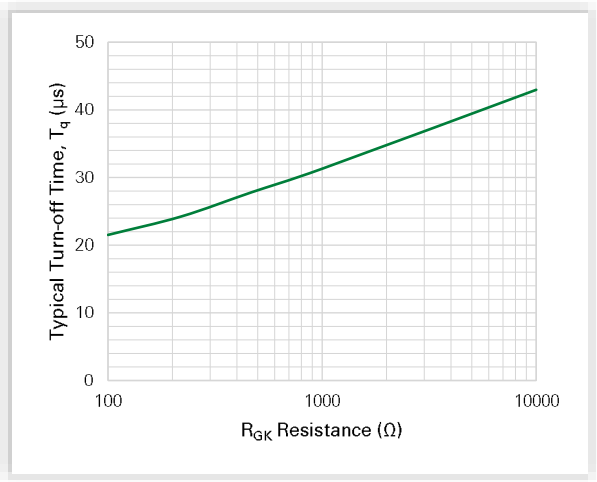
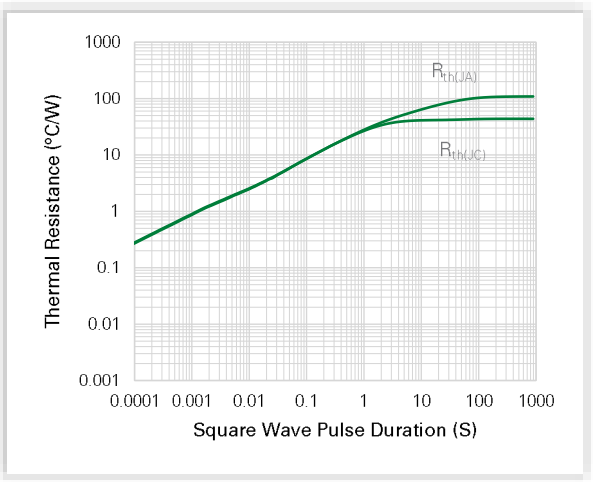
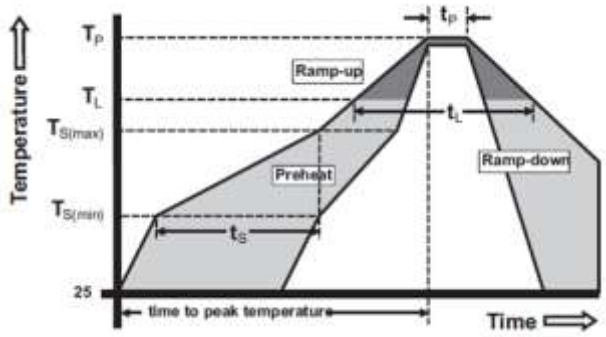


Figure 11. Thermal Resistance (°C/W) vs. Square Wave Pulse Duration (S)



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6. Soldering Parameters



Parameter		Value
Reflow Condition		Pc-free Assembly
Pre-Heat	Temperature Min, $T_{S(Min)}$	150 °C
	Temperature Max, $T_{S(Max)}$	200 °C
	Time (Min to Max), t_s	60 to 120 s
Average Ramp-up Rate Liquidus Temp., T_L to peak		3 °C/s (Max)
$T_{S(Max)}$ to T_L Ramp-up Rate		3 °C/s (Max)
Reflow	Temperature, T_L Liquidus	217 °C
	Time, t_L	60 to 150 s
Peak Temperature, T_P		260 °C (±5 °C)
Time within 5 °C of Actual Peak Temperature, t_P		30 seconds (Max)
Ramp-down Rate		6 °C/s (Max)
Time 25 °C to Peak Temperature, T_P		8 minutes (Max)
Do Not Exceed		260 °C

7. Physical Specifications

Device Feature	Detail
Terminal Finish	100% Matte Tin-plated with 150°C 1 hr annealing
Body Material	UL Recognized Compound Meeting Flammability Rating V-0
Terminal Material	Copper Alloy

8. Environmental Specifications

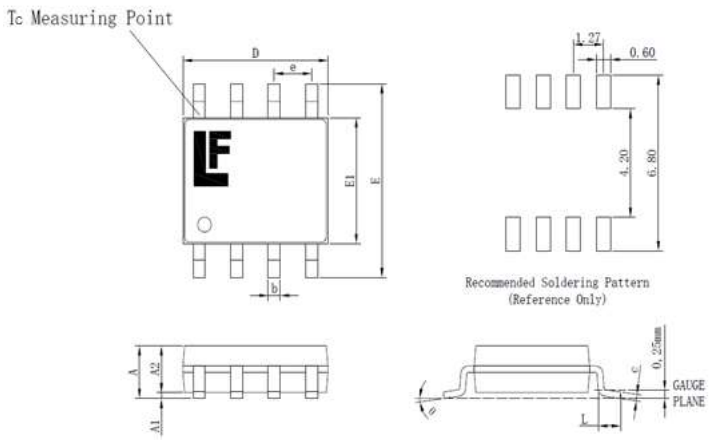
Test	Specifications and Conditions
AC Blocking	MIL-STD-750, M-1040, Cond A Applied Peak AC voltage @ 125°C for 1008 hours
Temperature Cycling	MIL-STD-750, M-1051, 1000 cycles; -40°C to +150°C; 15 min dwell time
Temperature/Humidity	EIA / JEDEC, JESD22-A101 1008 hours; 320V - DC: 85°C; 85% rel humidity
High-temp Storage	MIL-STD-750, M-1031, 1008 hours; 150°C
Low-temp Storage	1008 hours; -40°C
Resistance to Solder Heat	MIL-STD-750 Method 2031
Solderability	ANSI/J-STD-002, category 3, Test A
Lead Bend	MIL-STD-750, M-2036 Cond E
Moisture Sensitivity Level	Level 1, JEDEC-J-STD-020D

9. Design Considerations

Careful selection of the correct component for the application's operating parameters and environment will go a long way toward extending the operating life of the Thyristor. Good design practice should limit the maximum continuous current through the main terminals to 75% of the component rating. Other ways to ensure long life for a power discrete semiconductor are proper heat sinking and selection of voltage ratings for worst case conditions. Overheating, overvoltage (including dv/dt), and surge currents are the main killers of semiconductors. Correct mounting, soldering, and forming of the leads also help protect against component damage.

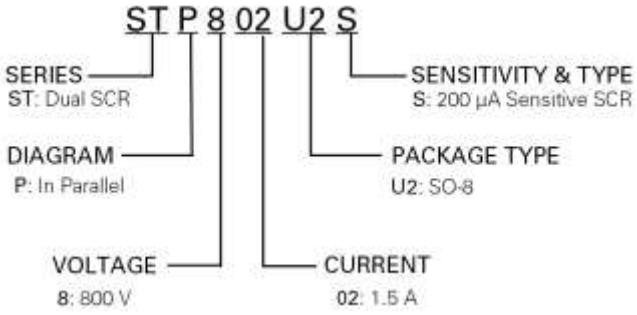
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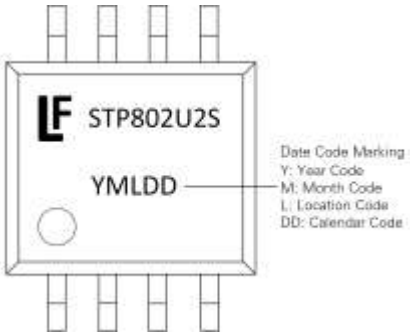
10. Package Dimensions



Package	SOIC			
Pins	8			
JEDEC	MS-012			
	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.65	0.050	0.065
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
L	0.40	1.27	0.016	0.050

11. Part Numbering and Marking





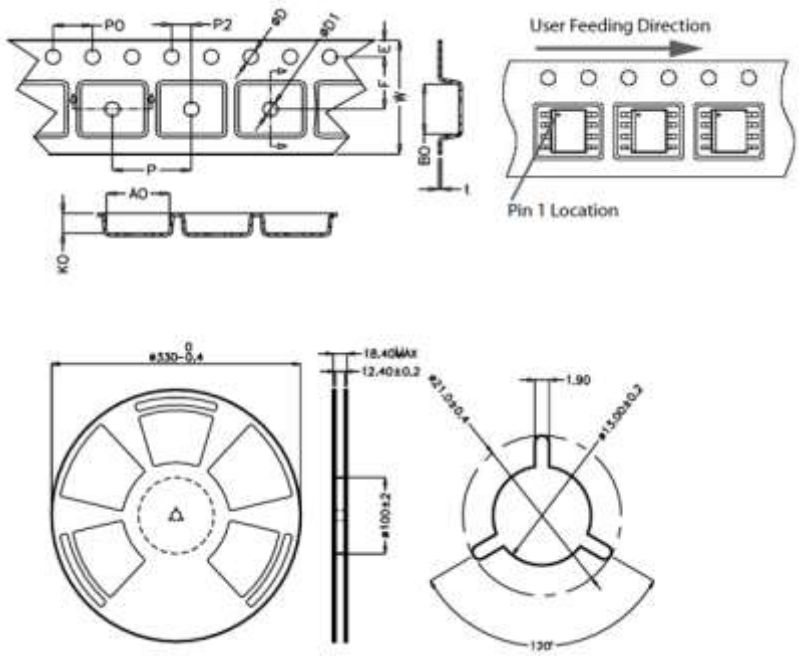
12. Packing Options

Part Number	Marking	Weight	Packing Mode	M.O.Q
STP802U2SRP	STP802U2S	0.08 g	Tape & Reel	2500

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13. Packing Specifications

Embossed Carrier Tape & Reel Specification – SOIC Package



	Millimeters		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	5.4	5.6	0.213	0.22
P2	1.95	2.05	0.077	0.081
D	1.5	1.6	0.059	0.063
D1	1.50 Min		0.059 Min	
P0	3.9	4.1	0.154	0.161
10P0	40.0 ± 0.20		1.574 ± 0.008	
W	11.9	12.1	0.468	0.476
P	7.9	8.1	0.311	0.319
A0	6.3	6.5	0.248	0.256
B0	5.1	5.3	0.2	0.209
K0	2	2.2	0.079	0.087
t	0.30 ± 0.05		0.012 ± 0.002	

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