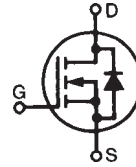


# High Voltage HiperFET IXFP05N100M

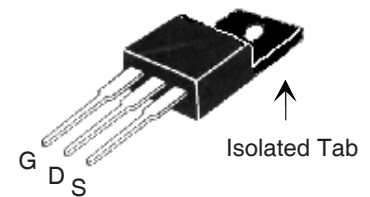
(Electrically Isolated Tab)



N-Channel Enhancement Mode  
Avalanche Rated

$$\begin{aligned}
 V_{DSS} &= 1000V \\
 I_{D25} &= 700mA \\
 R_{DS(on)} &\leq 17\Omega \\
 t_{rr} &\leq 300ns
 \end{aligned}$$

OVERMOLDED TO-220  
(IXFP...M) OUTLINE



G = Gate      D = Drain  
S = Source

Symbol	Test Conditions	Maximum Ratings	
$V_{DSS}$	$T_J = 25^\circ\text{C}$ to $150^\circ\text{C}$	1000	V
$V_{DGR}$	$T_J = 25^\circ\text{C}$ to $150^\circ\text{C}$ , $R_{GS} = 1\text{ M}\Omega$	1000	V
$V_{GSS}$	Continuous	$\pm 30$	V
$V_{GSM}$	Transient	$\pm 40$	V
$I_{D25}$	$T_C = 25^\circ\text{C}$	700	mA
$I_{DM}$	$T_C = 25^\circ\text{C}$ , pulse width limited by $T_{JM}$	3	A
$I_A$	$T_C = 25^\circ\text{C}$	1	A
$E_{AS}$	$T_C = 25^\circ\text{C}$	100	mJ
$dv/dt$	$I_S \leq I_{DM}$ , $V_{DD} \leq V_{DSS}$ , $T_J = 150^\circ\text{C}$	5	V/ns
$P_D$	$T_C = 25^\circ\text{C}$	25	W
$T_J$		- 55 ... +150	$^\circ\text{C}$
$T_{JM}$		150	$^\circ\text{C}$
$T_{stg}$		- 55 ... +150	$^\circ\text{C}$
$T_L$	1.6 mm (0.062 in.) from case for 10 s	300	$^\circ\text{C}$
$T_{SOLD}$	Plastic body for 10 s	260	$^\circ\text{C}$
$M_d$	Mounting torque	1.13/10	Nm/lb.in.
<b>Weight</b>		2.5	g

## Features

- Plastic overmolded tab for electrical isolation
- International standard package
- Avalanche rated
- Low package inductance

## Advantages

- Easy to mount
- Space savings
- High power density

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ , unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
$BV_{DSS}$	$V_{GS} = 0V$ , $I_D = 250\mu\text{A}$	1000		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\mu\text{A}$	2.5		V
$I_{GSS}$	$V_{GS} = \pm 30V$ , $V_{DS} = 0V$			$\pm 100$ nA
$I_{DSS}$	$V_{DS} = V_{DSS}$ $V_{GS} = 0V$ $T_J = 125^\circ\text{C}$			25 $\mu\text{A}$ 500 $\mu\text{A}$
$R_{DS(on)}$	$V_{GS} = 10V$ , $I_D = 375\text{mA}$ , Note 1		15	17 $\Omega$

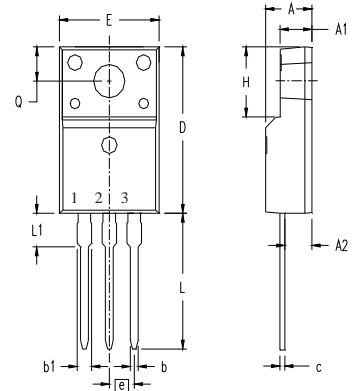
Symbol	Test Conditions	Characteristic Values ( $T_J = 25^\circ\text{C}$ , unless otherwise specified)		
		Min.	Typ.	Max.
$g_{fs}$	$V_{DS} = 20\text{V}$ , $I_D = 500\text{mA}$ , Note 1	0.55	0.93	S
$C_{iss}$	$V_{GS} = 0\text{V}$ , $V_{DS} = 25\text{V}$ , $f = 1\text{MHz}$		260	pF
$C_{oss}$			22	pF
$C_{rss}$			8	pF
$t_{d(on)}$	<b>Resistive Switching Times</b> $V_{GS} = 10\text{V}$ , $V_{DS} = 0.5 \cdot V_{DSS}$ , $I_D = 1\text{A}$ $R_G = 47\Omega$ (External)		11	ns
$t_r$			19	ns
$t_{d(off)}$			40	ns
$t_f$			28	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}$ , $V_{DS} = 0.5 \cdot V_{DSS}$ , $I_D = 1\text{A}$		7.8	nC
$Q_{gs}$			1.4	nC
$Q_{gd}$			4.1	nC
$R_{thJC}$				5.0 $^\circ\text{C/W}$

### Source-Drain Diode

Symbol	Test Conditions	Characteristic Values ( $T_J = 25^\circ\text{C}$ unless otherwise specified)		
		Min.	Typ.	Max.
$I_S$	$V_{GS} = 0\text{V}$			750 mA
$I_{SM}$	Repetitive, pulse width limited by $T_{JM}$			3 A
$V_{SD}$	$I_F = I_S$ , $V_{GS} = 0\text{V}$ , Note 1			1.5 V
$t_{rr}$	$I_F = 1\text{A}$ , $-di/dt = 100\text{A}/\mu\text{s}$ , $V_R = 100\text{V}$ , $V_{GS} = 0\text{V}$		1.8	300 ns
$I_{RM}$				A
$Q_{RM}$			200	nC

Notes: 1. Pulse test,  $t \leq 300 \mu\text{s}$ ; duty cycle,  $d \leq 2\%$ .

### ISOLATED TO-220 (IXFP...M)



Terminals: 1 - Gate  
2 - Drain (Collector)  
3 - Source (Emitter)

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.177	.193	4.50	4.90
A1	.092	.108	2.34	2.74
A2	.101	.117	2.56	2.96
b	.028	.035	0.70	0.90
b1	.050	.058	1.27	1.47
c	.018	.024	0.45	0.60
D	.617	.633	15.67	16.07
E	.392	.408	9.96	10.36
e	.100 BSC		2.54 BSC	
H	.255	.271	6.48	6.88
L	.499	.523	12.68	13.28
L1	.119	.135	3.03	3.43
$\varnothing P$	.121	.129	3.08	3.28
Q	.126	.134	3.20	3.40

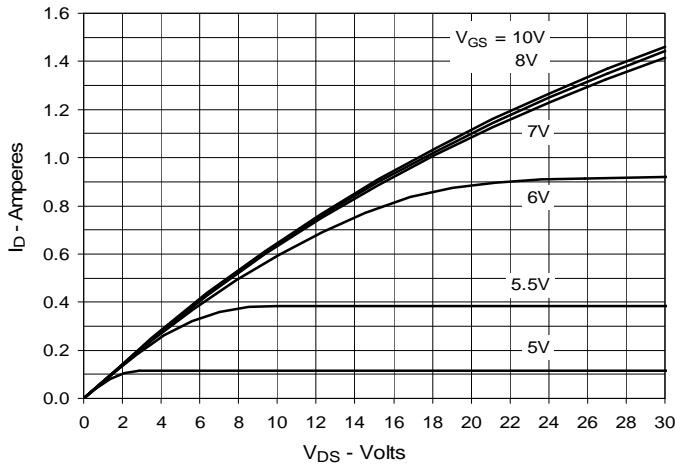
### PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

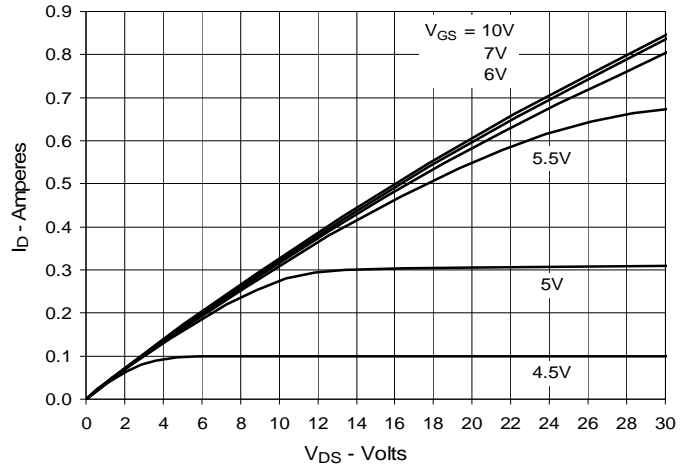
IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
	4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

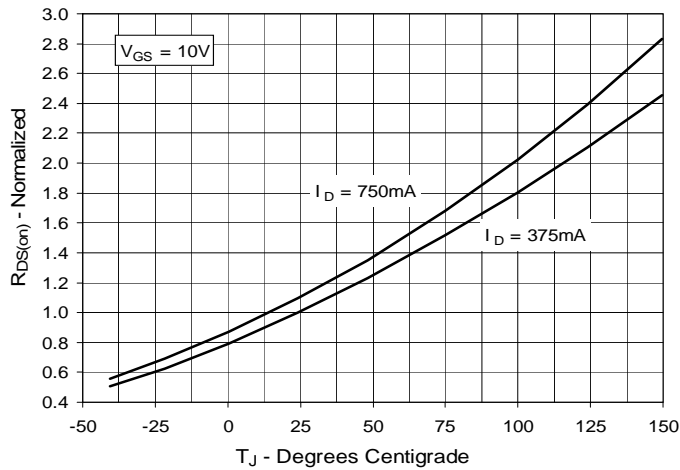
**Fig. 1. Output Characteristics @ 25°C**



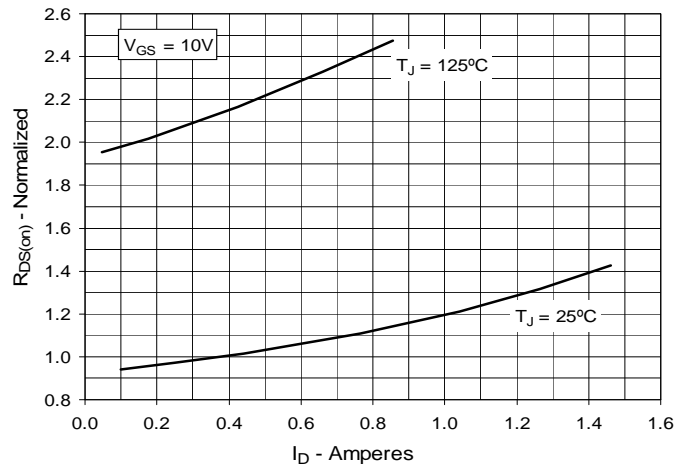
**Fig. 2. Output Characteristics @ 125°C**



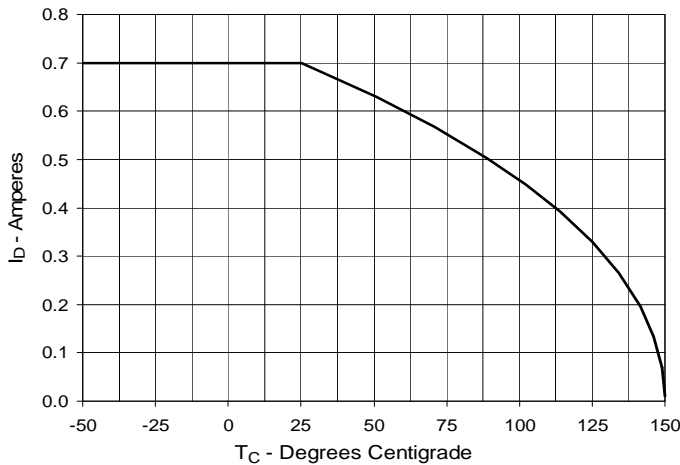
**Fig. 3.  $R_{DS(on)}$  Normalized to  $I_D = 375mA$  Value vs. Junction Temperature**



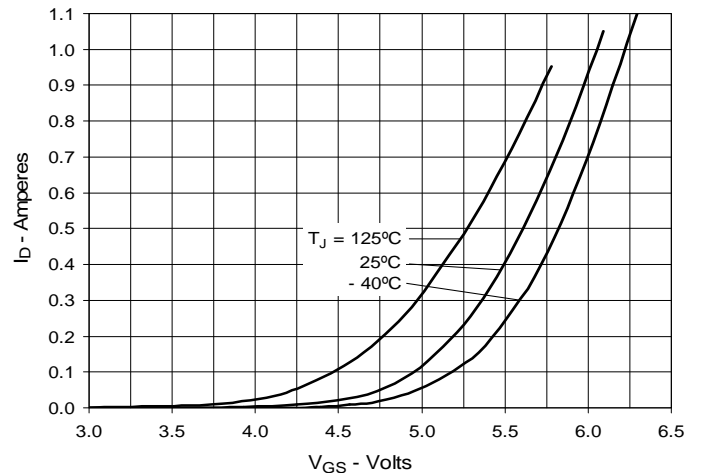
**Fig. 4.  $R_{DS(on)}$  Normalized to  $I_D = 375mA$  Value vs. Drain Current**



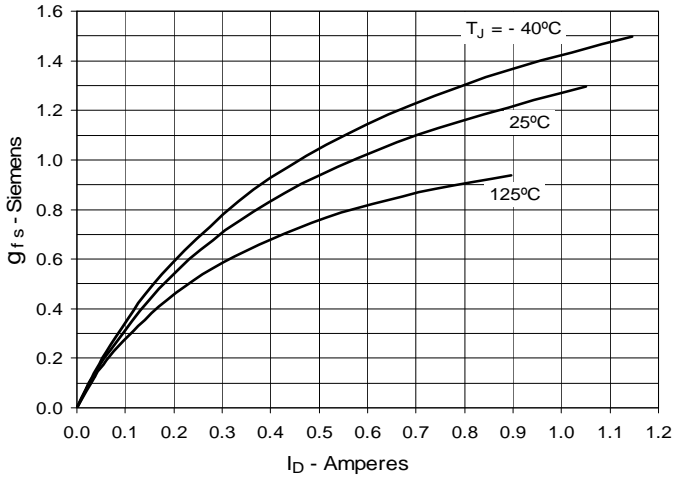
**Fig. 5. Maximum Drain Current vs. Case Temperature**



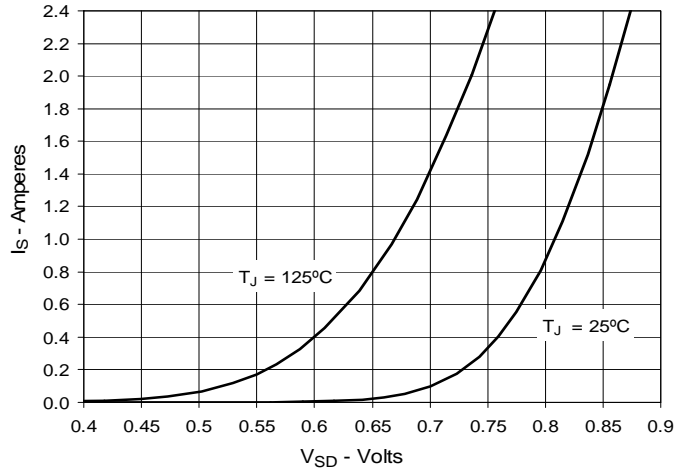
**Fig. 6. Input Admittance**



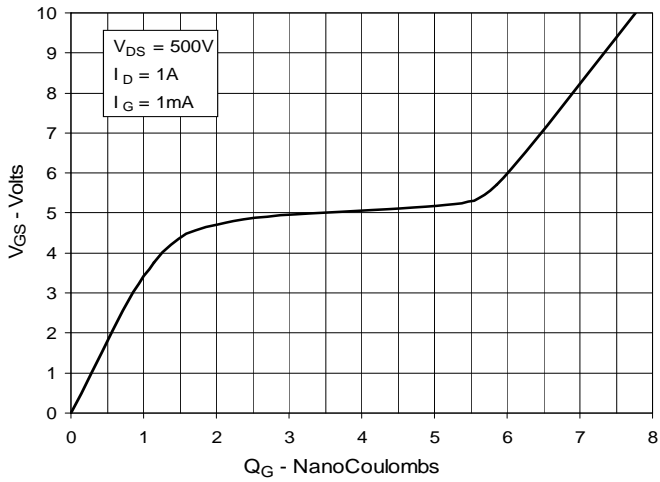
**Fig. 7. Transconductance**



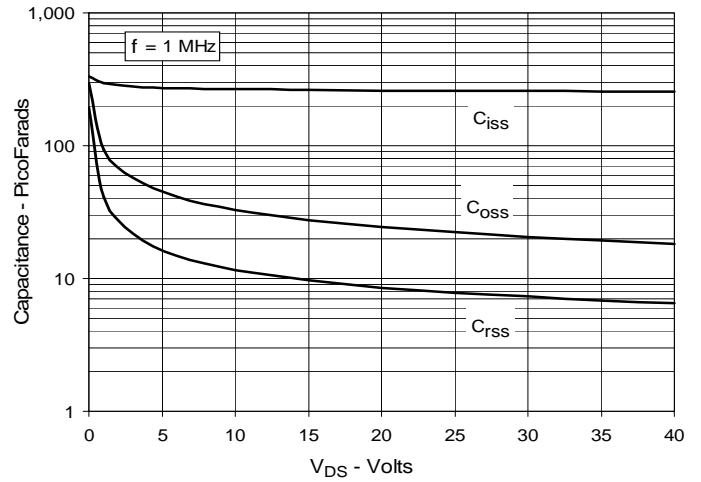
**Fig. 8. Forward Voltage Drop of Intrinsic Diode**



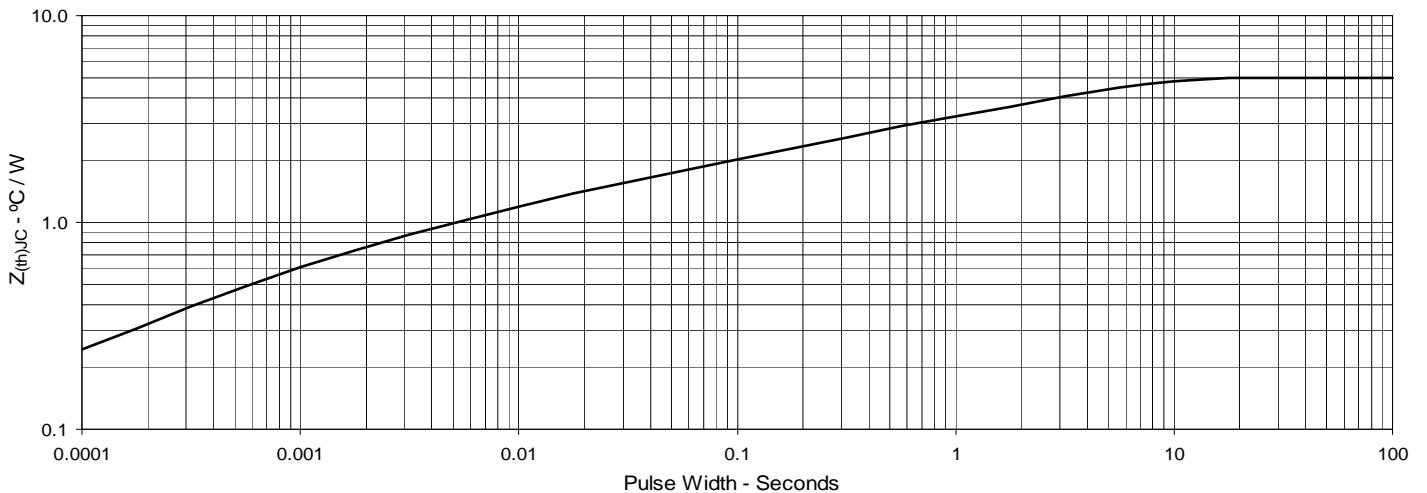
**Fig. 9. Gate Charge**



**Fig. 10. Capacitance**



**Fig. 11. Maximum Transient Thermal Impedance**



IXYS reserves the right to change limits, test conditions, and dimensions.



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