

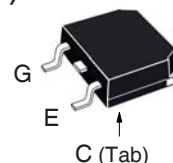
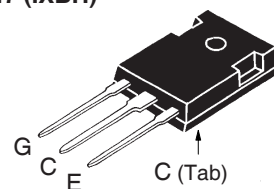
**High Voltage, High Gain
BIMOSFET™**
**IXBH2N250
IXBT2N250**
**Monolithic Bipolar MOS
Transistor**


$$V_{CES} = 2500V$$

$$I_{C110} = 2A$$

$$V_{CE(sat)} \leq 3.80V$$

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	$T_C = 25^\circ C$ to $150^\circ C$	2500	V
V_{CGR}	$T_J = 25^\circ C$ to $150^\circ C$, $R_{GE} = 1M\Omega$	2500	V
V_{GES}	Continuous	± 20	V
V_{GEM}	Transient	± 30	V
I_{C25}	$T_C = 25^\circ C$	5	A
I_{C110}	$T_C = 110^\circ C$	2	A
I_{CM}	$T_C = 25^\circ C$, 1ms	13	A
SSOA	$V_{GE} = 15V$, $T_{VJ} = 125^\circ C$, $R_G = 47\Omega$	$I_{CM} = 6$	A
(RBSOA)	Clamped Inductive Load	$V_{CE} \leq 2000$	V
P_C	$T_C = 25^\circ C$	32	W
T_J		-55 ... +150	$^\circ C$
T_{JM}		150	$^\circ C$
T_{stg}		-55 ... +150	$^\circ C$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ C$
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	$^\circ C$
M_d	Mounting Torque (TO-247)	1.13 / 10	Nm/lb.in
Weight	TO-247	6	g
	TO-268	4	g

TO-268 (IXBT)

TO-247 (IXBH)


G = Gate D = Drain
S = Source Tab = Drain

G = Gate C = Collector
E = Emitter Tab = Collector

Features

- High Blocking Voltage
- Integrated Anti-parallel Diode
- International Standard Packages
- Low Conduction Losses

Advantages

- Low Gate Drive Requirement
- High Power Density

Applications

- Switched-Mode and Resonant-Mode Power Supplies
- Uninterruptible Power Supplies (UPS)
- Laser Generator
- Capacitor Discharge Circuit
- AC Switches

Symbol	Test Conditions ($T_J = 25^\circ C$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{CES}	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	2500		V
$V_{GE(th)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	3.0		5.5 V
I_{CES}	$V_{CE} = 0.8 \cdot V_{CES}$, $V_{GE} = 0V$ $T_J = 125^\circ C$			10 μA 100 μA
I_{GES}	$V_{CE} = 0V$, $V_{GE} = \pm 20V$			± 100 nA
$V_{CE(sat)}$	$I_C = 2A$, $V_{GE} = 15V$, Note 1 $T_J = 125^\circ C$	3.15		V
		4.08		V

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$I_C = 2\text{A}, V_{CE} = 10\text{V}$, Note 1	0.85	1.40	S
C_{ies}	$V_{CE} = 25\text{V}, V_{GE} = 0\text{V}, f = 1\text{MHz}$		145	pF
C_{oes}			8.7	pF
C_{res}			3.2	pF
Q_g	$I_C = 2\text{A}, V_{GE} = 15\text{V}, V_{CE} = 1\text{kV}$		10.6	nC
Q_{ge}			0.8	nC
Q_{gc}			6.2	nC
$t_{d(on)}$	Resistive Switching times, $T_J = 25^\circ\text{C}$ $I_C = 2\text{A}, V_{GE} = 15\text{V}$ $V_{CE} = 2\text{kV}, R_G = 47\Omega$		30	ns
t_r			180	ns
$t_{d(off)}$			70	ns
t_f			182	ns
$t_{d(on)}$	Resistive Switching times, $T_J = 125^\circ\text{C}$ $I_C = 2\text{A}, V_{GE} = 15\text{V}$ $V_{CE} = 2\text{kV}, R_G = 47\Omega$		30	ns
t_r			280	ns
$t_{d(off)}$			74	ns
t_f			178	ns
R_{thJC}			3.90	$^\circ\text{C/W}$
R_{thCS}		0.21		$^\circ\text{C/W}$

Reverse Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
V_F	$I_F = 2\text{A}, V_{GE} = 0\text{V}$, Note 1			2.4 V
t_{rr}	$I_F = 2\text{A}, V_{GE} = 0\text{V}, -di_f/dt = 100\text{A}/\mu\text{s}$ $V_R = 100\text{V}, V_{GE} = 0\text{V}$		0.92	μs
I_{RM}			9.80	A
Q_{RM}			4.50	μC

Note 1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

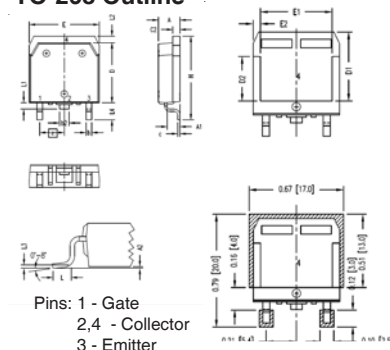
PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions and Dimensions.

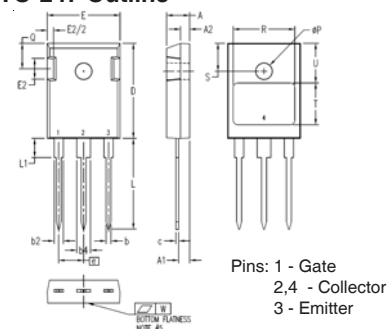
IXYS MOSFETs and IGBTs are covered 4,835,592 4,931,844 5,049,961 5,237,481 6,162,665 6,404,065 B1 6,683,344 6,727,585 7,005,734 B2 7,157,338B2
by one or more of the following U.S. patents: 4,860,072 5,017,508 5,063,307 5,381,025 6,259,123 B1 6,534,343 6,710,405 B2 6,759,692 7,063,975 B2
4,881,106 5,034,796 5,187,117 5,486,715 6,306,728 B1 6,583,505 6,710,463 6,771,478 B2 7,071,537

TO-268 Outline



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.193	.201	4.90	5.10
A1	.106	.114	2.70	2.90
A2	.001	.010	0.02	0.25
b	.045	.057	1.15	1.45
b2	.075	.083	1.90	2.10
C	.016	.026	0.40	0.65
C2	.057	.063	1.45	1.60
D	.543	.551	13.80	14.00
D1	.488	.500	12.40	12.70
D2	.320	.335	8.13	8.50
E	.624	.632	15.85	16.05
E1	.524	.535	13.30	13.60
E2	.045	.055	1.14	1.39
e	.215	BSC	5.45	BSC
H	.736	.752	18.70	19.10
L	.094	.106	2.40	2.70
L1	.047	.055	1.20	1.40
L2	.039	.045	1.00	1.15
L3	.010	BSC	0.25	BSC
L4	.150	.161	3.80	4.10

TO-247 Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.087	.100	2.21	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b2	.075	.085	1.91	2.16
b4	.115	.126	2.92	3.20
c	.023	.033	0.58	0.84
D	.820	.840	20.83	21.34
E	.620	.635	15.75	16.13
E2	.175	.195	4.44	4.95
e	.215	BSC	5.45	BSC
L	.780	.810	19.81	20.57
L1	.160	.177	4.06	4.50
Q	.220	.240	5.59	6.10
R	.520	.540	13.21	13.72
S	.242	BSC	6.15	BSC
T	.355	.375	9.02	9.53
U	.345	.370	8.76	9.40
ØP	.140	.144	3.55	3.66
W	.000	.004	0.00	0.10

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

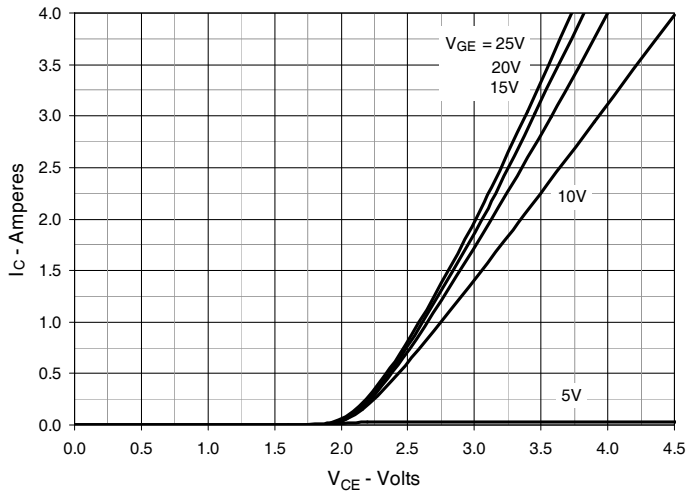


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

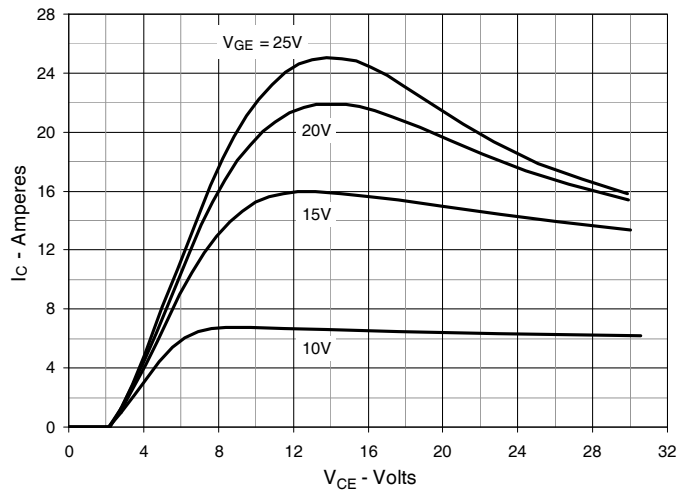


Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

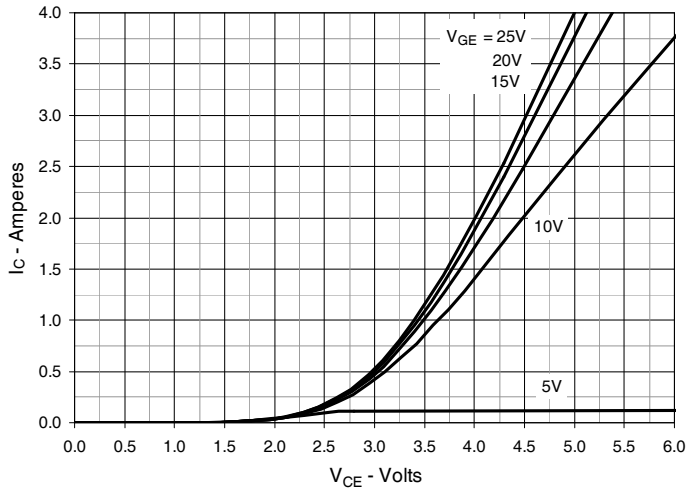


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

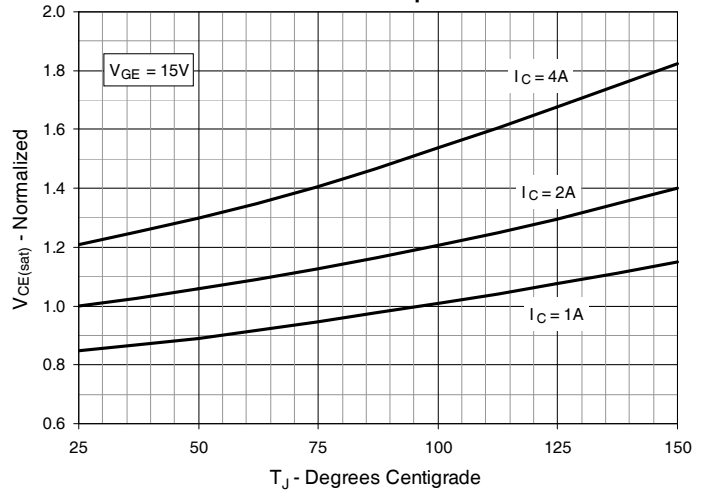


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

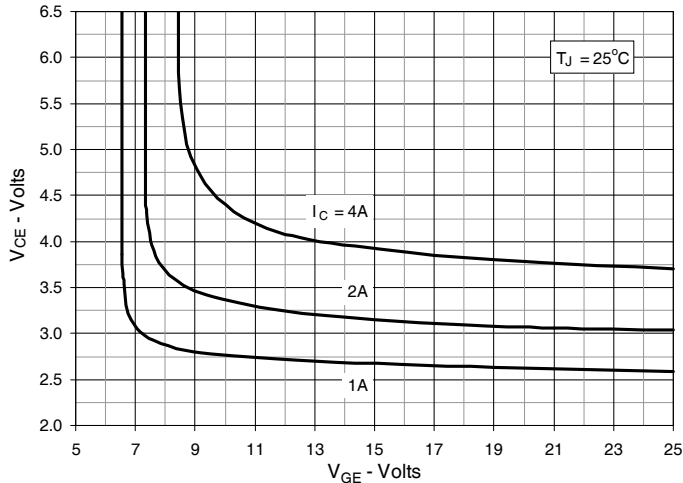


Fig. 6. Input Admittance

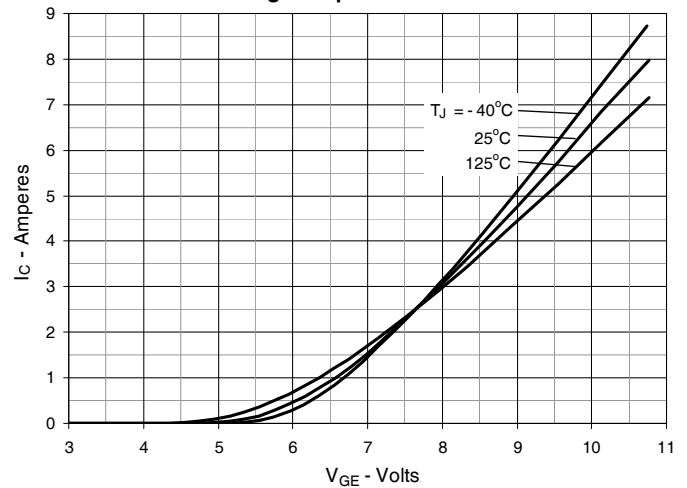


Fig. 7. Transconductance

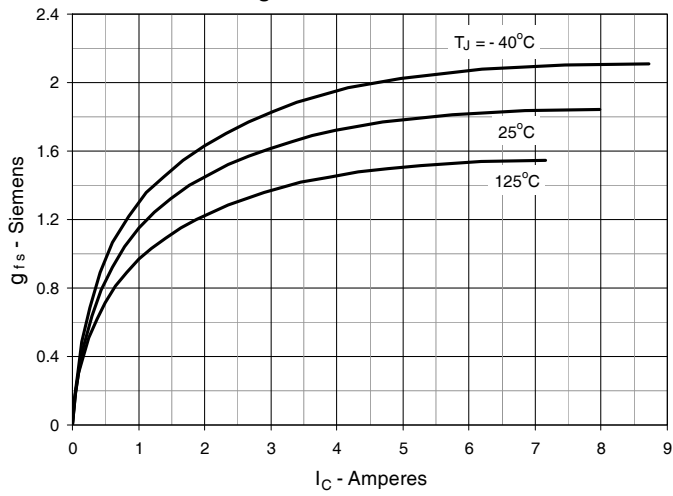


Fig. 8. Forward Voltage Drop of Intrinsic Diode

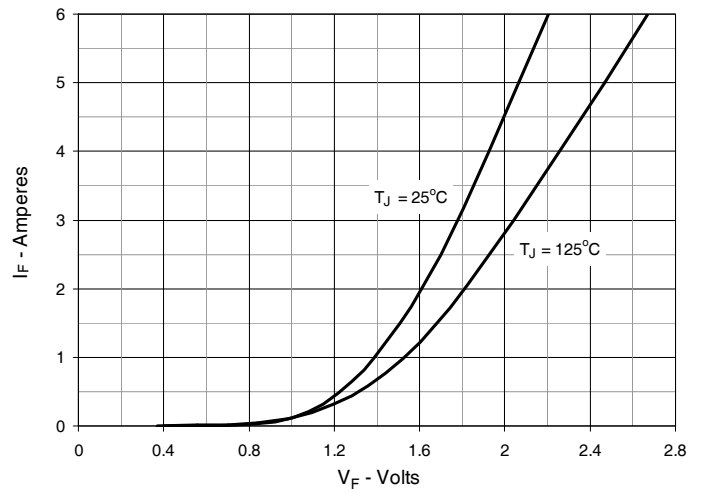


Fig. 9. Gate Charge

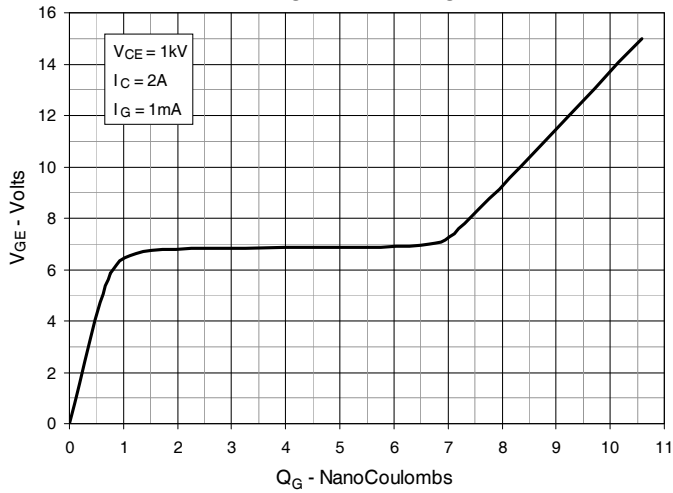


Fig. 10. Capacitance

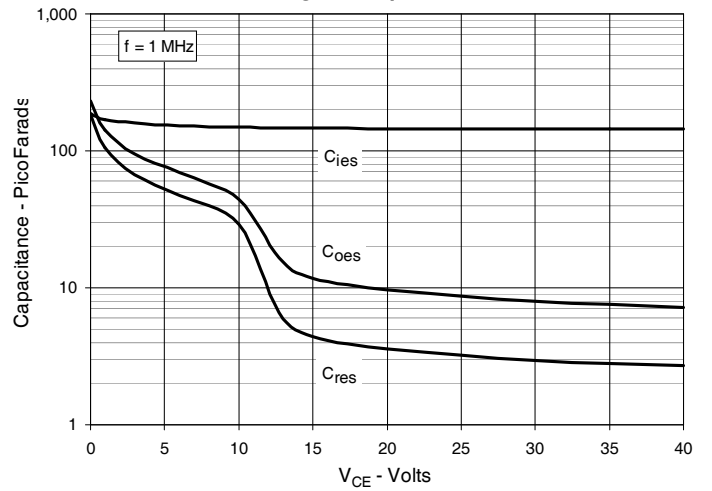


Fig. 11. Reverse-Bias Safe Operating Area

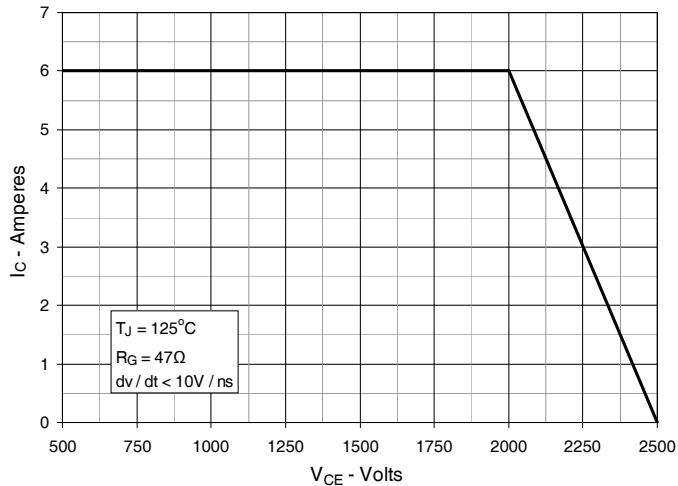


Fig. 12. Maximum Transient Thermal Impedance

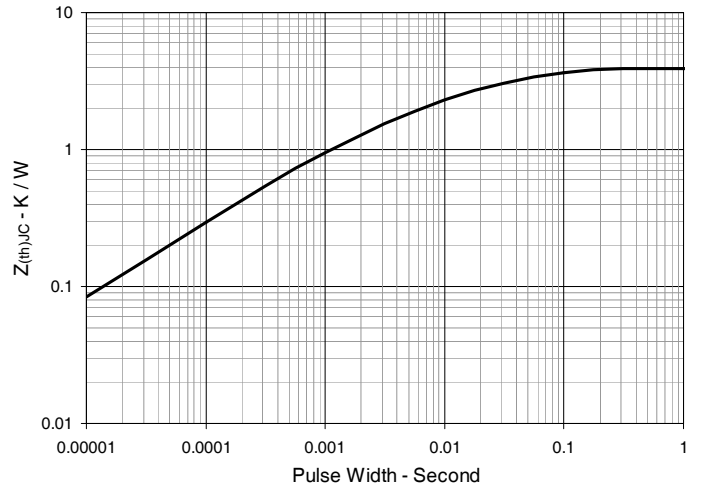


Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

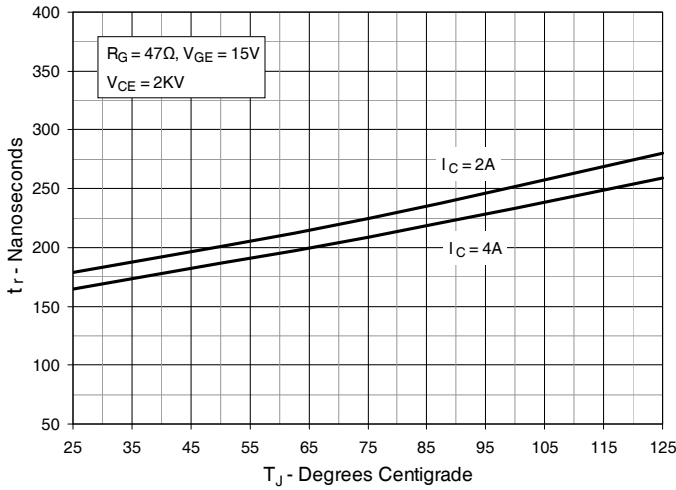


Fig. 14. Resistive Turn-on Rise Time vs. Collector Current

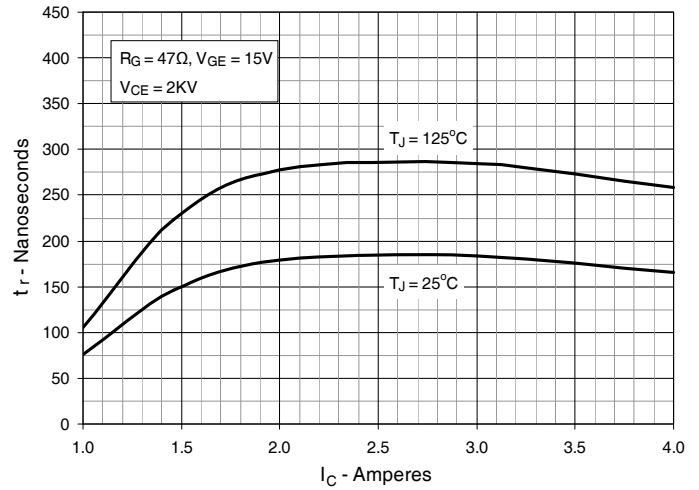


Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

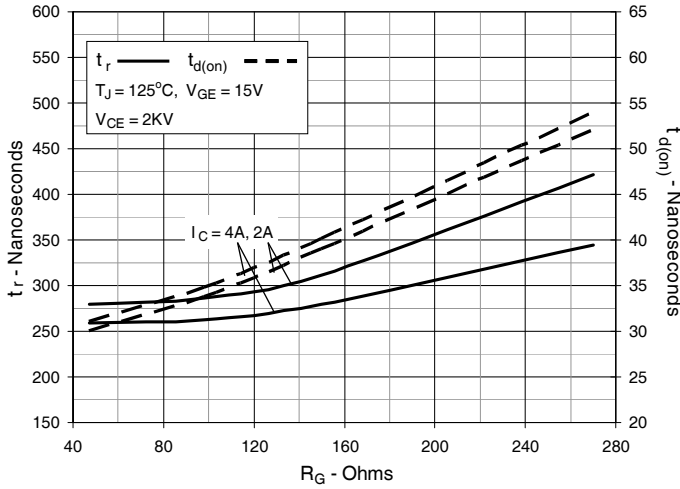


Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

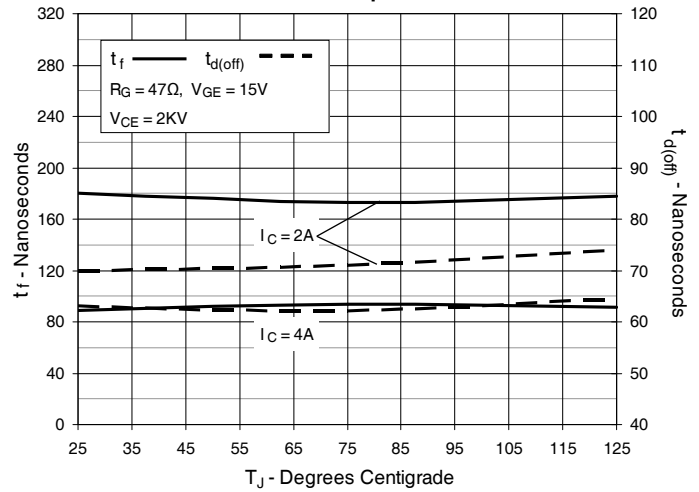


Fig. 17. Resistive Turn-off Switching Times vs. Collector Current

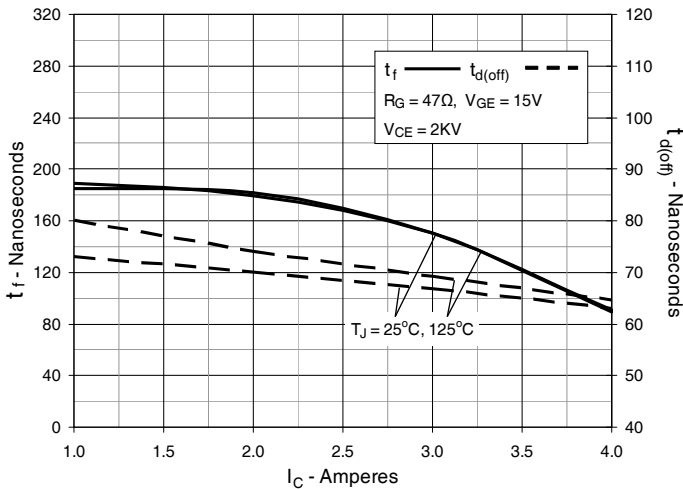
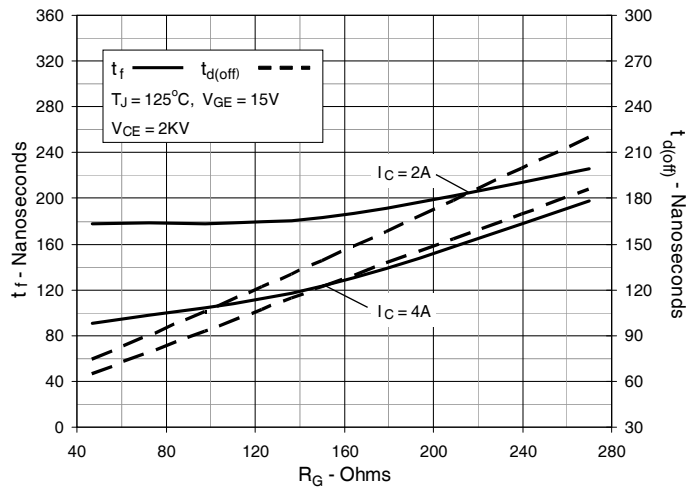


Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance





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