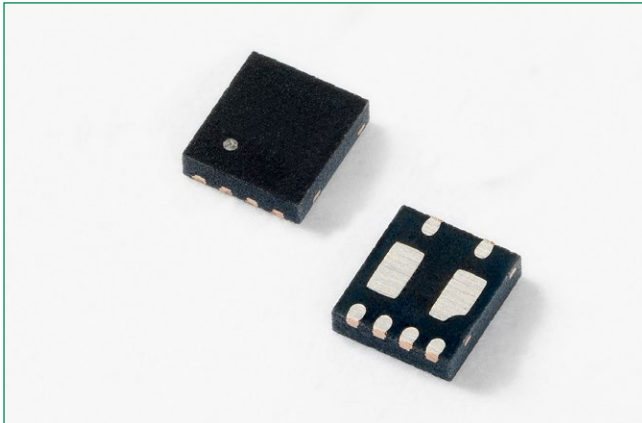


## SP1255P Series 0.5pF, 12kV Diode Array for $\mu$ USB

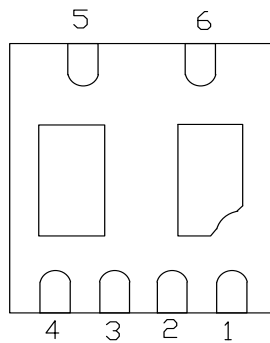


### Description

The SP1255P integrates three channels of ultra-low capacitance steering diodes and a low voltage TVS diode to provide maximum protection of the USB data and ID pins against ESD per the IEC 61000-4-2 standard. An additional 12V TVS diode is included to provide lightning surge protection for the USB  $V_{BUS}$  pin up to 100A ( $t_p=8/20\mu s$ ) per the IEC 61000-4-5 standard. The SP1255P provides superior protection for current intensive applications such as fast charging peripherals.

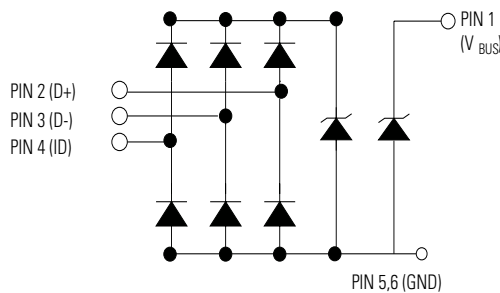
The SP1255P comes in a space saving 2.0x1.8mm  $\mu$ DFN package with a typical height of 0.55mm making it an ideal solution for smart phones, tablets, and other portable electronics.

### Pinout



Bottom View

### Functional Block Diagram



Life Support Note:

**Not Intended for Use in Life Support or Life Saving Applications**

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

### Features

- RoHS compliant and lead-free
- AEC-101 qualified

For USB Voltage Bus Pin ( $V_{BUS}$ )

- ESD, IEC 61000-4-2,  $\pm 30kV$  contact,  $\pm 30kV$  air
- EFT, IEC 61000-4-4, 80A ( $t_p=5/50ns$ )
- Lightning, IEC 61000-4-5, 100A ( $t_p=8/20\mu s$ )
- Protection for  $V_{BUS}$  operating up to 12V
- Benchmark setting protection
- High current handling capability for fast charging applications

For USB Data Pin (D+, D-, ID)

- ESD, IEC 61000-4-2,  $\pm 12kV$  contact,  $\pm 15kV$  air
- EFT, IEC 61000-4-4, 40A ( $t_p=5/50ns$ )
- Lightning, IEC 61000-4-5 2nd edition, 4A ( $t_p=8/20\mu s$ )
- 0.5pF capacitance
- Low clamping voltage and dynamic resistance (0.3 $\Omega$ )

### Applications

- USB 2.0
- USB OTG
- $\mu$ USB
- Protection for the  $V_{BUS}$  circuit on USB2.0 Fast Charging

### Additional Information



Datasheet



Resources



Samples

### Absolute Maximum Ratings

Symbol	Parameter	Value	Units
$I_{PP}$ (Pin 1)	Peak Current ( $t_p=8/20\mu s$ )	100	A
$I_{PP}$ (Pin 2-4)	Peak Current ( $t_p=8/20\mu s$ )	4	A
$T_{OP}$	Operating Temperature	-40 to 125	°C
$T_{STOR}$	Storage Temperature	-55 to 150	°C

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

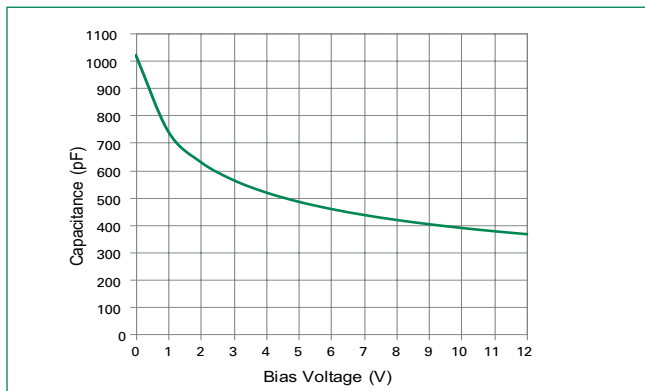
### Electrical Characteristics ( $T_{OP}=25^\circ C$ )

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
USB $V_{BUS}$ (Pin 1)						
Reverse Standoff Voltage	$V_{RWM}$	Pin 1 to GND			12	V
Reverse Breakdown Voltage	$V_{BR}$	$I_T=1mA$ , Pin 1 to GND	13.0	13.5	16.5	V
Reverse Leakage Current	$I_{LEAK}$	$V_R=12V$ , Pin 1 to GND			0.1	$\mu A$
Forward Voltage	$V_F$	$I_F=10mA$ , GND to Pin 1	0.6	0.7	1.0	V
Clamp Voltage <sup>1</sup>	$V_C$	$I_{PP}=30A$ , $t_p=8/20\mu s$ , Fwd		16.5	18	V
		$I_{PP}=100A$ , $t_p=8/20\mu s$ , Fwd		19.5	25	V
ESD Withstand Voltage <sup>1</sup>	$V_{ESD}$	IEC 61000-4-2 (Contact)	$\pm 30$			kV
		IEC 61000-4-2 (Air)	$\pm 30$			kV
Diode Capacitance <sup>1</sup>	$C_D$	Reverse Bias=0V, $f=1MHz$		1300	2500	pF
USB D+, D-, ID (Pin 2, 3, 4)						
Reverse Standoff Voltage	$V_{RWM}$	Pin 2, 3 and 4 to GND			4	V
Reverse Breakdown Voltage	$V_{BR}$	$I_T=2\mu A$ , Pin 2, 3 and 4 to GND	4.5	6.0	7.5	V
Reverse Leakage Current	$I_{LEAK}$	$V_R=2V$ , Pin 2, 3 and 4 to GND			0.02	$\mu A$
		$V_R=4V$ , Pin 2, 3 and 4 to GND			0.1	
Clamp Voltage <sup>1</sup>	$V_C$	$I_{PP}=1A$ , $t_p=8/20\mu s$ , Fwd		6.6	8.0	V
		$I_{PP}=2A$ , $t_p=8/20\mu s$ , Fwd		7.0	8.5	V
Dynamic Resistance	$R_{DYN}$	TLP, $t_p=100ns$ , Pin 2, 3 and 4 to GND <sup>2</sup>		0.3		$\Omega$
ESD Withstand Voltage <sup>1</sup>	$V_{ESD}$	IEC 61000-4-2 (Contact)	$\pm 12$			kV
		IEC 61000-4-2 (Air)	$\pm 15$			kV
Diode Capacitance <sup>1</sup>	$C_{VO-GND}$	Reverse Bias=0V, $f=1MHz$		0.5	0.6	pF

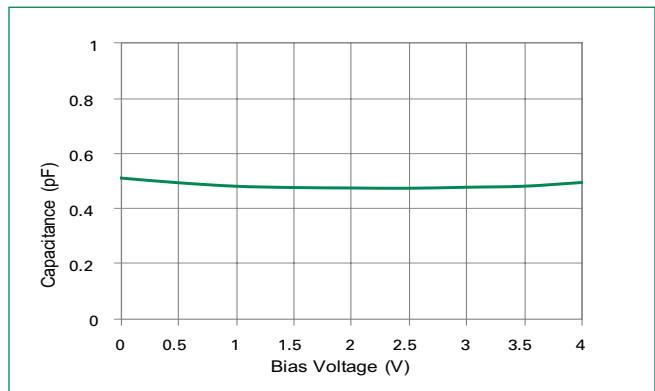
**Note:** 1 Parameter is guaranteed by design and/or device characterization.

2 Transmission Line Pulse (TLP) Test Setting:  $t_r=100ns$ ,  $t_f=0.2ns$   $I_{TL}$  and  $V_{TL}$ , averaging window: star  $t_r=70ns$  to  $t_f=90ns$

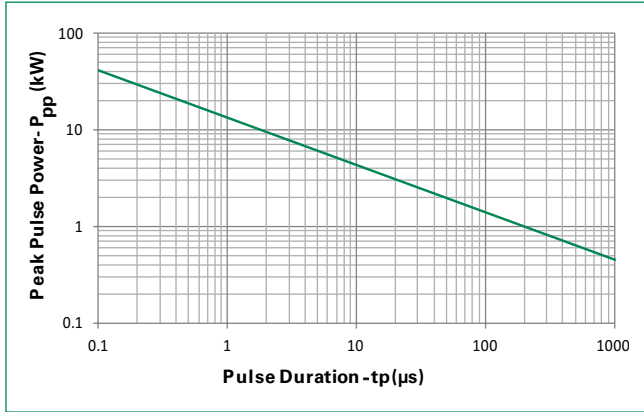
### Capacitance vs. Reverse Bias (Pin 1 to GND)



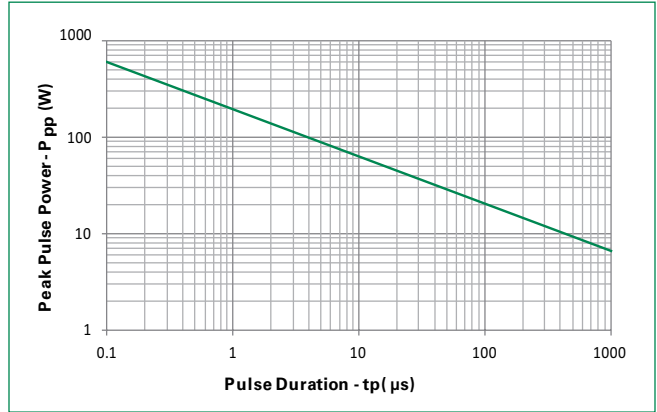
### Capacitance vs. Reverse Bias (Pin2, 3, 4 to GND)



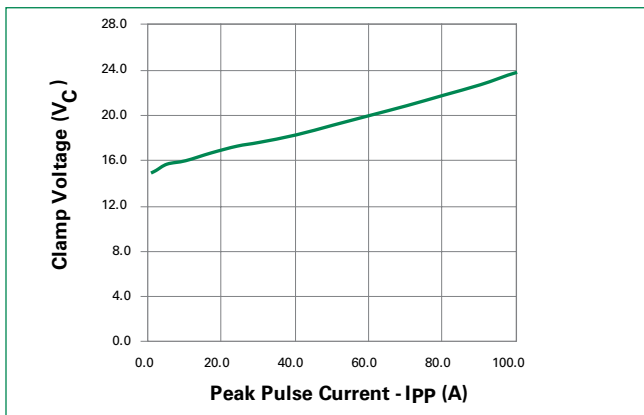
**Non-Repetitive Peak Pulse Power vs. Pulse Duration (Pin1 to GND)**



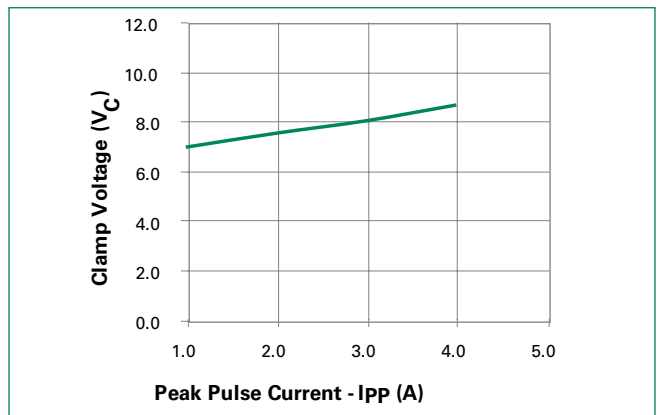
**Non-Repetitive Peak Pulse Power vs. Pulse Duration (Pin2, 3, 4 to GND)**



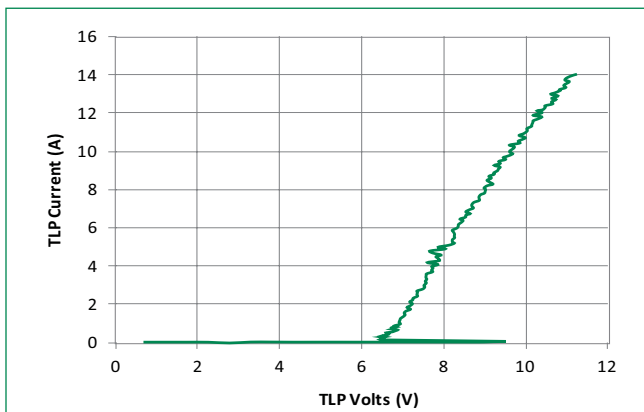
**Clamping Voltage vs. Peak Pulse Current (Pin1 to GND)**



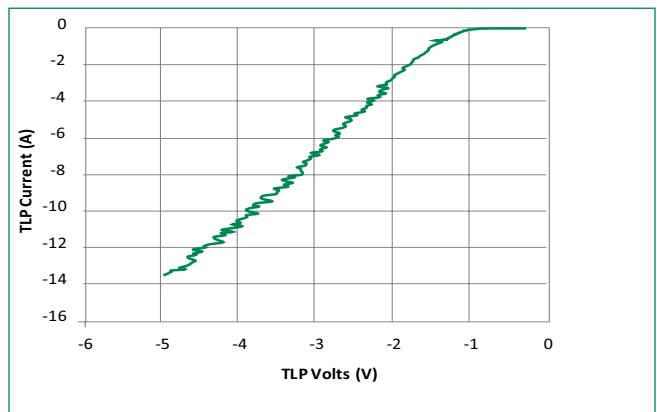
**Clamping Voltage vs. Peak Pulse Current (Pin2, 3, 4 to GND)**



**Positive Transmission Line Pulsing (TLP) Plot (Pin 2, 3, 4 to GND)**

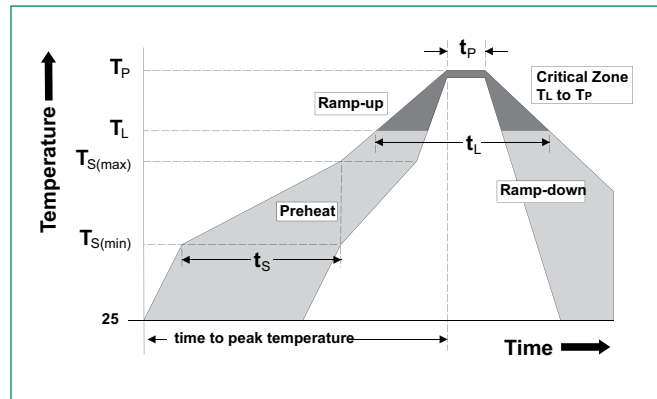


**Negative Transmission Line Pulsing (TLP) Plot (Pin 2, 3, 4 to GND)**

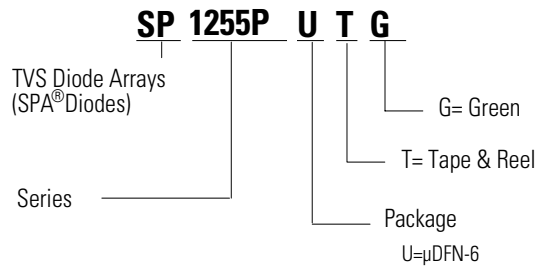


### Soldering Parameters

<b>Reflow Condition</b>		Pb – Free assembly
<b>Pre Heat</b>	- Temperature Min ( $T_{s(min)}$ )	150°C
	- Temperature Max ( $T_{s(max)}$ )	200°C
	- Time (min to max) ( $t_s$ )	60 – 180 secs
<b>Average ramp up rate (Liquidus) Temp (<math>T_L</math>) to peak</b>		3°C/second max
<b><math>T_{s(max)}</math> to <math>T_L</math> - Ramp-up Rate</b>		3°C/second max
<b>Reflow</b>	- Temperature ( $T_L$ ) (Liquidus)	217°C
	- Temperature ( $t_L$ )	60 – 150 seconds
<b>Peak Temperature (<math>T_p</math>)</b>		260 <sup>+0/-5</sup> °C
<b>Time within 5°C of actual peak Temperature (<math>t_p</math>)</b>		20 – 40 seconds
<b>Ramp-down Rate</b>		6°C/second max
<b>Time 25°C to peak Temperature (<math>T_p</math>)</b>		8 minutes Max.
<b>Do not exceed</b>		260°C



### Part Numbering System



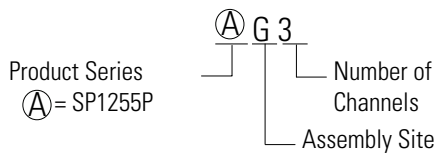
### Product Characteristics

<b>Lead Plating</b>	Pre-Plated Frame
<b>Lead Material</b>	Copper Alloy
<b>Lead Coplanarity</b>	0.0004 inches (0.102mm)
<b>Substrate material</b>	Silicon
<b>Body Material</b>	Molded Epoxy
<b>Flammability</b>	UL 94 V-0

**Notes :**

1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
5. Package surface matte finish VDI 11-13.

### Part Marking System



### Ordering Information

Part Number	Package	Marking	Min. Order Qty.	Packaging Option	P0/P1	Packaging Specification
SP1255PUTG	μDFN-6	Ⓐ3	3000	Tape & Reel – 8mm tape/7" reel	2mm/4mm	EIA RS-481

