CPC7524

Quad High Voltage Isolated Analog Switch Array

Features

- Switch Voltage up to 600V
- 110dB Switch-to-Switch Isolation at 5kHz
- Flexible Switch Configurations
- Smart Logic for Power-Up/Hot-Plug State Control
- 3.3V Operation with Very Low Power Consumption
- Switch Current Limiting and Thermal Shutdown Protects Against Fault Conditions
- TTL Logic-Level Inputs
- Input Latch
- Matched R_{ON}
- Clean, Bounce-Free Switching
- Monolithic IC Reliability

Applications

- Instrumentation
- Industrial Controls and Monitoring
- Worldwide AC Mains Monitor
- Automatic Test Equipment (ATE)
- Battery Monitoring and Charging

Description

The CPC7524 Quad High Voltage (HV) isolated Analog Switch Array builds upon our high voltage design and fabrication expertise for offline and telecom applications. This monolithic solid state device provides the switching functionality of four normally open (1-Form-A) relays in one small economical package.

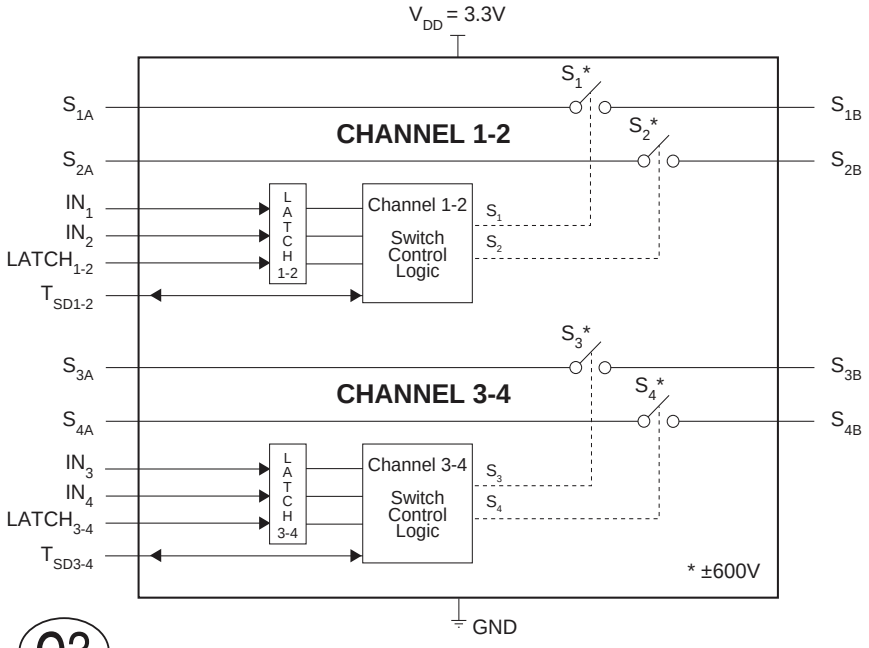
Designed to provide flexible single-ended or differential access to high voltage networks, the CPC7524 high voltage array is configured as two sets of matched paired switches for improved differential performance. Additionally, sensitive differential applications will benefit from the matched pairs' excellent pair-to-pair isolation. The self-biasing switches do not require external high-voltage supplies for proper operation.

Independent switch current limiting and switch-pair thermal shutdown features provide enhanced protection for devices connected to high voltage networks up to ±600V.

Ordering Information

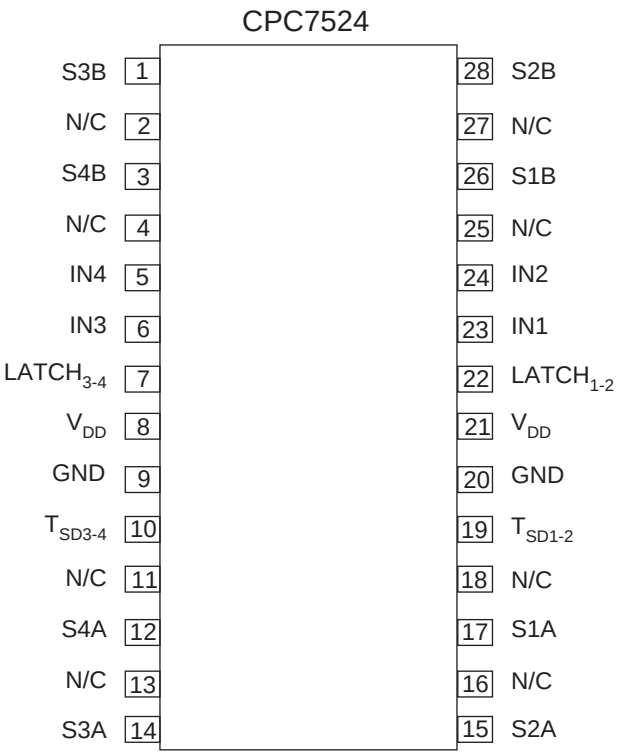
Part #	Description
CPC7524B	28-Pin SOIC in Tubes (29/Tube)
CPC7524BTR	28-Pin SOIC Tape & Reel (1000/Reel)

Figure 1. CPC7524 Block Diagram



1. Specifications

1.1 Package Pinout



1.2 Pin Descriptions

Pin	Name	Description
2, 4, 11, 13, 16, 18, 25, 27	NC	Not Connected
8,21	V_{DD}	Logic Supply Voltage
9, 20	GND	Ground
CHANNEL 1-2		
15	S_{2A}	Switch 2 - side A
17	S_{1A}	Switch 1 - side A
19	T_{SD1-2}	I/O - Thermal shutdown output and All-Off input control for SW1 & SW2
22	$LATCH_{1-2}$	Input - Latch control for SW1 & SW2
23	IN1	Input - Switch 1 state control
24	IN2	Input - Switch 2 state control
26	S_{1B}	Switch 1 - side B
28	S_{2B}	Switch 2 - side B
CHANNEL 3-4		
1	S_{3B}	Switch 3 - side B
3	S_{4B}	Switch 4 - side B
5	IN4	Input - Switch 4 state control
6	IN3	Input - Switch 3 state control
7	$LATCH_{3-4}$	Input - Latch control for SW3 & SW4
10	T_{SD3-4}	I/O - Thermal shutdown output and All-Off input control for SW3 & SW4
12	S_{4A}	Switch 4 - side A
14	S_{3A}	Switch 3 - side A

1.3 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
+3.3V power supply (V_{DD})	-0.3	+ 4	V
Logic input voltage	-0.3	V_{DD} + 0.3	V
Logic input to switch output isolation	-	600	V
Switch open-contact isolation (SW1, SW2, SW3, SW4)	-	600	V
Operating relative humidity	5	95	%
Operating temperature	-40	+110	°C
Storage temperature	-40	+150	°C

Absolute maximum electrical ratings are at 25°C.

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 General Conditions

Unless otherwise specified, minimum and maximum values are guaranteed by production testing. Typical values are characteristic of the device and are the result of engineering evaluations. They are provided for informational purposes only and are not guaranteed by production testing.

Specifications cover the operating temperature range T_A = -40°C to +85°C. Also, unless otherwise specified, all testing is performed with V_{DD} = 3.3V_{DC}, logic low input voltage is 0V_{DC} and logic high input voltage is 3.3V_{DC}.

1.5 Switch Electrical Specifications

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Off-State Leakage Current	V_{SW} (differential) = S_{xA} to S_{xB} V_{SW} (differential) = S_{xB} to S_{xA} Switch Off.	I_{SW}				µA
	+25°C, V_{SW} (differential) = ±600V to Gnd		-	±0.1	±1	
	+85°C, V_{SW} (differential) = ±600V to Gnd			±0.3		
	-40°C, V_{SW} (differential) = ±580V to Gnd			±0.1		
On Resistance	I_{SW}(on) = ±10mA, ±40mA	R_{ON}				Ω
	+25°C		-	50	-	
	+85°C		-	75	95	
	-40°C		-	27	-	
On Resistance Matching	Per On Resistance test conditions	ΔR_{ON}				Ω
	SW1 & SW2		-	2	7	
	SW3 & SW4					
ON-State Voltage [2]	Maximum Differential Voltage [1]	V_{ON}	-	-	600	V
Low Frequency Current Limit 1 [2]	V_{SW} (on) = ±15V	I_{LIM1}				mA
	+25°C		200	300	-	
	+85°C		80	-	-	
	-40°C		-	-	500	
High Frequency Dynamic Current Limit (t ≤0.5 µs)	Switches on, Apply ±1 kV 10x1000 µs pulse with appropriate protection in place	I_{SW}	-	1	-	A
Logic Input to Switch Output Isolation	V_{SW}: V_{SxA} = V_{SxB} to Gnd	I_{SW}				µA
	+25°C, V_{SW} = ±600V		-	±0.1	-	
	+85°C, V_{SW} = ±600V		-	±0.3	±1	
	-40°C, V_{SW} = ±550V		-	±0.1	-	
Switch to Switch Isolation	Any switch to any other switch f=5kHz		110	-	-	dB
Transient Immunity	100V_{P-P} Square Wave at 100Hz	dV/dt	1500	2100	-	V/µs

[1] Choice of high voltage side protector should ensure this rating is not exceeded.
[2] See **"Figure 1: Switch Low Frequency Response" on page 12**.

1.6 Digital I/O Electrical Specifications

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Input Characteristics						
Input Voltage: (IN_x, $LATCH_x$, T_{SDx})						
Logic High	Input voltage rising	V_{IH}	-	1.5	2.0	V
Logic Low	Input voltage falling	V_{IL}	0.8	1	-	V
Hysteresis		ΔV_{IN}		500		mV
Input Leakage Current						
Logic High:						
IN_x	V_{DD} = 3.6V, V_{IH} = 2.4V	I_{IH}	-	0.1	1	µA
$LATCH_x$			-10	-19	-100	
T_{SDx}			-10	-26	-50	
Logic Low:						
IN_x	V_{DD} =3.6V, V_{IL} = 0.4V	I_{IL}	-	0.1	1	µA
$LATCH_x$			-10	-52	-125	
T_{SDx}			-10	-28	-50	
Output Characteristics						
Output Voltage: T_{SDx}:						
Logic High	V_{DD} = 3.6V, I_{TSD} = 10µA	V_{TSD_off}	2.4	V_{DD}	-	V
Logic Low	V_{DD} = 3.6V, I_{TSD} = 1mA	V_{TSD_on}	-	0	0.4	V

1.7 Switch Timing Specifications

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Switch turn on delay	$LATCH_x$ = 0V, I_{SW_off} = 0mA, t_{on}@I_{SW} = 9mA	t_{d_on}	-	0.45	2	ms
Switch turn off delay	$LATCH_x$ = 0V, I_{SW_on} = 10mA, t_{off}@I_{SW} = 0.5mA	t_{d_off}	-	0.1	1	ms
Switch turn on matching	As per Switch Turn On Delay, Any switch to any other switch	Δt_{on}	-	10	100	µs
Switch turn off matching	As per Switch Turn Off Delay, Any switch to any other switch	Δt_{off}	-	2	100	µs
Switch Capacitance	S_{xA}=S_{xB} to Gnd	C	-	60	-	pF
	S_{xA} to S_{xB}, V_{SW} (differential)=0V		-	110	-	

1.8 V_{DD} Voltage Supply Specifications

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Voltage Requirements						
Voltage operational range	-	V_{DD}	3	3.3	3.6	V
Current Specifications						
V_{DD} Current	$3.0 \le V_{DD} \le 3.6V$, All switches = OFF, All logic I/O = Open	I_{DD}	0.1	0.6	1.5	mA
	$3.0 \le V_{DD} \le 3.6V$, All switches = ON, All logic I/O = Open		0.5	2	3	mA
Under Voltage Lockout Specifications						
Thresholds	V_{DD} rising	UVLO	-	2.4	2.9	V
	V_{DD} falling		1	2.3	-	
Hysteresis			-	100	-	mV

1.9 Protection Circuitry Thermal Specifications

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Temperature Shutdown Specifications [1]						
Shutdown activation temperature	Not production tested - limits are guaranteed by design and Quality Control sampling audits	T_{TSD_on}	125	140	160	°C
Shutdown circuit hysteresis		T_{TSD_off}	10	-	25	°C

[1] *Temperature shutdown flag (T_{SDx}) will be high during normal operation and low during temperature shutdown state.*

1.10 Truth Tables

1.10.1 $CHANNEL_{1-2}$

$LATCH_{1-2}$	IN_2	IN_1	T_{SD1-2}	S_2	S_1	$LATCH_{3-4}$	IN_4	IN_3	T_{SD3-4}	S_4	S_3
0	0	0	Z [1]	OFF	OFF	x	x	x	x	x	x
0	0	1		OFF	ON	x	x	x		x	x
0	1	0		ON	OFF	x	x	x		x	x
0	1	1		ON	ON	x	x	x		x	x
1	x	x		Unchanged	Unchanged	x	x	x	x	x	x
x	x	x	0	OFF	OFF	x	x	x	x	x	x

[1] *Z = High Impedance. Because T_{SD1-2} has an internal pull-up, it should be controlled with an open-collector or open-drain type device.*

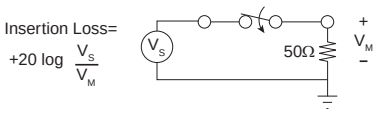
1.10.2 $CHANNEL_{3-4}$

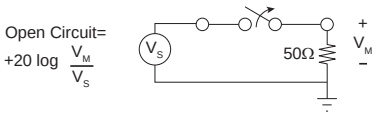
$LATCH_{1-2}$	IN_2	IN_1	T_{SD1-2}	S_2	S_1	$LATCH_{3-4}$	IN_4	IN_3	T_{SD3-4}	S_4	S_3
x	x	x	x	x	x	0	0	0	Z [1]	OFF	OFF
x	x	x		x	x	0	0	1		OFF	ON
x	x	x		x	x	0	1	0		ON	OFF
x	x	x		x	x	0	1	1		ON	ON
x	x	x		x	x	1	x	x		Unchanged	Unchanged
x	x	x	x	x	x	x	x	x	0	OFF	OFF

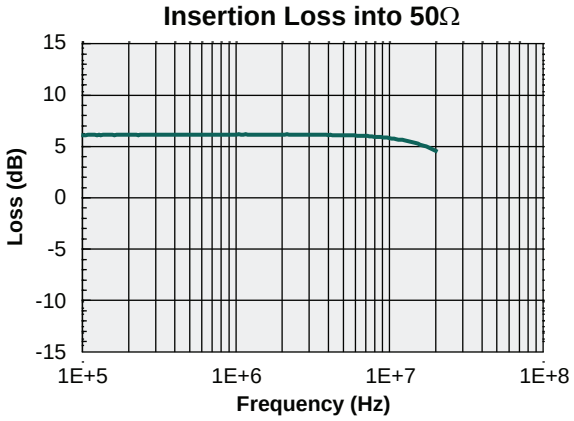
[1] *Z = High Impedance. Because T_{SD3-4} has an internal pull-up, it should be controlled with an open-collector or open-drain type device.*

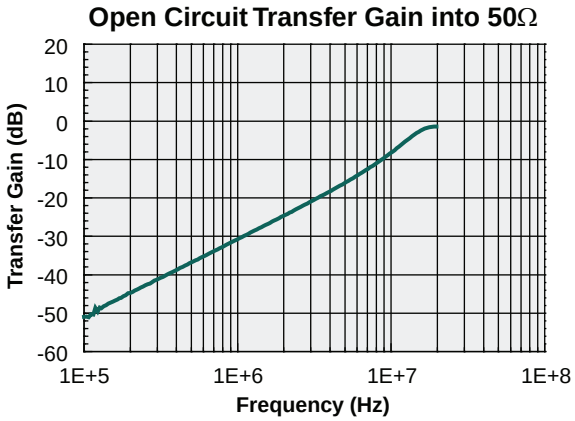
As can be seen in the two truth tables above, $CHANNEL_{1-2}$ and $CHANNEL_{3-4}$ have identical functionality yet are independent. As such, for each state of one channel there are four possible states for the other channel giving the CPC7524 a total of 16 realizable states.

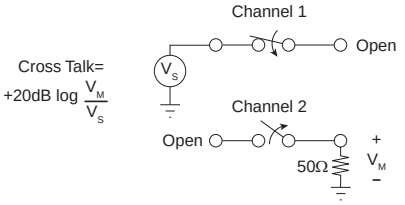
2. Performance Data

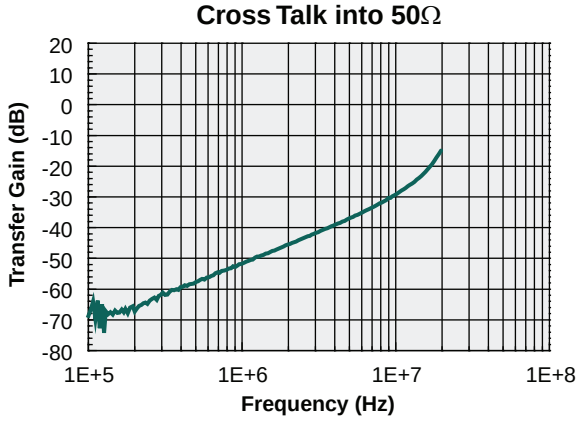












3. Functional Description

3.1 Introduction

The CPC7524 High Voltage Quad Analog Switch Array has four independent symmetrical switches providing 16 unique operating states. These operational states and the logical behavior of the device are shown in the tables given in **"Truth Tables" on page 8**. Switch organization consists of two channels each having a pair of switches. Within each channel there is a single LATCH input and a single Temperature Shutdown circuit shared by the switch pair. Other than these two shared circuits the performance of each switch within a channel is independent of the other. As there is no shared circuitry between the channels, the switches of one channel are completely independent of the other channel. Switch utilization under normal operating conditions allows the switches to be used in any combination. In designs where the switches will be required to carry high load currents or operate in higher temperature environments the thermal specifications should be reviewed.

Solid-state switch construction of the CPC7524 offers clean, bounce-free switching with simple logic input control to provide access to high voltage interfaces without the impulse noise generated by traditional electromechanical switching techniques. Simple logic input control eliminates the additional driver circuitry required by traditional techniques.

The low on-resistance (R_{ON}) symmetrical linear switches are configured as matched pairs, SW1/SW2 and SW3/SW4, for improved performance when differential access is required. Their symmetrical construction provides an additional degree of design flexibility allowing either side of the switch to be connected to the high voltage network.

Integrated into the CPC7524 switches are active current limiting and thermal shutdown mechanisms to provide protection for the electronics being connected to the high voltage network during a fault condition. High frequency positive and negative transient currents such as lightning are reduced by the current limiting circuitry. Protection from prolonged low frequency fault events and DC currents, also reduced by the current limiting circuitry, is supplemented by thermal shutdown circuits.

To protect against a high voltage fault in excess of the CPC7524's maximum voltage rating, use of an over-voltage protector is required. The protector must limit the voltage seen at the S_{xA} and S_{xB} terminals to a level below the switches maximum breakdown voltage. With proper selection of the protector, telecom applications using the CPC7524 will meet all relevant ITU, LSSGR, TIA/EIA and IEC protection requirements.

Operating from a +3.3V supply the CPC7524 has extremely low power consumption.

3.2 Under-Voltage Switch Lock-Out Circuitry

Smart logic in the CPC7524 provides for switch state control during both power up and power loss transitions to prevent undesired connections to high voltage networks. An internal detector evaluates the V_{DD} supply to determine when to de-assert the under-voltage switch lock-out circuitry with a rising V_{DD}, and when to assert the under-voltage switch lock-out circuitry with a falling V_{DD}. Any time unsatisfactory low V_{DD} conditions exist, the lock-out circuit overrides user switch control by blocking the external information at the input pins, and conditioning internal switch commands to the All-Off state. Upon restoration of V_{DD}, the switches will remain off until the $LATCH_x$ input is pulled low with proper conditioning of the IN_x inputs.

The rising V_{DD} lock-out release threshold is internally set to ensure all internal logic is properly biased and functional before accepting external switch commands from the inputs to control the switch states. For a falling V_{DD} event, the lock-out threshold is set to assure proper logic and switch behavior up to the moment the switches are forced off and external inputs are suppressed.

3.3 Switch Logic

3.3.1 Data Latch

The CPC7524 has two integrated transparent data latches. The latch-enable operation is controlled by logic input levels at the $LATCH_x$ pins. Data input to the latch is via the IN_x input pins while the outputs of the data latch are internal nodes used for state control.

When the latch enable control pin is at a logic 0 the data latch is transparent and the input control signals flow directly through the data latch to the state control circuitry. A change in input will be reflected by a change in the switch state.

Whenever the latch enable control pin is at logic 1, the data latch is active and the control data is locked. Subsequent changes to the IN_x input control pins will not result in a change to the control logic or affect the existing switch states.

The switches will remain in the state they were in when the $LATCH_x$ changes from logic 0 to logic 1, and will not respond to changes in input as long as the $LATCH_x$ is at logic 1. However, the T_{SDx} are not affected by the latch function. Since internal thermal shutdown control is not affected by the state of the latch enable input, T_{SDx} will override state control.

3.3.2 T_{SD} Pin Description

The T_{SDx} pins are bidirectional I/O structures with internal pull-ups from V_{DD}. As outputs, these pins indicate the status of the thermal shutdown circuitry for the associated channel. Typically, during normal operation, these pins will be pulled up to V_{DD}, but, under fault conditions that create excess thermal loading, the channel under duress will enter thermal shutdown and a logic low will be output at T_{SDx}.

As inputs, the T_{SDx} pins are utilized to place the channel into the All-Off state by simply pulling the input low. This is a convenient way to temporarily place the channel's switches into the off state without the need to cycle the inputs and LATCH through an off and then an on sequence.

For applications using logic devices powered from a supply voltage that differs from the CPC7524, (lower or higher than V_{DD}), IXYS Integrated Circuits Division recommends the use of an open-collector or an open-drain type output to control T_{SDx}. For lower-voltage logic control, this avoids sinking the T_{SDx} pull-up bias current to ground during normal operation when the All-Off state is not required. And for higher logic-voltage control, this prevents over-voltage biasing of the T_{SDx} input.

If T_{SDx} is forced to a logic 1 or tied to V_{DD}, the channel just ignores this input, and still enters the thermal shutdown state at high temperature. In other words, the thermal shutdown feature can not be overridden by an external pull-up on the T_{SDx} control.

3.4 Power Supplies

A +3.3V logic supply and ground are connected to the CPC7524. Switch state control is powered exclusively by the V_{DD} supply. As a result, the CPC7524 exhibits extremely low power consumption during active and idle states.

3.5 Protection

The CPC7524 provides protection for both the low voltage side circuitry it connects to high voltage networks and itself. Three separate layers of protection are interleaved within the device to protect against high-energy high-frequency transients and high-power, low-frequency fault conditions.

3.5.1 Dynamic High Frequency Current Limit

High voltage networks are ofttimes located in environments susceptible to lightning events resulting in high-frequency, high-energy transients being coupled onto the high voltage network. Low voltage circuits accessing high voltage networks through the CPC7524 are protected from these events by the dynamic high-frequency current-limit response incorporated into each switch.

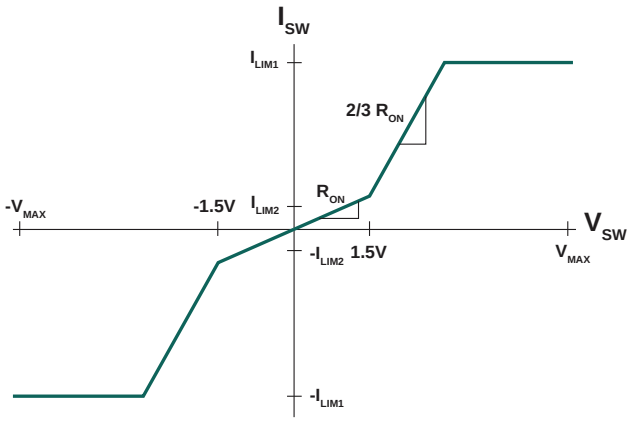
While in the ON state, the high frequency current is restricted by the CPC7524. For a GR-1089-CORE specified $\pm$1000V 10x1000µs lightning pulse with a generator source impedance of 10Ω applied to the high voltage network though a properly clamped external protector, the current seen at the CPC7524 low voltage side interface will be a pulse with a typical magnitude of 1A and a duration less than 0.5µs.

3.5.2 Low Frequency Current Limit

During high-power, low-frequency faults, current through a switch in the ON state will be constrained by the low-frequency current-limit response of the switch. As shown in **"Figure 1: Switch Low Frequency Response" on page 12** the low-frequency current-limit response is dependent on the voltage across the switch. For low levels of fault current the graph shows that the voltage across the active switch increases with increasing fault current. When the magnitude of the fault current into the CPC7524

reaches the Current Limit 1 (I_{LIM1}) threshold, the switch ceases to accept additional current causing the switch response to transition from low impedance to high impedance. This causes the voltage across the switch to increase rapidly.

Figure 1: Switch Low Frequency Response



Thermal management of each channel is necessary to minimize the internal temperature rise inside the package, created by a fault on one channel, from causing a thermal shutdown event of the other channel.

It is important to note that the low-frequency current-limit performance is dependent on a voltage clamping device on the low-voltage side sized to ensure that fault voltages do not exceed the specifications of the low-voltage circuits, and capable of redirecting currents up to the maximum level of Current Limit 1.

Note that the current-limit circuitry has a negative temperature coefficient. As a result, if the device is subjected to extended heating due to a prolonged fault condition, the current through the active switch will decrease as the device temperature rises. If the device temperature rises sufficiently, then the temperature shutdown mechanism will activate and the channel will enter the All-Off state.

3.5.3 Thermal Shutdown

The thermal-shutdown mechanism activates when the channel's die temperature reaches a minimum of 125°C, placing the channel's switch pair into the All-Off state regardless of logic input. During thermal shutdown events the T_{SDx} pin will output a logic low with a nominal 0V level. A logic high is output from the T_{SDx} pin during normal operation with a typical output level equal to V_{DD}.

If presented with a short-duration transient, such as a lightning event, the thermal-shutdown feature will typically not activate. But in an extended low-frequency event, the device temperature will rise, and the thermal shutdown mechanism will activate, forcing the channel's switches to the All-Off state. At this point the current into the active switch will drop to zero. Once the channel enters thermal shutdown, it will remain in the All-Off state until the temperature of the channel drops below the de-activation level of the thermal-shutdown circuit. This permits the circuit to autonomously return to normal operation. If the fault has not passed, current will again flow up to the value allowed by the low-frequency current-limit of the switches, and heating will resume, reactivating the thermal-shutdown mechanism. This cycle of entering and exiting the thermal-shutdown mode will continue as long as the fault condition persists. If the magnitude of the fault condition is great enough, the external over-voltage protector will activate, shunting the fault current to ground.

3.6 External Protection Elements

The CPC7524 requires only over-voltage secondary protection on the high-voltage side of the switch. Additional external protection may be required on the low-voltage side of the switch if the threshold of the high-voltage side protector exceeds the safe operation of the low-voltage side components. Because the fault current seen by the low-voltage side protector is limited by the switch's active current limit circuitry, the low-voltage side protector need not be as capable as that of the high-voltage side protector. The high-voltage side protector must limit voltage transients to levels that do not exceed the breakdown voltage or input-output isolation barrier of the CPC7524.

3.7 Thermal Design Assessment

A successful design utilizing the CPC7524 Quad High Voltage Analog Switch Array is dependent on careful consideration of the application's environment and the device's thermal constraints. For matters regarding the electrical design, this is simply a case of following the parameters provided in the preceding tables and for many this will be sufficient. However, those designers wishing to push the operational limits envelope with

higher switch current and/or higher ambient operating temperatures will need to consider the thermal performance.

Being a real physical device the CPC7524 has a finite thermal capability that when properly considered will ensure appropriate behavior and performance. Determination of the thermal constraint is easily accomplished using the following power equations:

$$P_{TOTAL} = P_{V_{DD}} + P_{SW}$$

and

$$P_{TOTAL} = \frac{\Delta T}{\Theta_{JA}}$$

Where P_{VDD} is the dissipated power drawn from the V_{DD} supply and P_{SW} is the power dissipated by the active switches. The V_{DD} power can be calculated from the "VDD Voltage Supply Specifications" on page 7 while the power dissipated by the switches is the sum of the concurrent active switches. Total switch power is the sum of the maximum current through each active switch times the On-Resistance of the switch (I_{SWx}^2 X R_{ON}).

The second equation is used to calculate the maximum ambient temperature that the device can be operated in based on the calculated total power of the previous equation. P_{TOTAL}, the value obtained in the first equation; ΔT, the junction temperature rise of the CPC7524 from ambient; and Θ_{JA}, the thermal impedance of the device package are used to determine the maximum operating ambient temperature.

Using the junction temperature rise equation $\Delta T = T_J - T_A$; the thermal impedance Θ_{JA} = 70°C/W; and a maximum junction temperature $T_{J\text{-}MAX}$ = 110°C, the equation reduces to:

$$T_{A-MAX} = T_{J-MAX} - (P_{TOTAL} \times \Theta_{JA})$$

To avoid entering thermal shutdown, the value for the maximum junction temperature was set to 110°C.

Conversely, it is possible to rework the equations to determine the maximum switch current for a maximum ambient current.

When using the individual switches of the CPC7524 within their allowable operating region, no restrictions are placed on any other switch.

4. Manufacturing Information

4.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Integrated Circuits Division classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
CPC7524B	MSL 3

4.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

4.3 Reflow Profile

Provided in the table below is the Classification Temperature (T_C) of this product and the maximum dwell time the body temperature of this device may be above (T_C - 5)ºC. The classification temperature sets the Maximum Body Temperature allowed for this device during lead-free reflow processes. For through hole devices, and any other processes, the guidelines of **J-STD-020** must be observed.

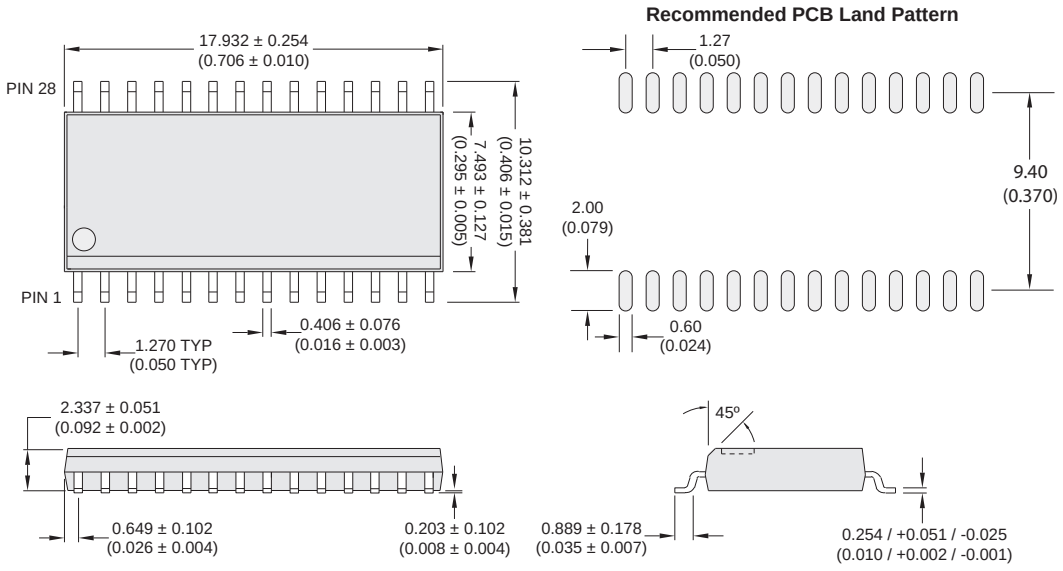
Device	Classification Temperature (T_C)	Dwell Time (t_p)	Max Reflow Cycles
CPC7524B	260°C	30 seconds	3

4.4 Board Wash

IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to flux or solvents that are Chlorine- or Fluorine-based.

4.5 Mechanical Dimensions

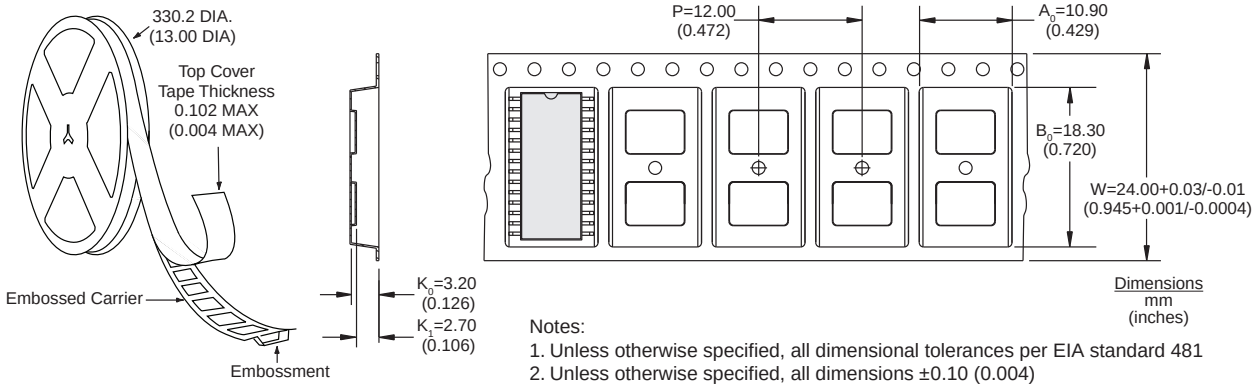
4.5.1 Package Dimensions



NOTES:
1. Coplanarity = 0.1016 (0.004) max.
2. Leadframe thickness does not include solder plating (1000 microinch maximum).

DIMENSIONS
mm
(inches)

4.5.2 Tape & Reel Specification



Dimensions
mm
(inches)

Notes:
1. Unless otherwise specified, all dimensional tolerances per EIA standard 481
2. Unless otherwise specified, all dimensions ±0.10 (0.004)

For additional information please visit www.ixysic.com

Specifications: DS-CPC7524-R02

2/28/2017

The information below supercedes any previously presented material.

For additional information please visit our website at: https://www.littelfuse.com

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