



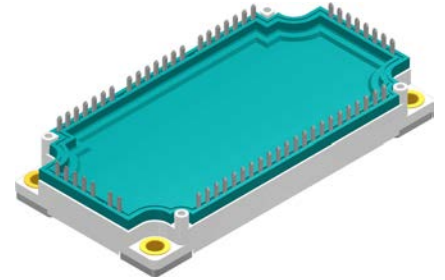
Thyristor Module

3~ Rectifier
$V_{RRM} = 1600\text{ V}$
$I_{DAV} = 450\text{ A}$
$I_{FSM} = 2400\text{ A}$

3~ Rectifier Bridge, half-controlled (high-side) + NTC

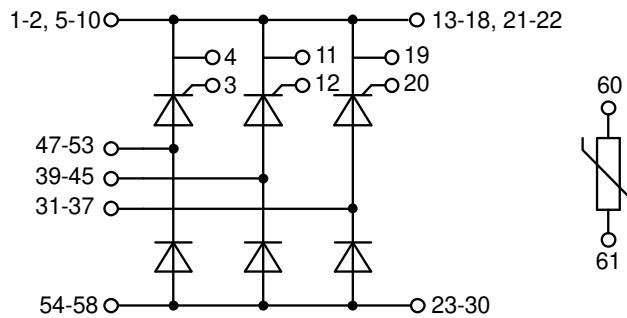
Part number

MCMA450UH1600TEH



Backside: isolated

E72873



Features / Advantages:

- Package with DCB ceramic
- Improved temperature and power cycling
- Planar passivated chips
- Very low forward voltage drop
- Very low leakage current

Applications:

- 3~ half-controlled Rectifier for drive inverters

Package: E3-Pack

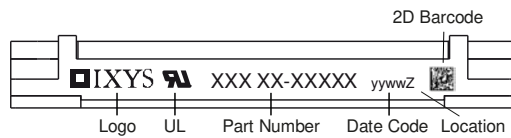
- Isolation Voltage: 4300 V~
- Industry standard outline
- RoHS compliant
- Soldering pins for PCB mounting
- Height: 17 mm
- Base plate: Copper internally DCB isolated
- Advanced power cycling
- Phase Change Material available

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Rectifier				Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit	
$V_{RSM/DSM}$	max. non-repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			1700	V	
$V_{RRM/DRM}$	max. repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			1600	V	
I_{RD}	reverse current, drain current	$V_{R/D} = 1600 V$	$T_{VJ} = 25^{\circ}C$		100	μA	
		$V_{R/D} = 1600 V$	$T_{VJ} = 150^{\circ}C$		15	mA	
V_T	forward voltage drop	$I_T = 150 A$	$T_{VJ} = 25^{\circ}C$		1,34	V	
		$I_T = 450 A$			2,10	V	
		$I_T = 150 A$	$T_{VJ} = 125^{\circ}C$		1,31	V	
		$I_T = 450 A$			2,20	V	
I_{DAV}	bridge output current	$T_C = 90^{\circ}C$ rectangular $d = 120^{\circ}$	$T_{VJ} = 150^{\circ}C$		450	A	
V_{T0}	threshold voltage	} for power loss calculation only	$T_{VJ} = 150^{\circ}C$		0,84	V	
r_T	slope resistance				3,1	m Ω	
R_{thJC}	thermal resistance junction to case				0,17	K/W	
R_{thCH}	thermal resistance case to heatsink			0,08		K/W	
P_{tot}	total power dissipation		$T_C = 25^{\circ}C$		735	W	
I_{TSM}	max. forward surge current	$t = 10 ms; (50 Hz), sine$	$T_{VJ} = 45^{\circ}C$		2,40	kA	
		$t = 8,3 ms; (60 Hz), sine$	$V_R = 0 V$		2,59	kA	
		$t = 10 ms; (50 Hz), sine$	$T_{VJ} = 150^{\circ}C$		2,04	kA	
		$t = 8,3 ms; (60 Hz), sine$	$V_R = 0 V$		2,21	kA	
I^2t	value for fusing	$t = 10 ms; (50 Hz), sine$	$T_{VJ} = 45^{\circ}C$		28,8	kA ² s	
		$t = 8,3 ms; (60 Hz), sine$	$V_R = 0 V$		27,9	kA ² s	
		$t = 10 ms; (50 Hz), sine$	$T_{VJ} = 150^{\circ}C$		20,8	kA ² s	
		$t = 8,3 ms; (60 Hz), sine$	$V_R = 0 V$		20,2	kA ² s	
C_J	junction capacitance	$V_R = 400V f = 1 MHz$	$T_{VJ} = 25^{\circ}C$		119	pF	
P_{GM}	max. gate power dissipation	$t_p = 30 \mu s$	$T_C = 150^{\circ}C$		10	W	
		$t_p = 300 \mu s$			5	W	
P_{GAV}	average gate power dissipation				0,5	W	
$(di/dt)_{cr}$	critical rate of rise of current	$T_{VJ} = 150^{\circ}C; f = 50 Hz$ repetitive, $I_T = 450 A$			150	A/ μs	
		$t_p = 200 \mu s; di_G/dt = 0,45 A/\mu s;$ $I_G = 0,45A; V_D = \frac{2}{3} V_{DRM}$ non-repet., $I_T = 150 A$			500	A/ μs	
$(dv/dt)_{cr}$	critical rate of rise of voltage	$V_D = \frac{2}{3} V_{DRM}$ $R_{GK} = \infty; method 1 (linear voltage rise)$	$T_{VJ} = 150^{\circ}C$		1000	V/ μs	
V_{GT}	gate trigger voltage	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		1,5	V	
			$T_{VJ} = -40^{\circ}C$		1,6	V	
I_{GT}	gate trigger current	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		150	mA	
			$T_{VJ} = -40^{\circ}C$		200	mA	
V_{GD}	gate non-trigger voltage	$V_D = \frac{2}{3} V_{DRM}$	$T_{VJ} = 150^{\circ}C$		0,2	V	
I_{GD}	gate non-trigger current				10	mA	
I_L	latching current	$t_p = 10 \mu s$	$T_{VJ} = 25^{\circ}C$		200	mA	
		$I_G = 0,45A; di_G/dt = 0,45 A/\mu s$					
I_H	holding current	$V_D = 6 V R_{GK} = \infty$	$T_{VJ} = 25^{\circ}C$		200	mA	
t_{gd}	gate controlled delay time	$V_D = \frac{1}{2} V_{DRM}$	$T_{VJ} = 25^{\circ}C$		2	μs	
		$I_G = 0,45A; di_G/dt = 0,45 A/\mu s$					
t_q	turn-off time	$V_R = 100 V; I_T = 150A; V_D = \frac{2}{3} V_{DRM}$ $di/dt = 10 A/\mu s; dv/dt = 20 V/\mu s; t_p = 200 \mu s$	$T_{VJ} = 125^{\circ}C$		185	μs	

Package E3-Pack		Ratings				
Symbol	Definition	Conditions	min.	typ.	max.	Unit
I_{RMS}	RMS current	per terminal			50	A
T_{VJ}	virtual junction temperature		-40		150	°C
T_{op}	operation temperature		-40		125	°C
T_{stg}	storage temperature		-40		125	°C
Weight				270		g
M_D	mounting torque		3		6	Nm
$d_{Spp/App}$	creepage distance on surface striking distance through air	terminal to terminal	6,0			mm
$d_{Spb/Apb}$		terminal to backside	12,0			mm
V_{ISOL}	isolation voltage	t = 1 second t = 1 minute	4300			V
		50/60 Hz, RMS; $I_{ISOL} \leq 1$ mA	3600			V



Part description

M = Module
 C = Thyristor (SCR)
 M = Thyristor
 A = (up to 1800V)
 450 = Current Rating [A]
 UH = 3- Rectifier Bridge, half-controlled (high-side)
 1600 = Reverse Voltage [V]
 T = Thermistor \ Temperature sensor
 EH = E3-Pack

Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	MCMA450UH1600TEH	MCMA450UH1600TEH	Box	5	521901

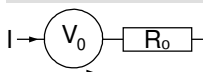
Temperature Sensor NTC

Symbol	Definition	Conditions	min.	typ.	max.	Unit
R_{25}	resistance	$T_{VJ} = 25^\circ$	4,85	5	5,15	k Ω
$B_{25/50}$	temperature coefficient			3375		K

Equivalent Circuits for Simulation

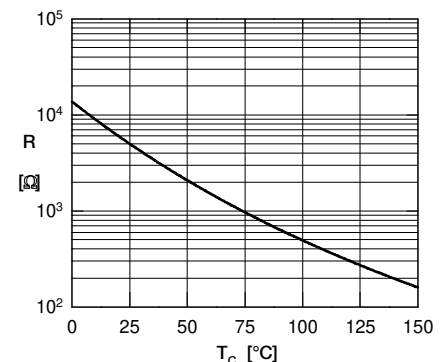
* on die level

$T_{VJ} = 150^\circ\text{C}$



Thyristor

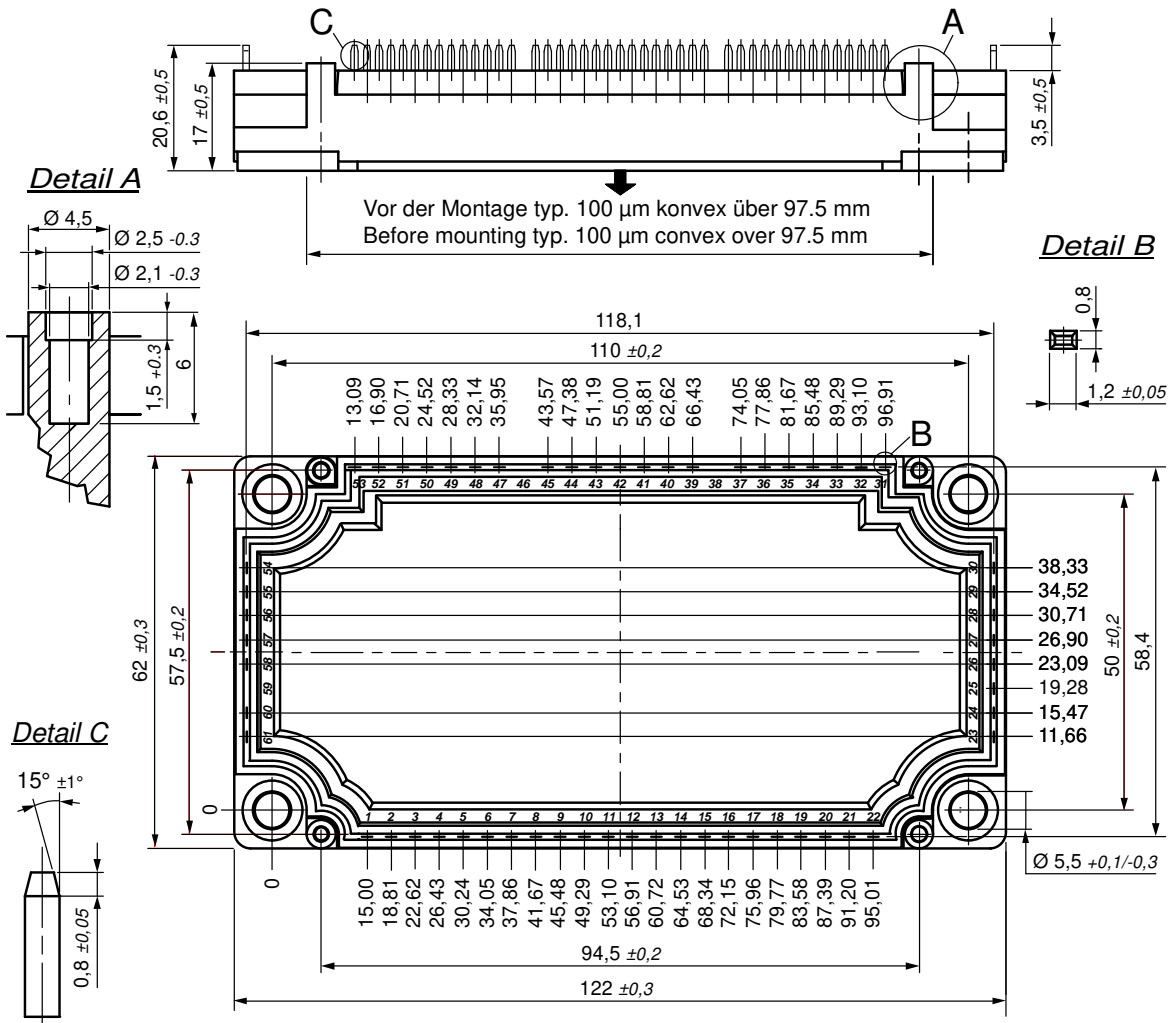
$V_{0 \max}$	threshold voltage	0,84				V
$R_{0 \max}$	slope resistance *	1,65				m Ω



Typ. NTC resistance vs. temperature



Outlines E3-Pack

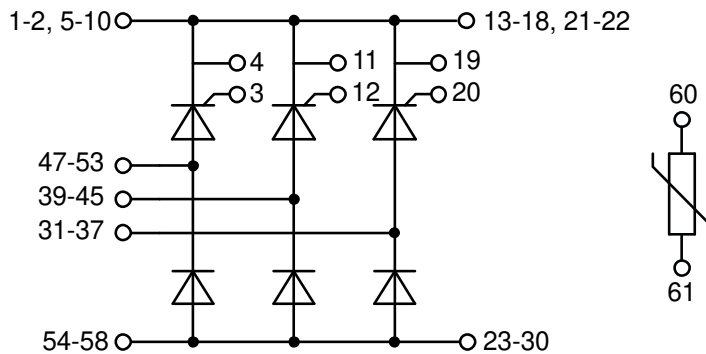


Bemerkung / Note:

- Nichttolerierete Maße nach / Measure without tolerances according DIN ISO 2768-T1-m
- PCB-Lochmuster / PCB hole pattern: **see pin position**
- Toleranz Pin-Position und PCB-Lochmuster / Tolerance of pin position and PCB hole pattern: $\oplus 0,1$
- Montageanleitung / Mounting instruction: www.ixys.com **Application note IXAN0024**

Detail A: PCB-Montage / Mounting on PCB

- Empfohlene, selbstschneidende Schraube / Recommended, self-tapping screw: **EJOT PT®** (Größe / size: **K25**)
- Max. Schraubenlänge / Max. screw length: **PCB-Dicke / thickness + 6 mm** (max. Lochtiefe / hole depth)
- Empfohlenes Drehmoment / Recommended mounting torque: **1.5 Nm**



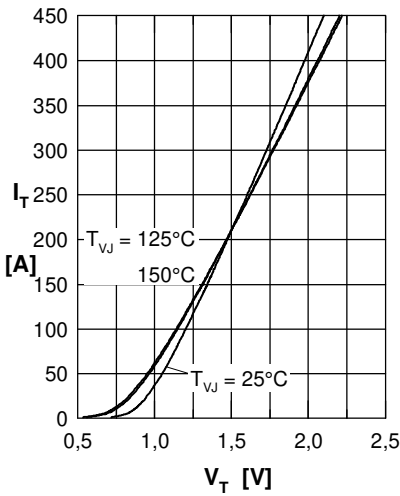
Thyristor


Fig. 1 Forward characteristics

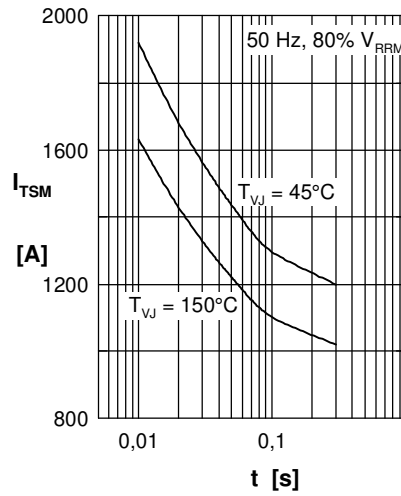
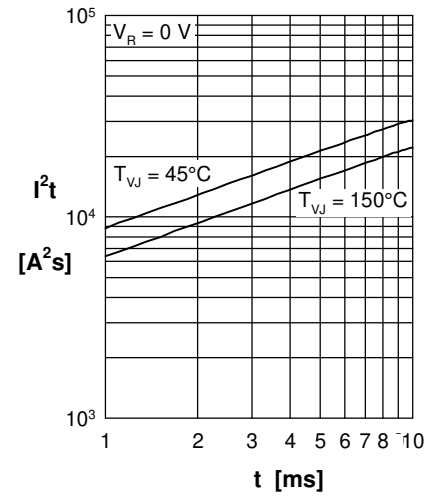
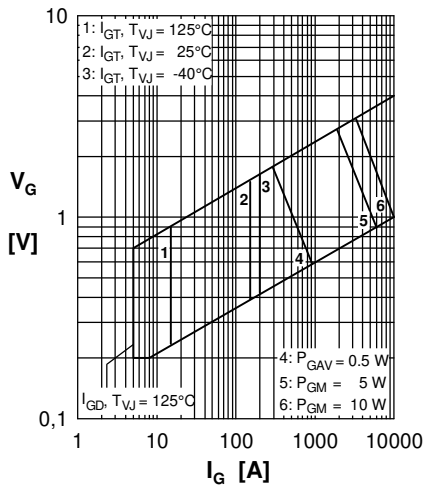

 Fig. 2 Surge overload current
 I_{TSM} : crest value, t: duration

 Fig. 3 I^2t versus time (1-10 s)


Fig. 4 Gate voltage & gate current

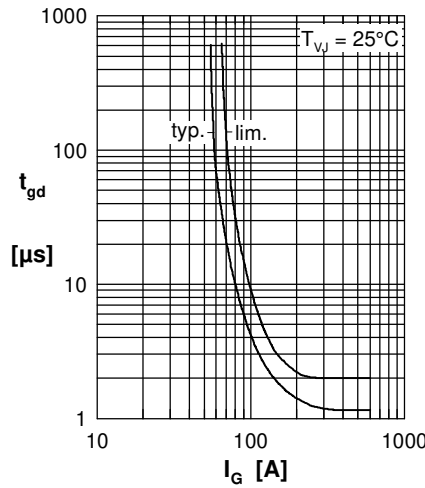
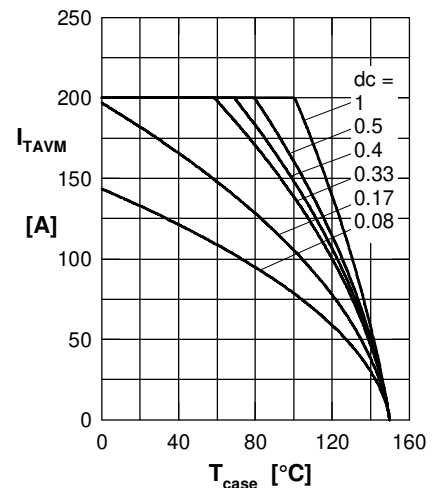

 Fig. 5 Gate controlled delay time t_{gd}


Fig. 6 Max. forward current at case temperature

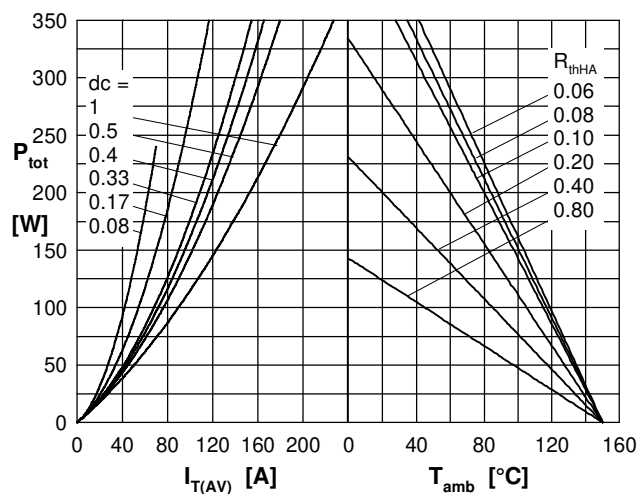
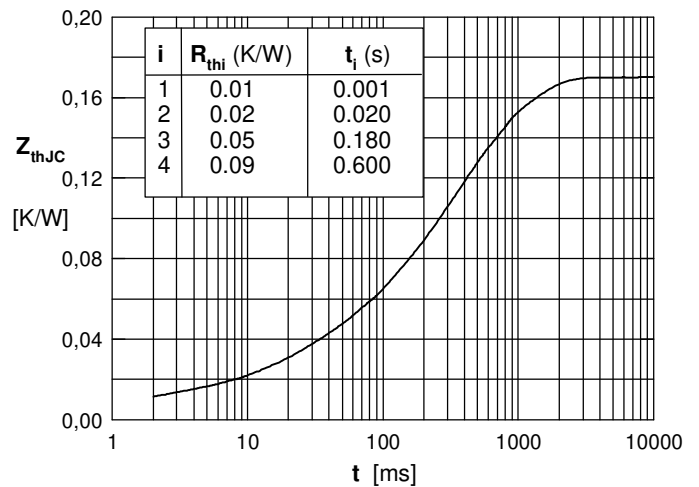

 Fig. 7a Power dissipation versus direct output current
 Fig. 7b and ambient temperature


Fig. 8 Transient thermal impedance junction to case