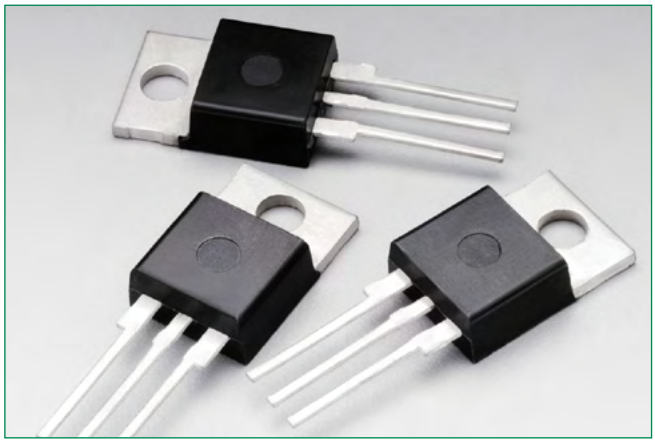
MAC8SDG, MAC8SMG, MAC8SNG

Surface Mount – 50V

RoHS Pb



Additional Information

Resources | Accessories | Samples

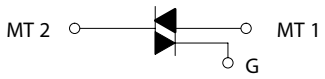
Description

Designed for industrial and consumer applications for full wave control of ac loads such as appliance controls, heater controls, motor controls, and other power switching applications. The MAC8SxG is designed for industrial and consumer applications for full wave control of ac loads such as appliance controls, heater controls, motor controls, and other power switching applications.

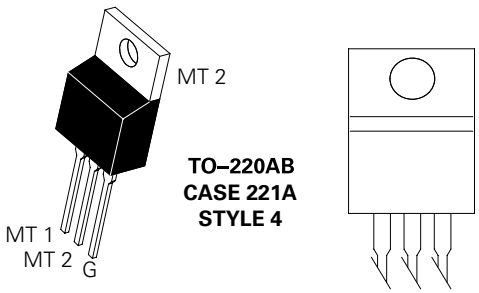
Features

- Sensitive Gate Allows Triggering by Microcontrollers and other Logic Circuits
- Uniform Gate Trigger Currents in Three Quadrants; Q1, Q2, and Q3
- High Immunity to dv/dt – 25 V/µs Minimum at 110°C
- High Commutating di/dt – 8.0 A/ms Minimum at 110°C
- Maximum Values of I_{GT}, V_{GT} and I_H Specified for Ease of Design
- On–State Current Rating of 8 Amperes RMS at 70°C
- High Surge Current Capability – 70 Amperes
- Blocking Voltage to 800 Volts
- Rugged, Economical TO–220 Package
- These Devices are Pb–Free and are RoHS Compliant

Functional Diagram



Pin Out



TO–220AB
CASE 221A
STYLE 4

Revised: TK. 04/28/22

MAC8SDG, MAC8SMG, MAC8SNG
Surface Mount – 50V

Maximum Ratings (T_J = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Note 1) (Gate Open, Sine Wave 50 to 60 Hz, T_J = 25° to 110°C)	MAC8SDG MAC8SMG MAC8SNG	V_{DRM}, V_{RRM}	400 600 800	V
On-State RMS Current (Full Cycle Sine Wave, 60 Hz, T_C = 70°C)		$I_{T\ (RMS)}$	8.0	A
Peak Non-Repetitive Surge Current (One Full Cycle Sine Wave, 60 Hz, T_J= 110°C)		I_{TSM}	70	A
Circuit Fusing Consideration (t = 8.3 ms)		I^2t	20	A^2sec
Peak Gate Power (Pulse Width ≤ 1.0 µs, T_C = 70°C)		P_{GM}	16	W
Average Gate Power (t = 8.3 ms, T_C = 70°C)		$P_{G(AV)}$	0.35	W
Operating Junction Temperature Range		T_J	-40 to +110	°C
Storage Temperature Range		T_{stg}	-40 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

Thermal Characteristics

Rating		Symbol	Value	Unit
Thermal Resistance,	Junction–to–Case (AC) Junction–to–Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.2 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds		T_L	260	°C

Electrical Characteristics - OFF (T_J = 25°C unless otherwise noted ; Electricals apply in both directions)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Repetitive Blocking Current ($V_D = V_{DRM} = V_{RRM}$; Gate Open)	T_J = 25°C	I_{DRM}, I_{RRM}	-	-	0.01	mA
	T_J = 110°C		-	-	2.0	

Electrical Characteristics - ON (T_J = 25°C unless otherwise noted; Electricals apply in both directions)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak On–State Voltage (Note 4) (I_{TM} = ±11 A)		V_{TM}	–	–	1.85	V
Gate Trigger Current (Continuous dc) (V_D = 12 V, R_L = 100 Ω)	MT2(+), G(+)	I_{GT}	–	2.0	5.0	mA
	MT2(+), G(–)		–	3.0	5.0	
	MT2(–), G(–)		–	3.0	5.0	
Holding Current (V_D = 12 V, Gate Open, Initiating Current = ±150 mA))		I_H	–	3.0	10	mA
Latching Current (V_D = 24 V, I_G = 5 mA)	MT2(+), G(+)	I_L	_	5.0	15	mA
	MT2(+), G(–)		_	10	20	
	MT2(–), G(–)		_	5.0	15	
Gate Trigger Voltage (V_D = 12 V, R_L = 100 Ω)	MT2(+), G(+)	V_{GT}	0.45	0.62	1.5	V
	MT2(+), G(–)		0.45	0.60	1.5	
	MT2(–), G(–)		0.45	0.65	1.5	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Indicates Pulse Test: Pulse Width ≤ 2.0 ms, Duty Cycle ≤ 2%.

Revised: TK. 04/28/22

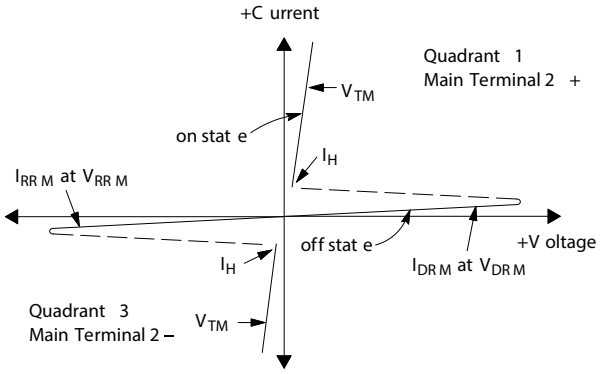
MAC8SDG, MAC8SMG, MAC8SNG
Surface Mount – 50V

Dynamic Characteristics

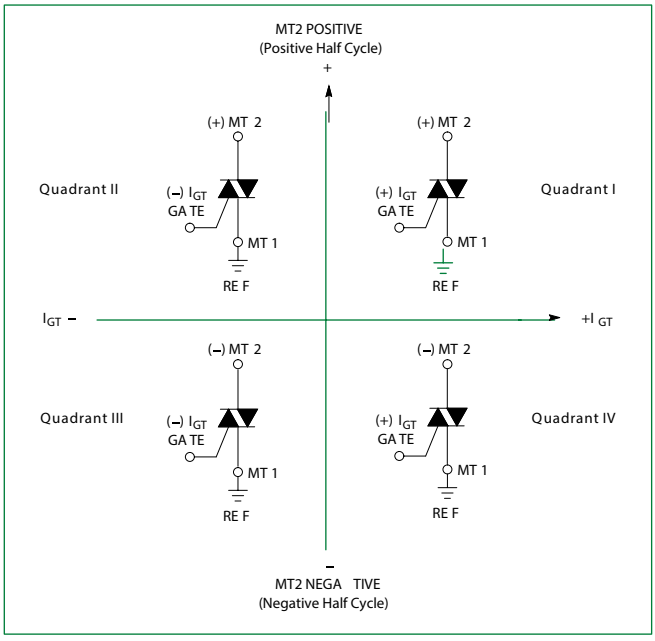
Characteristic	Symbol	Min	Typ	Max	Unit
Rate of Change of Commutating Current See Figure 10. (V_D = 400 V, I_{TM} = 3.5 A, Commutating dv/dt = 10 V/µs,Gate Open, T_J = 110°C, f = 500 Hz, Snubber), C_S= 0.01 µF, R_S =15 Ω	$di/dt_{(C)}$	8.0	10	–	A/ms
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, R_{GK} = 510 Ω, T_J = 110°C)	dV/dt	25	75	–	V/µs

Voltage Current Characteristic of SCR

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On State Voltage
I_H	Holding Current



Quadrant Definitions for a Triac



All polarities are referenced to MT1.
With in–phase signals (using standard AC lines) quadrants I and III are used

MAC8SDG, MAC8SMG, MAC8SNG

Surface Mount – 50V

Figure 1. RMS Current Derating

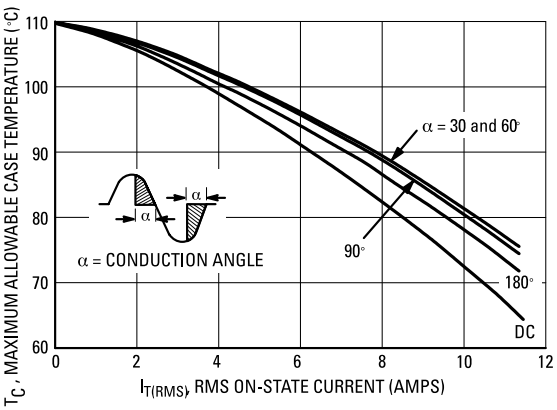


Figure 2. Maximum On-State Power Dissipation

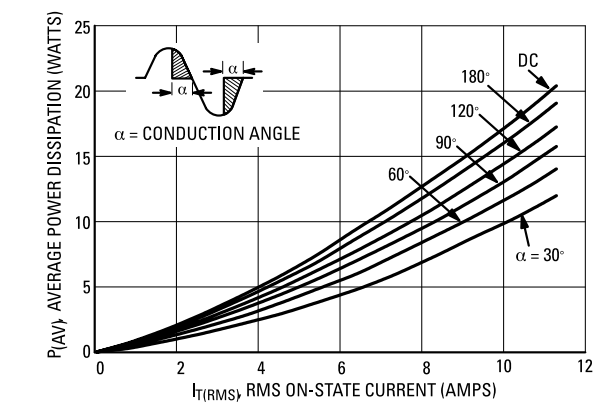


Figure 3. On–State Characteristics

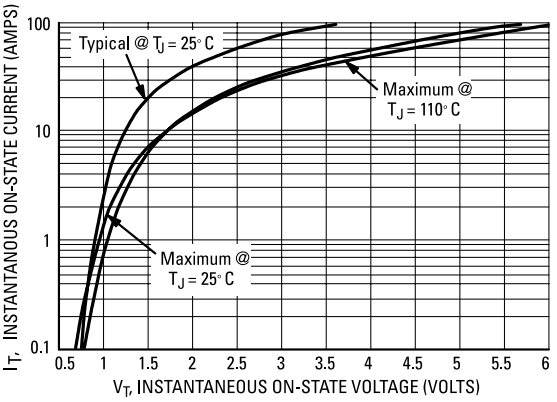


Figure 4. Transient Thermal Response

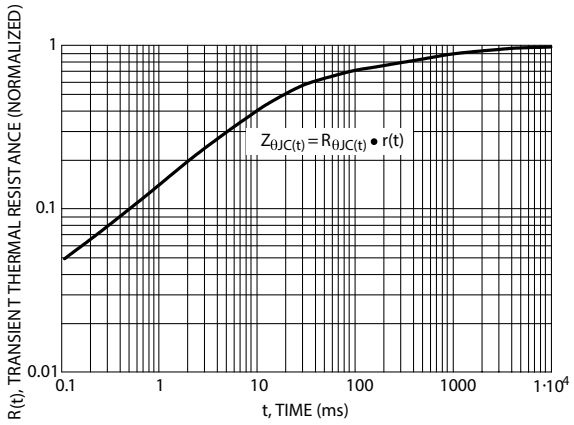


Figure 5. Typical Holding Current Vs. Junction Temperature

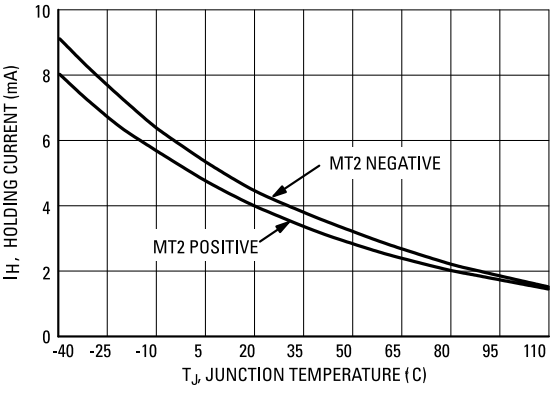
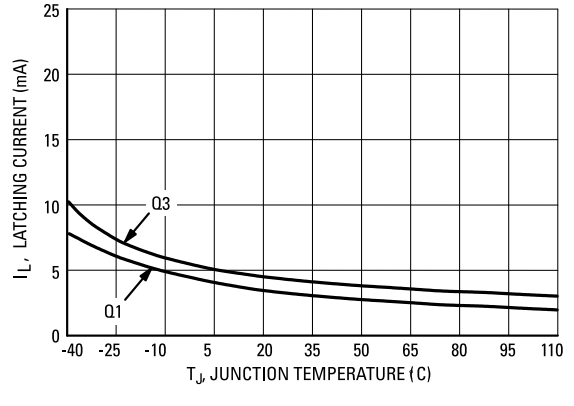


Figure 6. Typical Latching Current Vs. Junction Temperature



Revised: TK. 04/28/22

MAC8SDG, MAC8SMG, MAC8SNG

Surface Mount – 50V

Figure 7. Typical Gate Trigger Current Vs. Junction Temperature

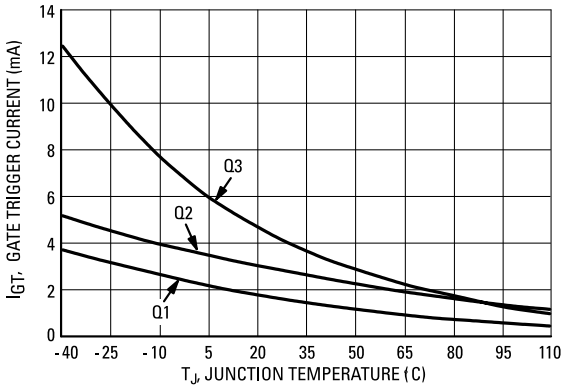


Figure 8. Typical Gate Trigger Voltage Vs. Junction Temperature

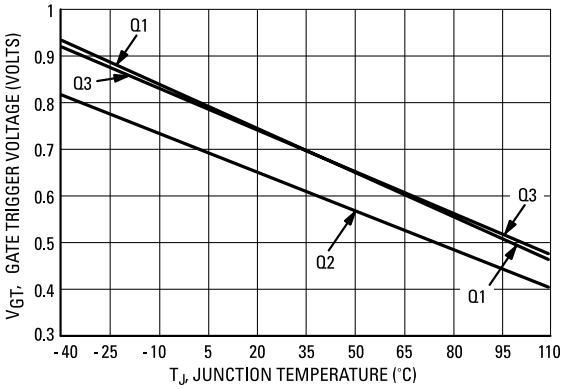


Figure 9. Typical Exponential Static dv/dt Vs. Gate–MT1 Resistance, MT2(+)

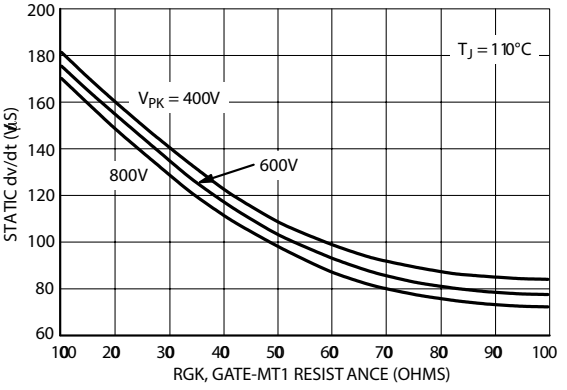


Figure 10. Typical Exponential Static dv/dt Versus Peak Voltage, MT2(+)

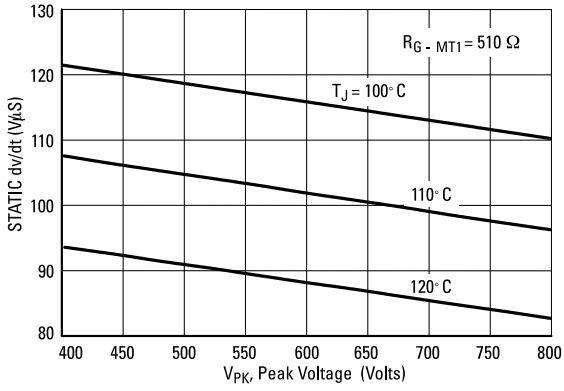


Figure 11. Typical Exponential Static dv/dt Vs. Junction Temperature, MT2(+)

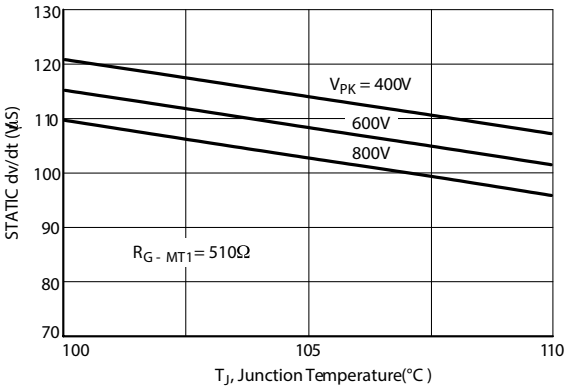
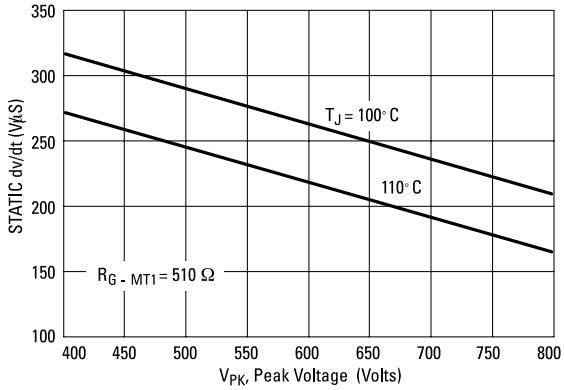


Figure 12. Typical Exponential Static dv/dt Vs. Peak Voltage, MT2(–)



Revised: TK. 04/28/22

MAC8SDG, MAC8SMG, MAC8SNG
Surface Mount – 50V

Figure 13. Typical Exponential Static dv/dt Versus Junction Temperature, MT2(–)

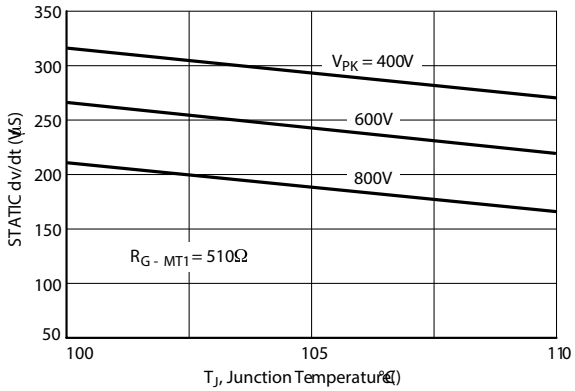


Figure 14. Typical Exponential Static dv/dt Versus Gate–MT1 Resistance, MT2(–)

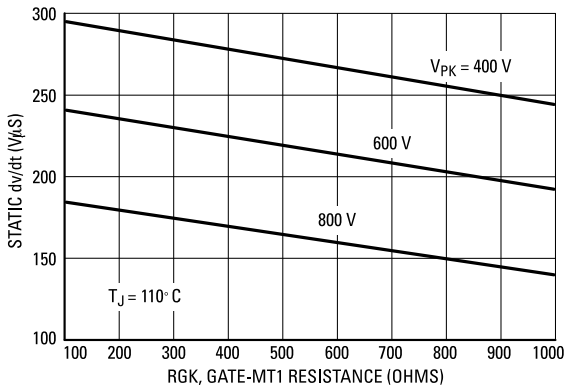


Figure 15. Critical Rate of Rise of Commutating Voltage

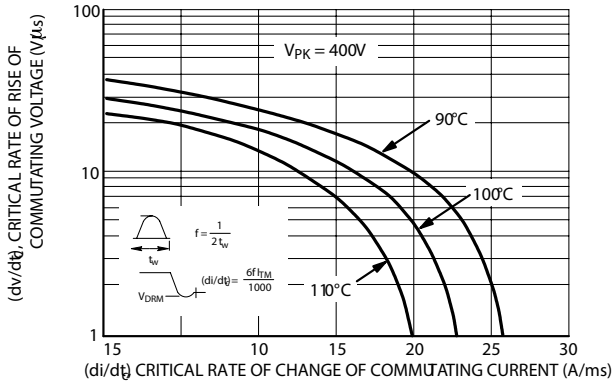
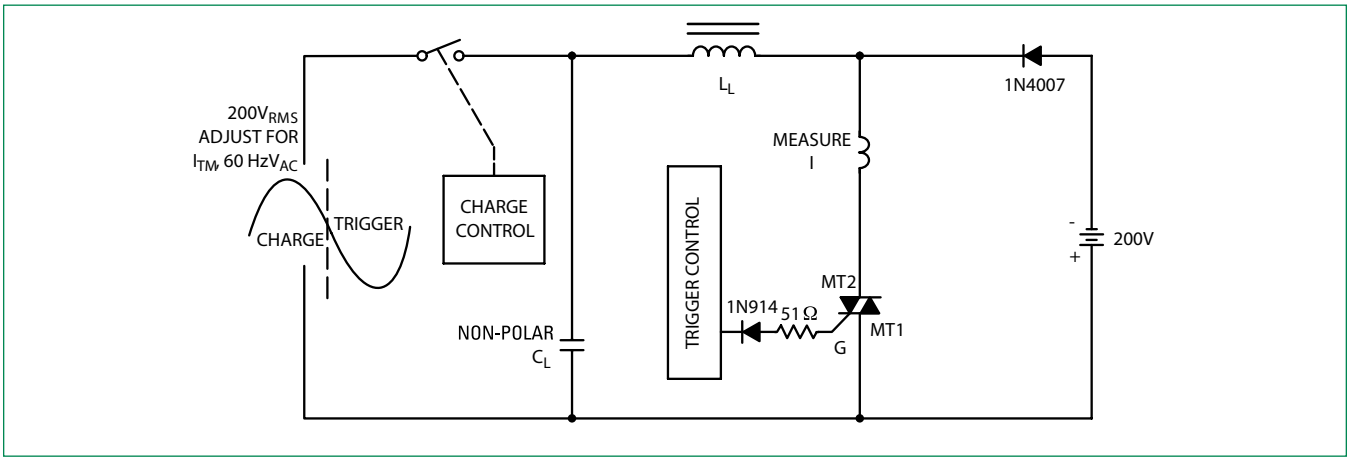


Figure 16. Simplified Test Circuit to Measure the Critical Rate of Rise of Commutating Current (di/dt)



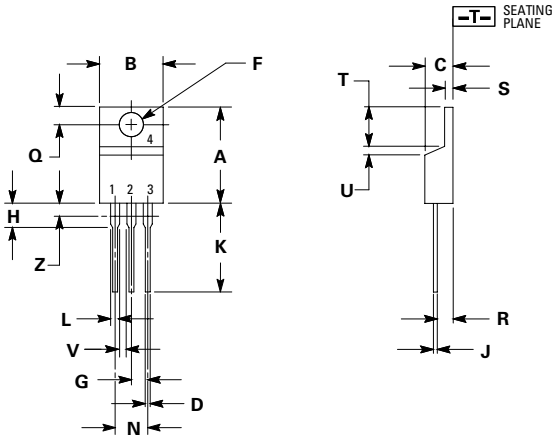
Note: Component values are for verification of rated (di/dt)c. See AN1048 for additional information

Revised: TK. 04/28/22

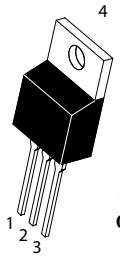
MAC8SDG, MAC8SMG, MAC8SNG

Surface Mount – 50V

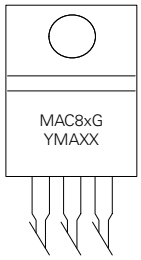
Dimensions



Part Marking System



TO–220AB
CASE 221A
STYLE 12



x =D, M, or N
Y =Year
M =Month
A =Assembly Site
XX =Lot Serial Code
G =Pb-Free Package

Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.590	0.620	14.99	15.75
B	0.380	0.420	9.65	10.67
C	0.178	0.188	4.52	4.78
D	0.025	0.035	0.64	0.89
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.41	2.67
H	0.110	0.130	2.79	3.30
J	0.018	0.024	0.46	0.61
K	0.540	0.575	13.72	14.61
L	0.060	0.075	1.52	1.91
N	0.195	0.205	4.95	5.21
Q	0.105	0.115	2.67	2.92
R	0.085	0.095	2.16	2.41
S	0.045	0.060	1.14	1.52
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

1. Dimensioning and tolerancing per ansi y14.5m, 1982.
2. Controlling dimension: inch.
3. Dimension z defines a zone where all body and lead irregularities are allowed.

Pin Assignment	
1	Main Terminal 1
2	Main Terminal 2
3	Gate
4	Main Terminal 2

Ordering Information

Device	Package	Shipping
MAC8SDG	TO-220AB (Pb-Free)	1000 Units / Box
MAC8SMG		
MAC8SNG		

Revised: TK. 04/28/22