

Thyristor Module

$$V_{RRM} = 1600 \text{ V}$$

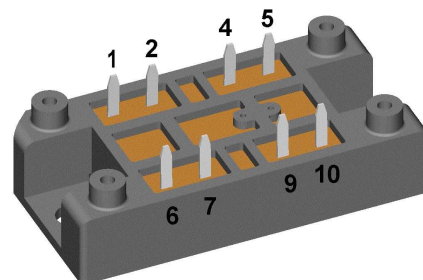
$$I_{TAV} = 27 \text{ A}$$

$$V_T = 1.28 \text{ V}$$

AC Controlling
 2~ full-controlled

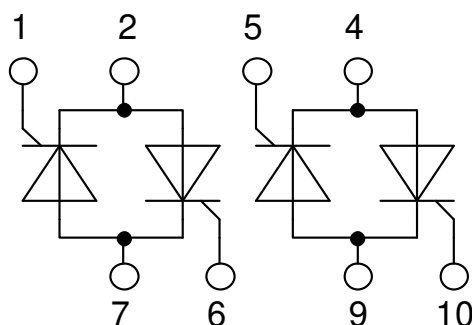
Part number

VW2x60-16io1



Backside: isolated

 E72873



Features / Advantages:

- Thyristor for line frequency
- Planar passivated chip
- Long-term stability
- Direct Copper Bonded Al₂O₃-ceramic

Applications:

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

Package: V1-A-Pack

- Isolation Voltage: 3600 V~
- Industry standard outline
- RoHS compliant
- Soldering pins for PCB mounting
- Height: 17 mm
- Base plate: DCB ceramic
- Reduced weight
- Advanced power cycling

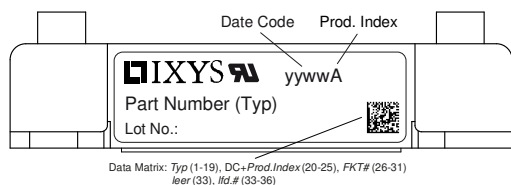
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Rectifier				Ratings			
Symbol	Definition	Conditions		min.	typ.	max.	Unit
$V_{RSM/DSM}$	max. non-repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}\text{C}$				1700	V
$V_{RRM/DRM}$	max. repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}\text{C}$				1600	V
$I_{R/D}$	reverse current, drain current	$V_{R/D} = 1600\text{ V}$	$T_{VJ} = 25^{\circ}\text{C}$			100	μA
		$V_{R/D} = 1600\text{ V}$	$T_{VJ} = 125^{\circ}\text{C}$			5	mA
V_T	forward voltage drop	$I_T = 40\text{ A}$	$T_{VJ} = 25^{\circ}\text{C}$			1.25	V
		$I_T = 80\text{ A}$				1.65	V
		$I_T = 40\text{ A}$	$T_{VJ} = 125^{\circ}\text{C}$			1.28	V
		$I_T = 80\text{ A}$				1.75	V
I_{TAV}	average forward current	$T_C = 85^{\circ}\text{C}$	$T_{VJ} = -40^{\circ}\text{C}$			27	A
I_{RMS}	RMS forward current per phase	180° sine				60	A
V_{T0}	threshold voltage	} for power loss calculation only	$T_{VJ} = -40^{\circ}\text{C}$			0.85	V
r_T	slope resistance					11	m Ω
R_{thJC}	thermal resistance junction to case					0.92	K/W
R_{thCH}	thermal resistance case to heatsink				0.3		K/W
P_{tot}	total power dissipation		$T_C = 25^{\circ}\text{C}$			110	W
I_{TSM}	max. forward surge current	$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}\text{C}$			520	A
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$			560	A
		$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = -40^{\circ}\text{C}$			440	A
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$			475	A
I^2t	value for fusing	$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}\text{C}$			1.35	kA ² s
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$			1.31	kA ² s
		$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = -40^{\circ}\text{C}$			970	A ² s
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$			940	A ² s
C_J	junction capacitance	$V_R = 400\text{ V}$ $f = 1\text{ MHz}$	$T_{VJ} = 25^{\circ}\text{C}$		64		pF
P_{GM}	max. gate power dissipation	$t_p = 30\text{ }\mu\text{s}$	$T_C = -40^{\circ}\text{C}$			10	W
		$t_p = 300\text{ }\mu\text{s}$				5	W
P_{GAV}	average gate power dissipation					0.5	W
$(di/dt)_{cr}$	critical rate of rise of current	$T_{VJ} = 125^{\circ}\text{C}; f = 50\text{ Hz}$ repetitive, $I_T = 45\text{ A}$				100	A/ μs
		$t_p = 200\text{ }\mu\text{s}; di_G/dt = 0.45\text{ A}/\mu\text{s};$ $I_G = 0.45\text{ A}; V = \frac{2}{3} V_{DRM}$ non-repet., $I_T = 27\text{ A}$				500	A/ μs
$(dv/dt)_{cr}$	critical rate of rise of voltage	$V = \frac{2}{3} V_{DRM}$	$T_{VJ} = 125^{\circ}\text{C}$			1000	V/ μs
		$R_{GK} = \infty$; method 1 (linear voltage rise)					
V_{GT}	gate trigger voltage	$V_D = 6\text{ V}$	$T_{VJ} = 25^{\circ}\text{C}$			1.5	V
			$T_{VJ} = -40^{\circ}\text{C}$			1.6	V
I_{GT}	gate trigger current	$V_D = 6\text{ V}$	$T_{VJ} = 25^{\circ}\text{C}$			100	mA
			$T_{VJ} = -40^{\circ}\text{C}$			200	mA
V_{GD}	gate non-trigger voltage	$V_D = \frac{2}{3} V_{DRM}$	$T_{VJ} = 125^{\circ}\text{C}$			0.2	V
I_{GD}	gate non-trigger current					5	mA
I_L	latching current	$t_p = 10\text{ }\mu\text{s}$	$T_{VJ} = 25^{\circ}\text{C}$			450	mA
		$I_G = 0.45\text{ A}; di_G/dt = 0.45\text{ A}/\mu\text{s}$					
I_H	holding current	$V_D = 6\text{ V}$ $R_{GK} = \infty$	$T_{VJ} = 25^{\circ}\text{C}$			200	mA
t_{gd}	gate controlled delay time	$V_D = \frac{1}{2} V_{DRM}$	$T_{VJ} = 25^{\circ}\text{C}$			2	μs
		$I_G = 0.45\text{ A}; di_G/dt = 0.45\text{ A}/\mu\text{s}$					
t_q	turn-off time	$V_R = 100\text{ V}; I_T = 20\text{ A}; V = \frac{2}{3} V_{DRM}$ $T_{VJ} = -65^{\circ}\text{C}$ $di/dt = 10\text{ A}/\mu\text{s}$ $dv/dt = 15\text{ V}/\mu\text{s}$ $t_p = 200\text{ }\mu\text{s}$			150		μs

Package V1-A-Pack				Ratings			
Symbol	Definition	Conditions		min.	typ.	max.	Unit
I _{RMS}	RMS current	per terminal				100	A
T _{VJ}	virtual junction temperature			-40		-40	°C
T _{op}	operation temperature			-40		-65	°C
T _{stg}	storage temperature			-40		125	°C
Weight					37		g
M _D	mounting torque			2		2.5	Nm
d _{Spp/App}	creepage distance on surface striking distance through air	terminal to terminal		6.0			mm
d _{Spb/Apb}		terminal to backside		12.0			mm
V _{ISOL}	isolation voltage	t = 1 second		3600			V
		t = 1 minute		3000			V
50/60 Hz, RMS; I _{ISOL} ≤ 1 mA							



Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	VW2x60-16io1	VW2x60-16io1	Blister	24	517894

Equivalent Circuits for Simulation

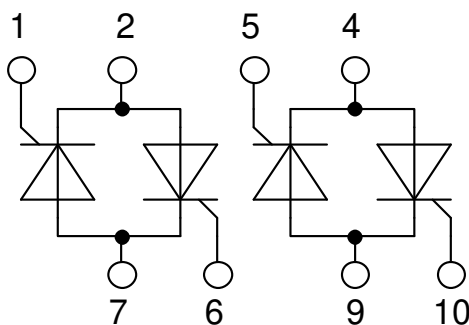
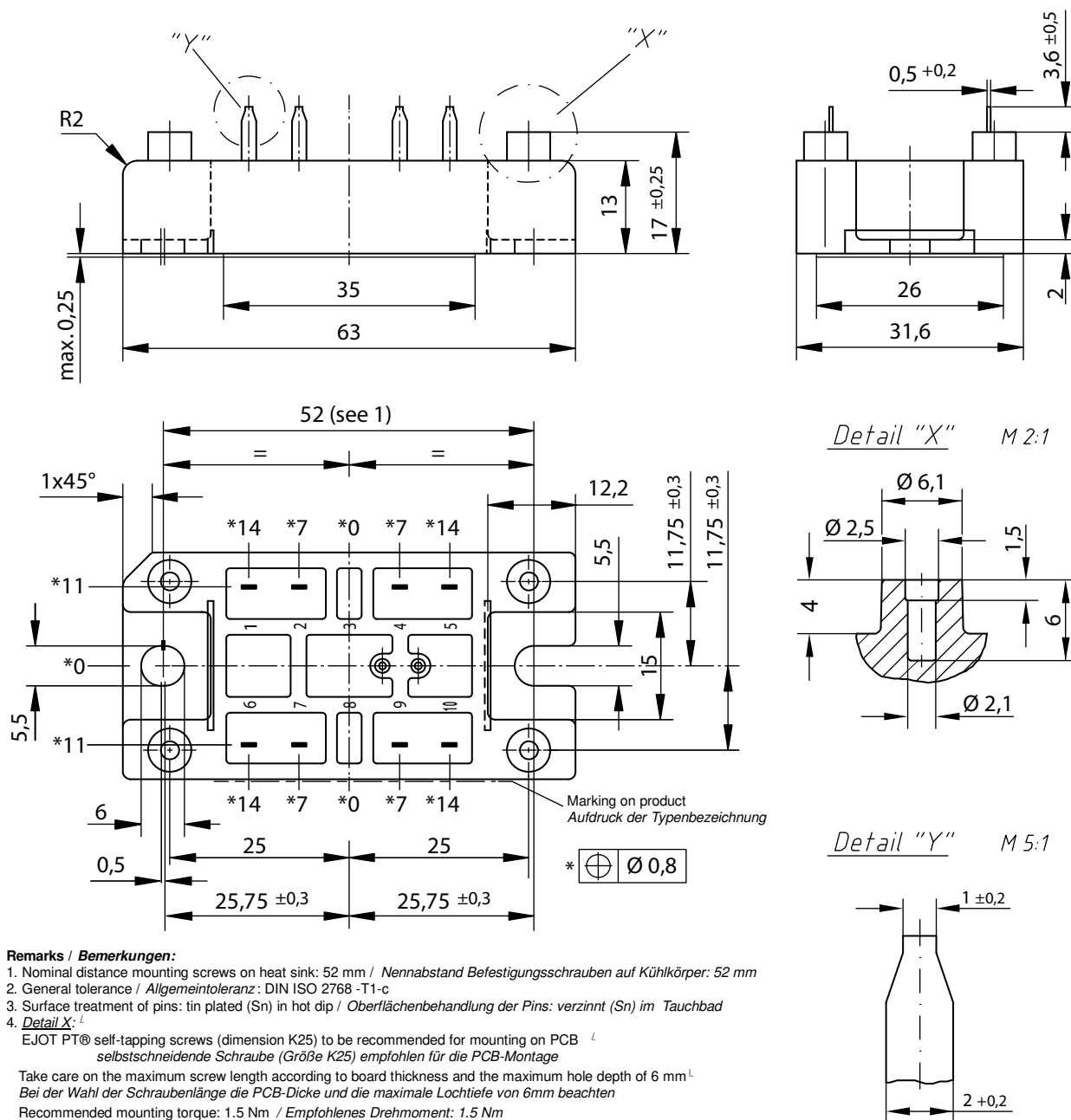
* on die level

$T_{VJ} = -40$ °C



Thyristor

$V_{0\ max}$	threshold voltage	0.85	V
$R_{0\ max}$	slope resistance *	8.5	mΩ

Outlines V1-A-Pack


Thyristor

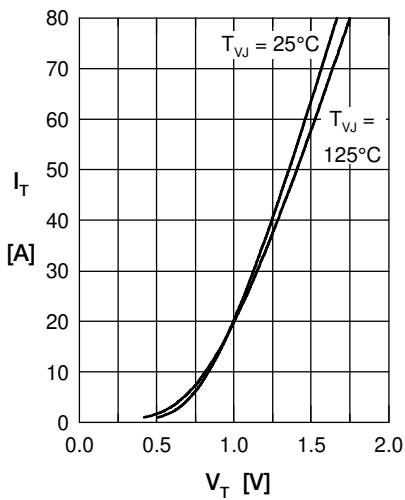


Fig. 1 Forward characteristics

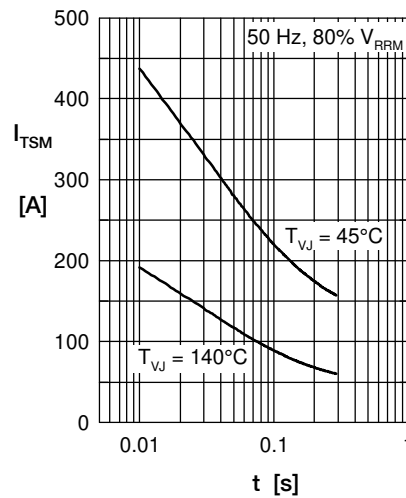


Fig. 2 Surge overload current
 I_{TSM} : crest value, t : duration

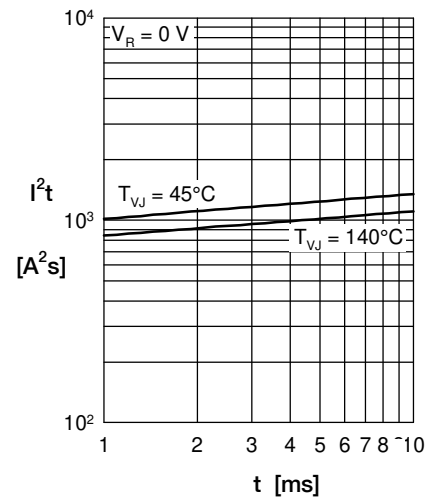


Fig. 3 I^2t versus time (1-10 s)

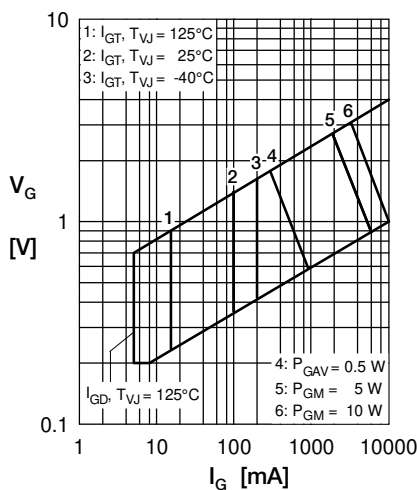


Fig. 4 Gate voltage & gate current

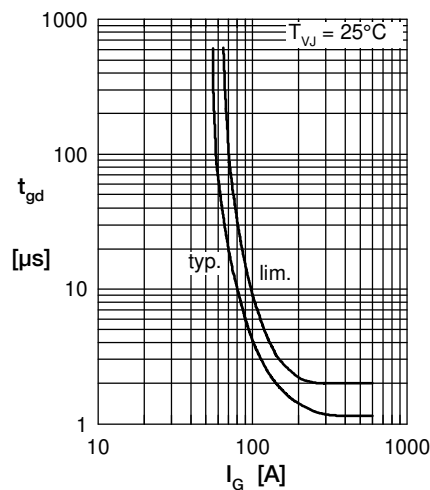


Fig. 5 Gate controlled delay time t_{gd}

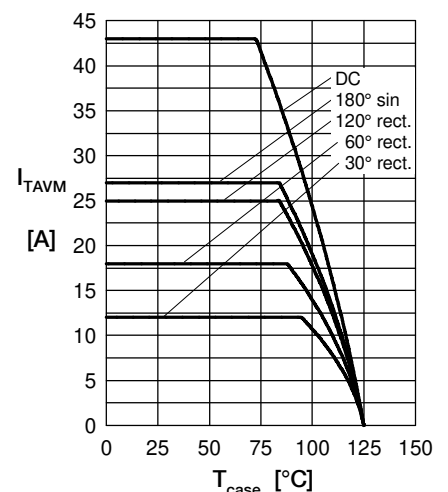


Fig. 6 Max. forward current at case temperature

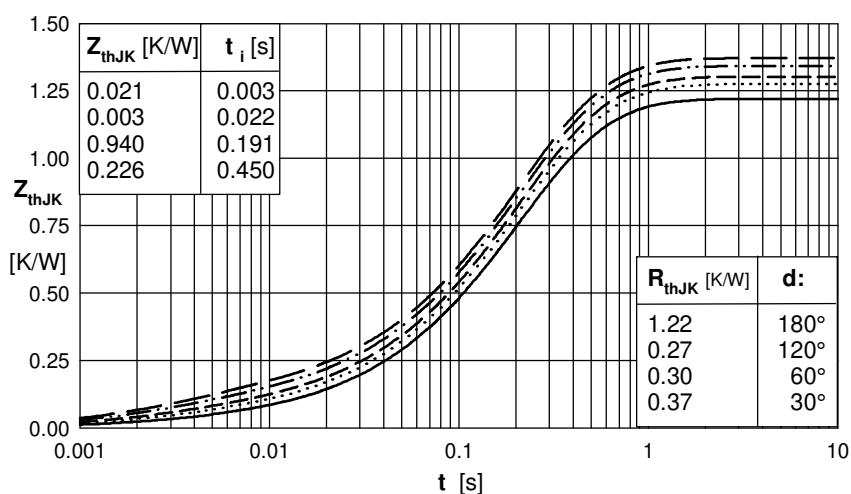


Fig. 7 Transient thermal impedance junction to heatsink (per thyristor)

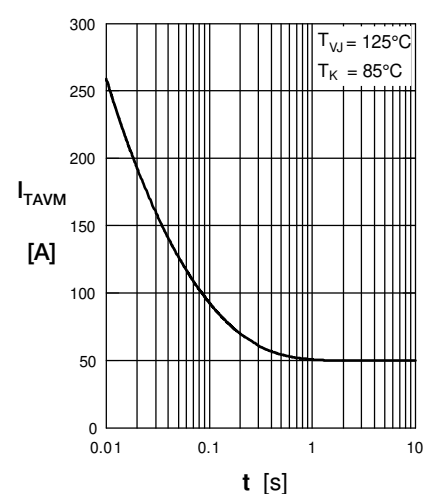


Fig. 8 Rated RMS current vs. time
(360° conduction)

Rectifier

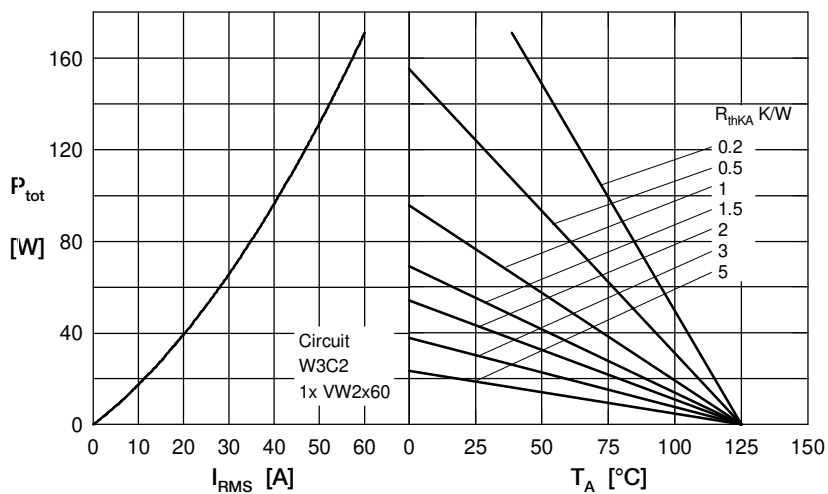


Fig. 9 Load current capability for two phase AC controller

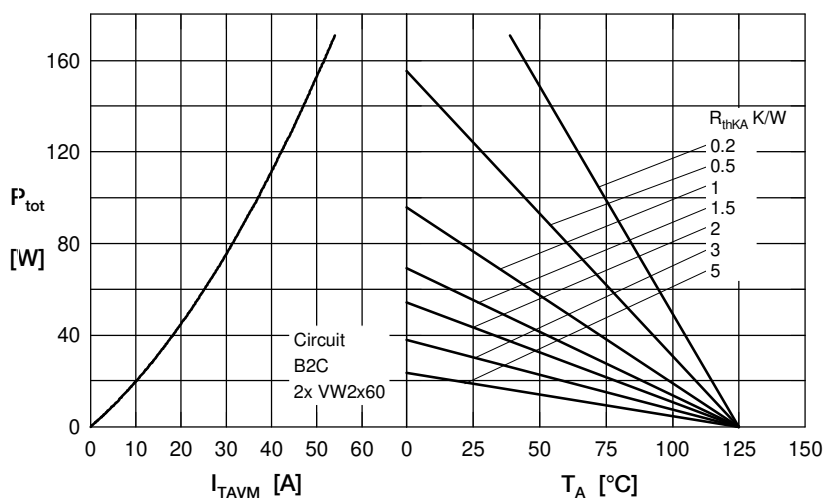


Fig. 10 Power dissipation vs. direct output current and ambient temperature
cyclo converter, four quadrant operation