IXYS

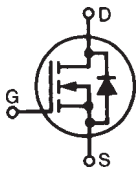
HiPerFET™ Power MOSFETs ISOPLUS247™, Q-Class

(Electrically Isolated Backside)

N-Channel Enhancement Mode
Avalanche Rated, Low Q_g, High dv/dt

	V_{DSS}	I_{D25}	$R_{DS(on)}$
IXFR 44N50Q	500 V	34 A	120 mΩ
IXFR 48N50Q	500 V	40 A	110 mΩ

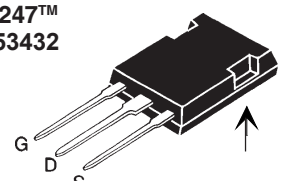
$t_{rr} \leq 250$ ns



Symbol	Test Conditions		Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C		500	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ		500	V
V_{GS}	Continuous		±20	V
V_{GSM}	Transient		±30	V
I_{D25}	T_C = 25°C	44N50Q	34	A
		48N50Q	40	A
I_{DM}	T_C = 25°C, Note 1	44N50Q	176	A
		48N50Q	192	A
I_{AR}	T_C = 25°C	44N50Q	44	A
		48N50Q	48	A
E_{AR}	T_C = 25°C		60	mJ
E_{AS}	T_C = 25°C		2.5	J
dv/dt	$I_S \leq I_{DM}$, di/dt ≤ 100 A/µs, $V_{DD} \leq V_{DSS}$ $T_J \leq$ 150°C, R_G = 2 Ω		15	V/ns
P_D	T_C = 25°C		310	W
T_J			-55 ... +150	°C
T_{JM}			150	°C
T_{stg}			-55 ... +150	°C
T_L	1.6 mm (0.063 in.) from case for 10 s		300	°C
V_{ISOL}	50/60 Hz, RMS t = 1 min		2500	V~
Weight			5	g

Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
V_{DSS}	V_{GS} = 0 V, I_D = 250µA		500			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 4mA		2.0		4.0	V
I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0				±100	nA
I_{DSS}	$V_{DS} = V_{DSS}$ V_{GS} = 0 V	 T_J = 125°C			100 2	µA mA
$R_{DS(on)}$	V_{GS} = 10 V, $I_D = I_T$ Notes 2, 3	44N50Q 48N50Q			120 110	mΩ mΩ

ISOPLUS247™
E153432



Isolated backside*

G = Gate D = Drain
S = Source

* Patent pending

Features
- Silicon chip on Direct-Copper-Bond substrate
  - High power dissipation
  - Isolated mounting surface
  - 2500V electrical isolation
- Low drain to tab capacitance(<30pF)
- IXYS advanced low Q_g process
- Rugged polysilicon gate cell structure
- Rated for Unclamped Inductive Load Switching (UIS)
- Fast intrinsic diode

Applications
- DC-DC converters
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- AC motor control

Advantages
- Easy assembly
- Space savings
- High power density

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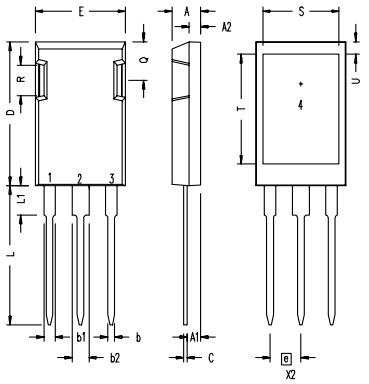
Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
g_{fs}	V_{DS} = 10 V; I_D = I_T	Notes 2, 3	30	42		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz			7000		pF
C_{oss}				960		pF
C_{rss}				230		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS}, I_D = I_T			33		ns
t_r	R_G = 1 Ω (External), Notes 2, 3			22		ns
$t_{d(off)}$				75		ns
t_f				10		ns
$Q_{g(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS}, I_D = I_T Notes 2, 3			190		nC
Q_{gs}				40		nC
Q_{gd}				86		nC
R_{thJC}					0.40	K/W
R_{thCK}				0.15		K/W

Source-Drain Diode — Characteristic Values (T_J = 25°C, unless otherwise specified)

Symbol	Test Conditions	min.	typ.	max.	
I_S	V_{GS} = 0 V			48	A
I_{SM}	Repetitive; Note 1			192	A
V_{SD}	I_F = I_T, V_{GS} = 0 V, Notes 2, 3			1.5	V
t_{rr}	I_F = 25A,-di/dt = 100 A/µs, V_R = 100 V			250	ns
Q_{RM}			1.0		µC
I_{RM}			10		A

Note: 1. Pulse width limited by T_{JM}
2. Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %
3. IXFR44N50Q: I_T = 22 A
IXFR48N50Q: I_T = 24 A

ISOPLUS 247 OUTLINE



1 Gate, 2 Drain (Collector)
3 Source (Emitter)
4 no connection

Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.83	5.21	.190	.205
A_1	2.29	2.54	.090	.100
A_2	1.91	2.16	.075	.085
b	1.14	1.40	.045	.055
b_1	1.91	2.13	.075	.084
b_2	2.92	3.12	.115	.123
C	0.61	0.80	.024	.031
D	20.80	21.34	.819	.840
E	15.75	16.13	.620	.635
e	5.45 BSC		.215 BSC	
L	19.81	20.32	.780	.800
L1	3.81	4.32	.150	.170
Q	5.59	6.20	.220	.244
R	4.32	4.83	.170	.190

IXYS reserves the right to change limits, test conditions, and dimensions.
IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,881,106 5,017,508 5,049,961 5,187,117 5,486,715 6,306,728B1 6,259,123B1 6,306,728B1 4,850,072 4,931,844 5,034,796 5,063,307 5,237,481 5,381,025 6,404,065B1 6,162,665 6,534,343

Fig. 1. Output Characteristics @ 25 Deg. C

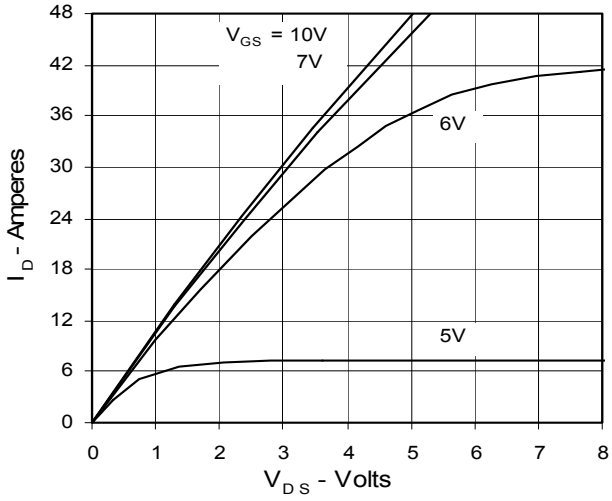


Fig. 2. Extended Output Characteristics @ 25 deg. C

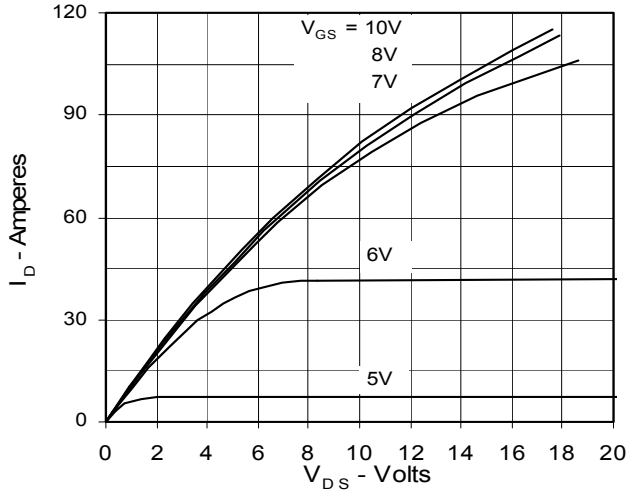


Fig. 3. Output Characteristics @ 125 Deg. C

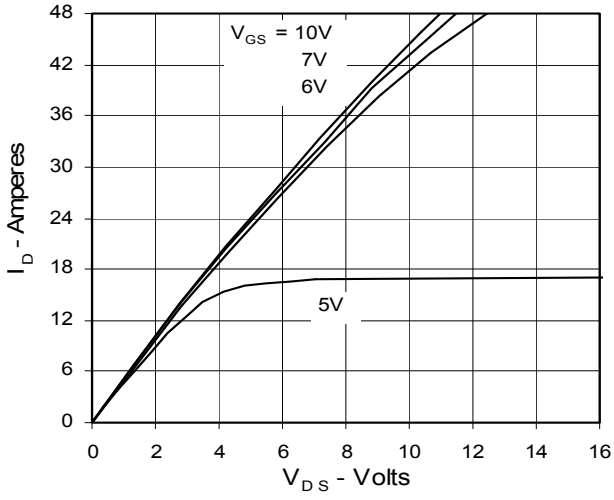


Fig. 4. $R_{DS(on)}$ Normalized to I_{D25} Value vs. Junction Temperature

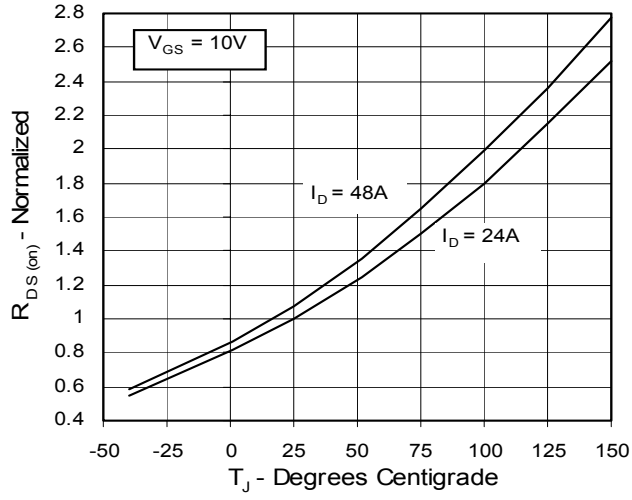


Fig. 5. $R_{DS(on)}$ Normalized to I_{D25} Value vs. I_D

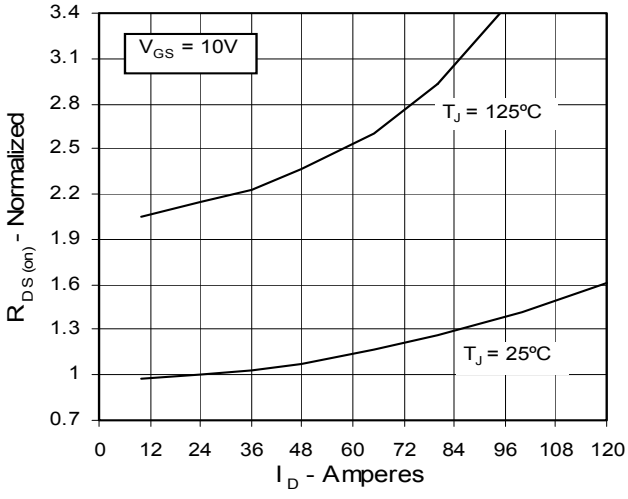


Fig. 6. Drain Current vs. Case Temperature

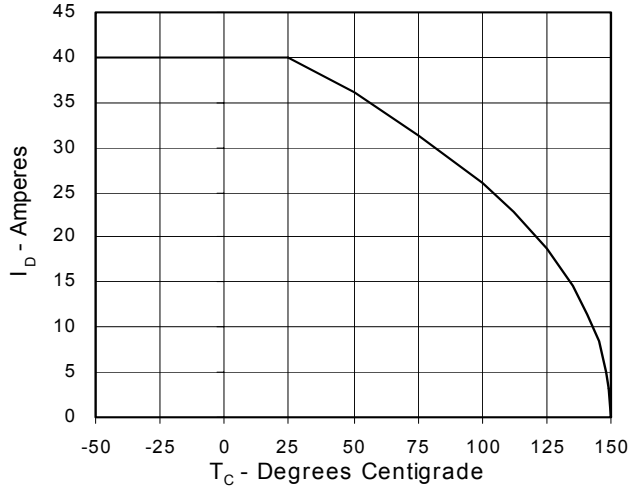


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Fig. 7. Input Admittance

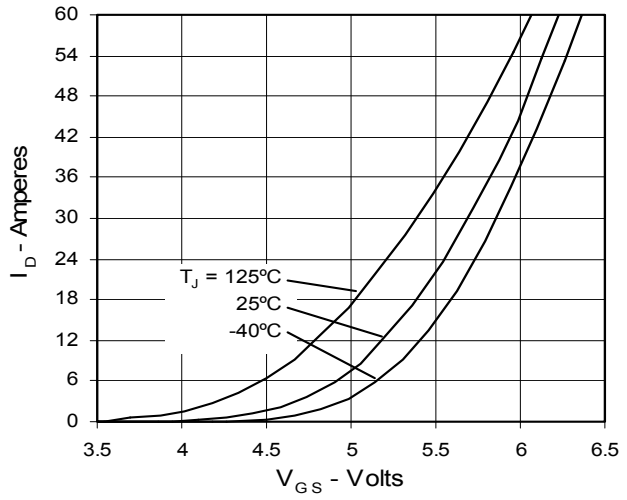


Fig. 8. Transconductance

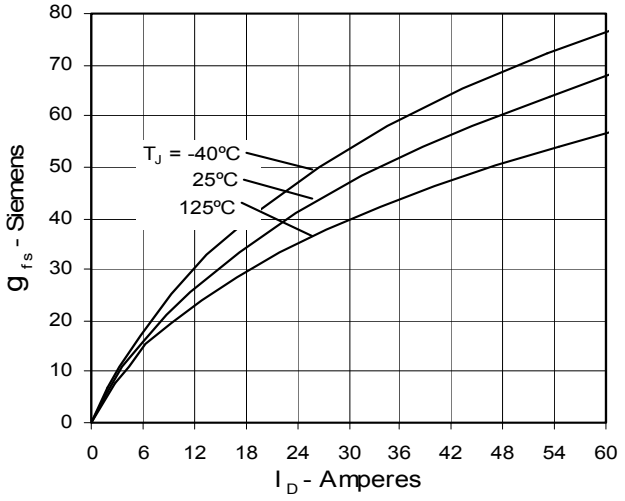


Fig. 9. Source Current vs. Source-To-Drain Voltage

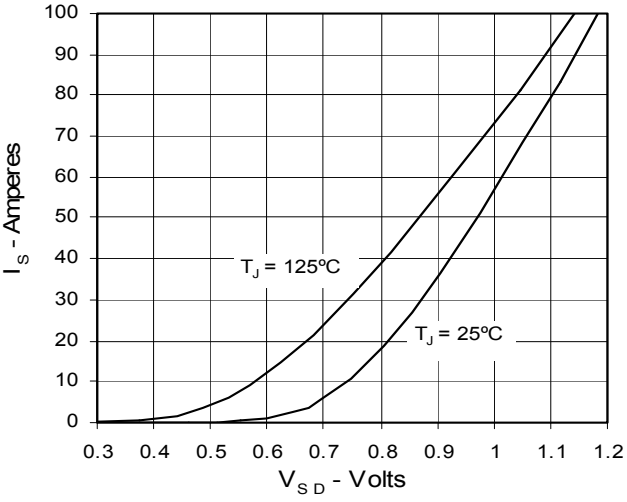


Fig. 10. Gate Charge

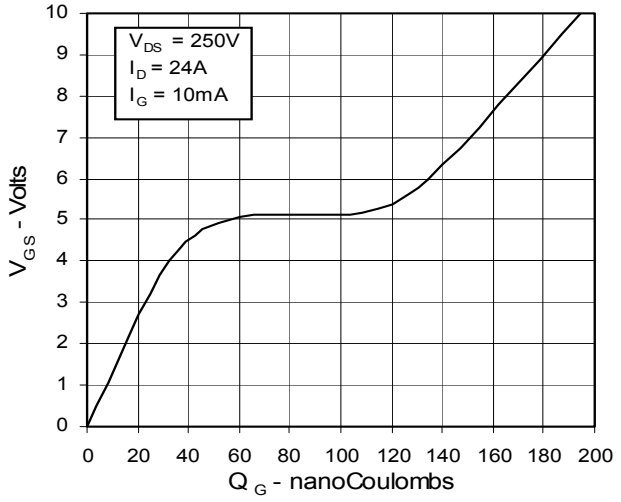


Fig. 11. Capacitance

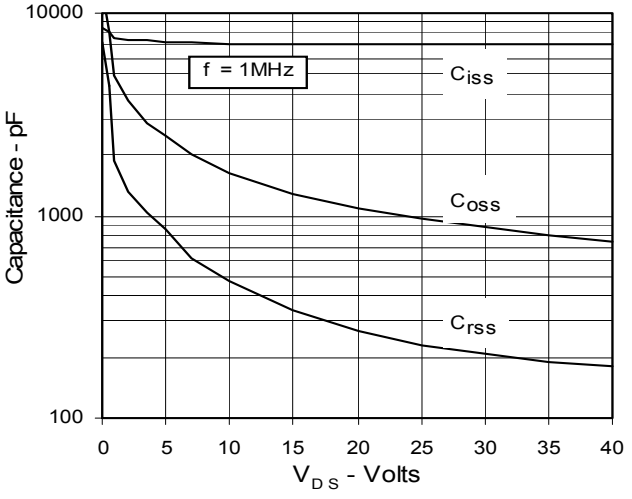
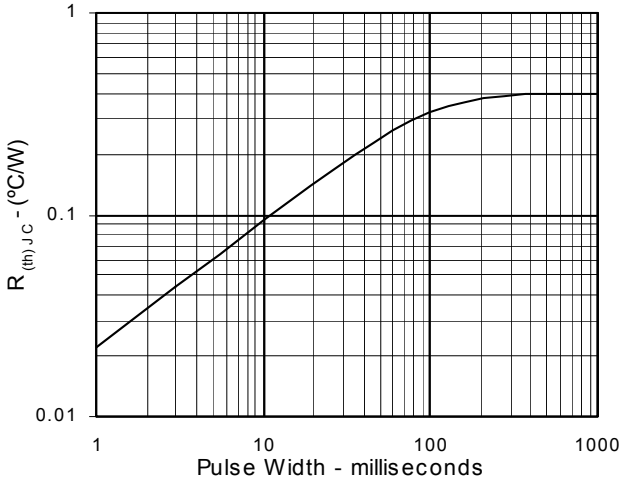


Fig. 12. Maximum Transient Thermal Resistance



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