

# Thyristor

$$V_{RRM} = 1600 \text{ V}$$

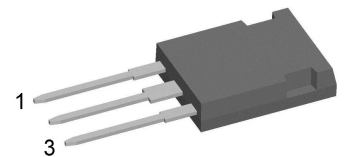
$$I_{TAV} = 45 \text{ A}$$

$$V_T = 1.37 \text{ V}$$

## Single Thyristor

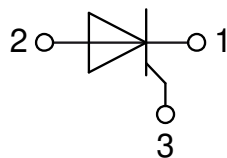
Part number

**CS45-16io1R**



Backside: isolated

 E72873



### Features / Advantages:

- Thyristor for line frequency
- Planar passivated chip
- Long-term stability

### Applications:

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

### Package: ISOPLUS247

- Isolation Voltage: 3600 V~
- Industry standard outline
- RoHS compliant
- Epoxy meets UL 94V-0
- Soldering pins for PCB mounting
- Backside: DCB ceramic
- Reduced weight
- Advanced power cycling

### Disclaimer Notice

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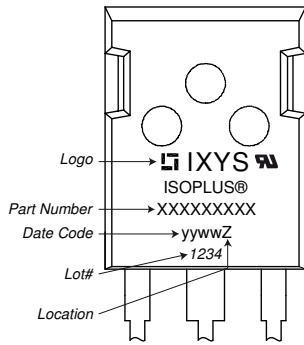


Thyristor			Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit
$V_{RSM/DSM}$	max. non-repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			1700	V
$V_{RRM/DRM}$	max. repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			1600	V
$I_{RD}$	reverse current, drain current	$V_{R/D} = 1600 V$	$T_{VJ} = 25^{\circ}C$		50	$\mu A$
		$V_{R/D} = 1600 V$	$T_{VJ} = 125^{\circ}C$		3	mA
$V_T$	forward voltage drop	$I_T = 45 A$	$T_{VJ} = 25^{\circ}C$		1.36	V
		$I_T = 90 A$			1.73	V
		$I_T = 45 A$	$T_{VJ} = 125^{\circ}C$		1.37	V
		$I_T = 90 A$			1.85	V
$I_{TAV}$	average forward current	$T_C = 90^{\circ}C$	$T_{VJ} = 150^{\circ}C$		45	A
$I_{T(RMS)}$	RMS forward current	180° sine			71	A
$V_{T0}$	threshold voltage	} for power loss calculation only	$T_{VJ} = 150^{\circ}C$		0.88	V
$r_T$	slope resistance				11	m $\Omega$
$R_{thJC}$	thermal resistance junction to case				0.6	K/W
$R_{thCH}$	thermal resistance case to heatsink			0.3		K/W
$P_{tot}$	total power dissipation		$T_C = 25^{\circ}C$		208	W
$I_{TSM}$	max. forward surge current	$t = 10 ms; (50 Hz), sine$	$T_{VJ} = 45^{\circ}C$		520	A
		$t = 8,3 ms; (60 Hz), sine$	$V_R = 0 V$		560	A
		$t = 10 ms; (50 Hz), sine$	$T_{VJ} = 150^{\circ}C$		440	A
		$t = 8,3 ms; (60 Hz), sine$	$V_R = 0 V$		475	A
$I^2t$	value for fusing	$t = 10 ms; (50 Hz), sine$	$T_{VJ} = 45^{\circ}C$		1.35	kA <sup>2</sup> s
		$t = 8,3 ms; (60 Hz), sine$	$V_R = 0 V$		1.31	kA <sup>2</sup> s
		$t = 10 ms; (50 Hz), sine$	$T_{VJ} = 150^{\circ}C$		970	A <sup>2</sup> s
		$t = 8,3 ms; (60 Hz), sine$	$V_R = 0 V$		940	A <sup>2</sup> s
$C_J$	junction capacitance	$V_R = 400 V f = 1 MHz$	$T_{VJ} = 25^{\circ}C$		22	pF
$P_{GM}$	max. gate power dissipation	$t_p = 30 \mu s$	$T_C = 150^{\circ}C$		10	W
		$t_p = 300 \mu s$			5	W
$P_{GAV}$	average gate power dissipation				0.5	W
$(di/dt)_{cr}$	critical rate of rise of current	$T_{VJ} = 125^{\circ}C; f = 50 Hz$ repetitive, $I_T = 135 A$			150	A/ $\mu s$
		$t_p = 200 \mu s; di_G/dt = 0.3 A/\mu s;$ $I_G = 0.3 A; V = \frac{2}{3} V_{DRM}$ non-repet., $I_T = 45 A$			500	A/ $\mu s$
$(dv/dt)_{cr}$	critical rate of rise of voltage	$V = \frac{2}{3} V_{DRM}$ $R_{GK} = \infty; method 1 (linear voltage rise)$	$T_{VJ} = 125^{\circ}C$		1000	V/ $\mu s$
$V_{GT}$	gate trigger voltage	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		1.5	V
			$T_{VJ} = -40^{\circ}C$		1.6	V
$I_{GT}$	gate trigger current	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		80	mA
			$T_{VJ} = -40^{\circ}C$		200	mA
$V_{GD}$	gate non-trigger voltage	$V_D = \frac{2}{3} V_{DRM}$	$T_{VJ} = 125^{\circ}C$		0.2	V
$I_{GD}$	gate non-trigger current				10	mA
$I_L$	latching current	$t_p = 10 \mu s$	$T_{VJ} = 25^{\circ}C$		150	mA
		$I_G = 0.3 A; di_G/dt = 0.3 A/\mu s$				
$I_H$	holding current	$V_D = 6 V R_{GK} = \infty$	$T_{VJ} = 25^{\circ}C$		100	mA
$t_{gd}$	gate controlled delay time	$V_D = \frac{1}{2} V_{DRM}$	$T_{VJ} = 25^{\circ}C$		2	$\mu s$
		$I_G = 0.3 A; di_G/dt = 0.3 A/\mu s$				
$t_q$	turn-off time	$V_R = 100 V; I_T = 45 A; V = \frac{2}{3} V_{DRM}$ $di/dt = 15 A/\mu s dv/dt = 20 V/\mu s t_p = 200 \mu s$	$T_{VJ} = 125^{\circ}C$		150	$\mu s$



Package ISOPLUS247		Ratings				
Symbol	Definition	Conditions	min.	typ.	max.	Unit
$I_{RMS}$	RMS current	per terminal			70	A
$T_{VJ}$	virtual junction temperature		-40		150	°C
$T_{op}$	operation temperature		-40		125	°C
$T_{stg}$	storage temperature		-40		150	°C
<b>Weight</b>				6		g
$F_C$	mounting force with clip		20		120	N
$d_{Spp/ App}$	creepage distance on surface / striking distance through air	terminal to terminal	2.7			mm
$d_{Spb/ Apb}$		terminal to backside	4.1			mm
$V_{ISOL}$	isolation voltage	t = 1 second	3600			V
		t = 1 minute	3000			V
		50/60 Hz, RMS; $I_{ISOL} \leq 1$ mA				

**Product Marking**



Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	CS45-16io1R	CS45-16io1R	Tube	30	480312

Similar Part	Package	Voltage class
CS45-08io1	TO-247AD (3)	800
CS45-12io1	TO-247AD (3)	1200
CS45-16io1	TO-247AD (3)	1600

**Equivalent Circuits for Simulation**

\* on die level

$T_{VJ} = 150^{\circ}C$

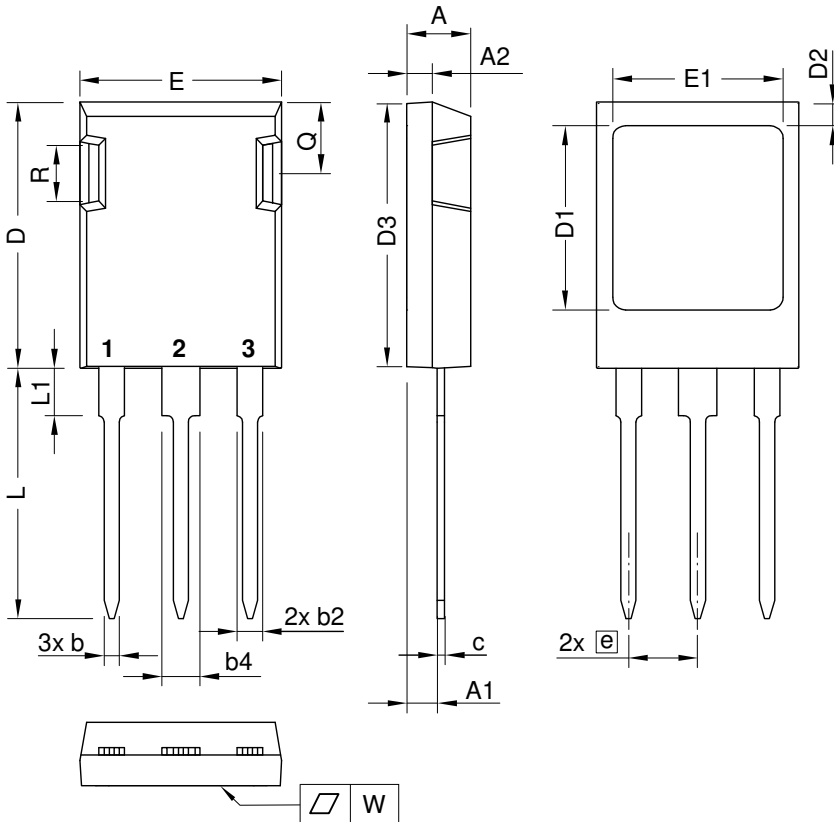


**Thyristor**

$V_{0 \max}$	threshold voltage	0.88	V
$R_{0 \max}$	slope resistance *	8.5	mΩ



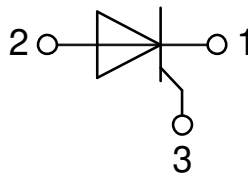
**Outlines ISOPLUS247**



Dim.	Millimeter		Inches	
	min	max	min	max
A	4.83	5.21	0.190	0.205
A1	2.29	2.54	0.090	0.100
A2	1.91	2.16	0.075	0.085
b	1.14	1.40	0.045	0.055
b2	1.91	2.20	0.075	0.087
b4	2.92	3.24	0.115	0.128
c	0.61	0.83	0.024	0.033
D	20.80	21.34	0.819	0.840
D1	15.75	16.26	0.620	0.640
D2	1.65	2.15	0.065	0.085
D3	20.30	20.70	0.799	0.815
E	15.75	16.13	0.620	0.635
E1	13.21	13.72	0.520	0.540
e	5.45 BSC		0.215 BSC	
L	19.81	20.60	0.780	0.811
L1	3.81	4.38	0.150	0.172
Q	5.59	6.20	0.220	0.244
R	4.25	5.50	0.167	0.217
W	-	0.10	-	0.004

Die konvexe Form des Substrates ist typ. < 0.04 mm über der Kunststoffoberfläche der Bauteilunterseite  
The convex bow of substrate is typ. < 0.04 mm over plastic surface level of device bottom side

Die Gehäuseabmessungen entsprechen dem Typ TO-247 AD gemäß JEDEC außer Schraubloch und L<sub>max</sub>.  
This drawing will meet all dimensions requirement of JEDEC outline TO-247 AD except screw hole and except L<sub>max</sub>.



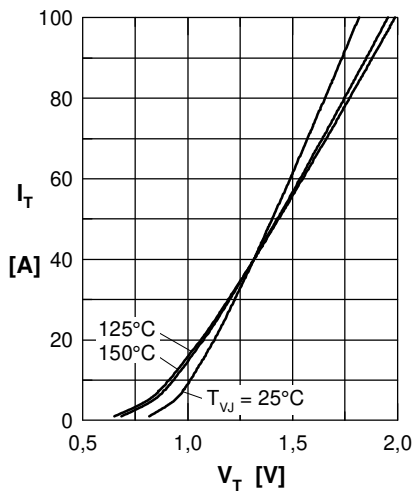
**Thyristor**


Fig. 1 Forward characteristics

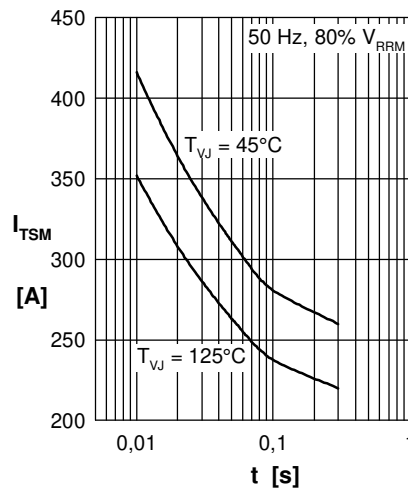


Fig. 2 Surge overload current

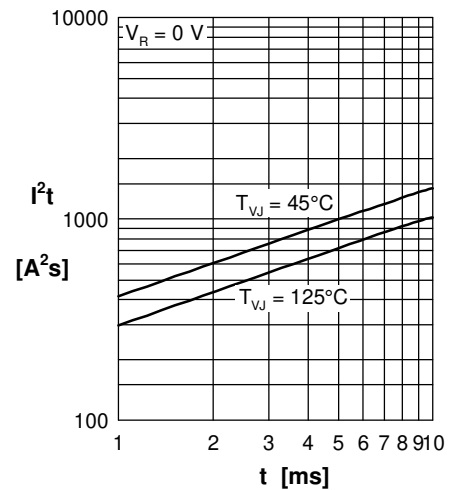
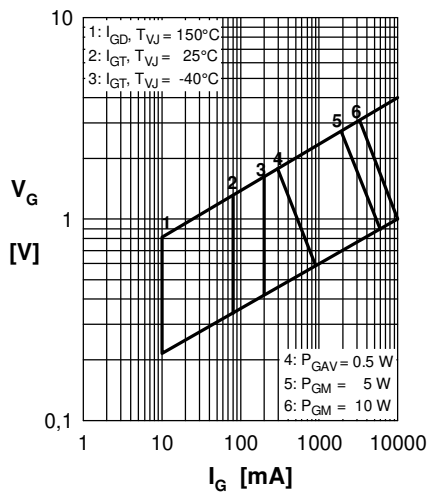

 Fig. 3  $I^2t$  versus time (1-10 ms)


Fig. 4 Gate trigger characteristics

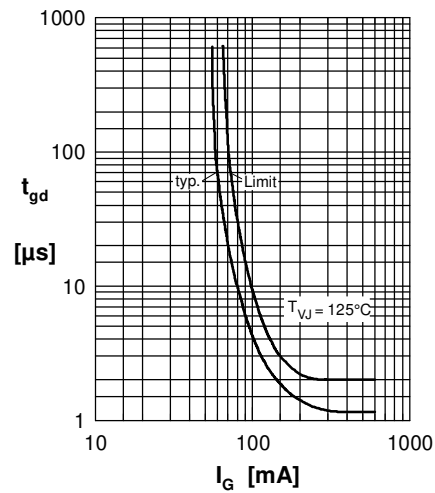


Fig. 5 Gate controlled delay time

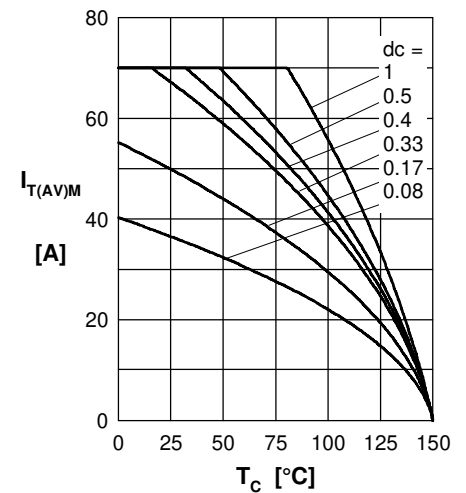


Fig. 6 Max. forward current at case temperature

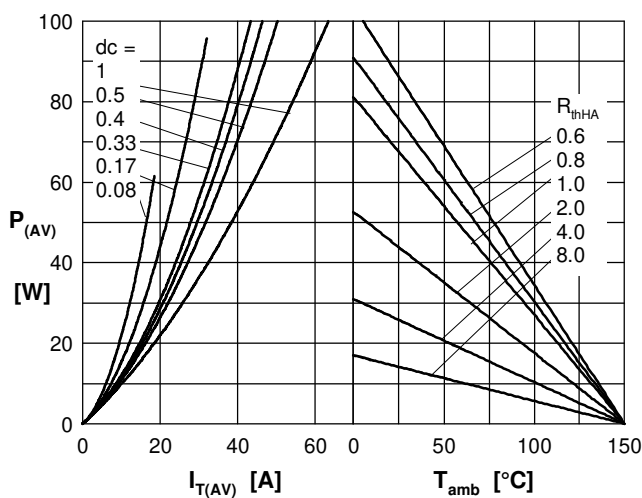
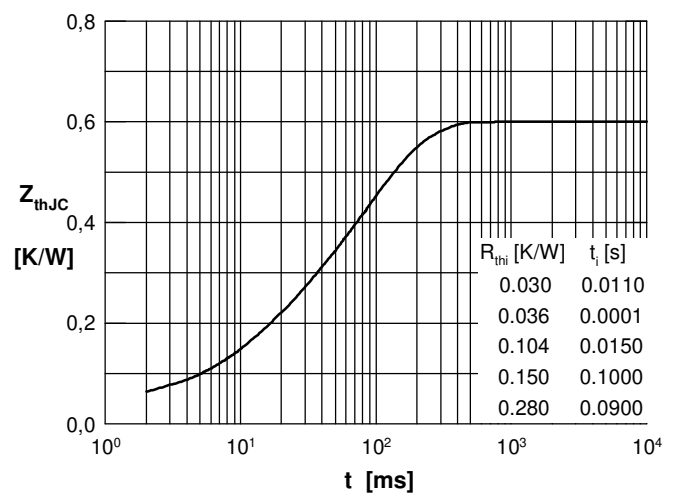

 Fig. 7a Power dissipation versus direct output current  
 Fig. 7b and ambient temperature


Fig. 8 Transient thermal impedance junction to case