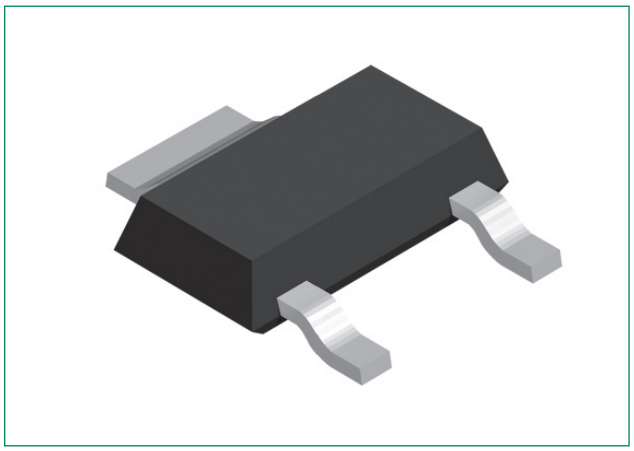
CPC3981Z

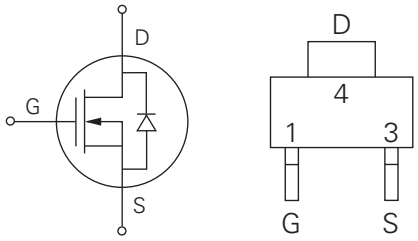
800V, 45Ω N-Channel MOSFET

Key Attributes

Characteristic	Rating	Unit
$V_{(BR)DSX}$	800	V
T_J	150	°C
$R_{DS(on)}$	45	Ω
I_{DSS}	100	mA



Pinout Diagram (SOT-223-2L)



G: Gate; **D:** Drain; **S:** Source

Description

The CPC3981Z is an 800V, N-channel, depletion-mode, Field Effect Transistor (FET) in a modified SOT-223 package to provide greater separation of the drain and source leads for high voltage applications.

The CPC3981Z's robust MOSFET has been used extensively in Littelfuse Integrated Circuits' Solid State Relays in power, industrial, and telecommunications applications.

The CPC3981Z is available in the SOT-223-2L package.

Features & Benefits

- 800V breakdown voltage
- 45Ω on-resistance
- $V_{GS(off)}$: -1.4V to -3.1V
- T_J(max): 150°C
- High input impedance

Applications

- Normally on switches
- Solid state relays
- Converters
- Telecommunications
- Power supplies
- Current regulators

Ordering Information

Part #	Description
CPC3981ZTR	SOT-223-2L: Tape and Reel (3000/Reel)

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Absolute Maximum Ratings

Parameter	Rating	Unit
Drain-to-Source Voltage	800	V
Gate-to-Source Voltage	±15	V
Pulsed Drain Current	150	mA
Total Package Dissipation [1]	2.25	W
Operational Temperature, Ambient	-55 to +150	°C
Junction Temperature, Maximum	+150	°C
Storage Temperature	-55 to +150	°C

[1] Mounted on 1"x1" 2 oz. Copper FR4 board.

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied. Absolute Maximum Ratings are at T_A=25°C.

Unless otherwise specified, device characteristics are at T_A=25°C. Typical values are characteristic of the device at T_A=25°C and are the result of engineering evaluations. They are provided for informational purposes only and are not part of the manufacturing testing requirements.

Electrical Characteristics

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSX}$	V_{GS}=-5.5V, I_D=1µA	800	-	-	V
Gate-to-Source Off Voltage	$V_{GS(off)}$	V_{DS}=15V, I_D=1µA	-1.4	-	-3.1	V
Change in $V_{GS(off)}$ with Temperature	$dV_{GS(off)}/dT$	V_{DS}=15V, I_D=1µA	-	-	-6.3	mV/°C
Gate Leakage Current	I_{GSS}	V_{GS}=±15V, V_{DS}=0V	-	-	100	nA
Drain-to-Source Off-state Leakage Current	$I_{D(off)}$	V_{GS}=-5.5V, V_{DS}=800V	-	-	1	µA
Saturated Drain-to-Source Current	I_{DSS}	V_{GS}=0V, V_{DS}=15V	100	-	-	mA
Static Drain-to-Source On-State Resistance*	$R_{DS(on)}$	V_{GS}=0V, I_D=100mA	-	32.5	45	Ω
Change in $R_{DS(on)}$ with Temperature	$dR_{DS(on)}/dT$		-	-	2.5	%/°C
Forward Transconductance	g_{fs}	I_D=50mA, V_{DS}=10V	100	-	-	mS
Input Capacitance	C_{ISS}	V_{GS}=-3.5V V_{DS}=25V f=1MHz	-	105	-	pF
Output Capacitance	C_{OSS}			7.5		
Reverse Transfer Capacitance	C_{RSS}			2.75		
Drain-Source Reverse Voltage	V_{SD}	V_{GS}=-5.5V, I_S=100mA	-	0.67	0.95	V

*Measurement taken within 500µs

Timing Characteristics

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Turn-On Delay Time	$t_{d(on)}$	V_{DD}=25V, I_D=50mA, V_{GS}=0V to -10V, R_{GEN}=50Ω	-	79.2	170	ns
Fall Time	t_f			34.9	145	
Turn-Off Delay Time	$t_{d(off)}$			25.3	65	
Rise Time	t_r			19.7	35	

Thermal Characteristics

Parameter	Symbol	Rating	Unit
Thermal Resistance			
Junction to Ambient	$R_{th(J-A)}$	55	°C/W
Junction to Case	$R_{th(J-C)}$	23	

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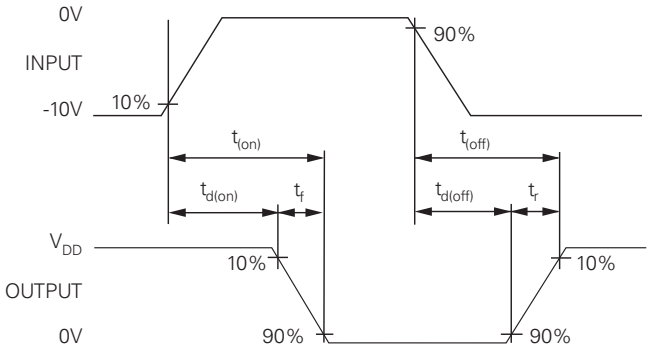
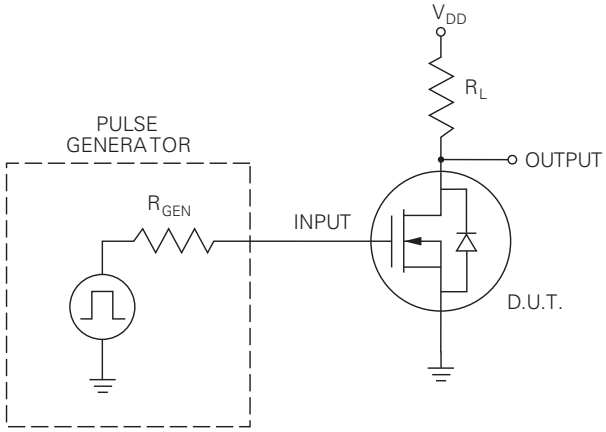
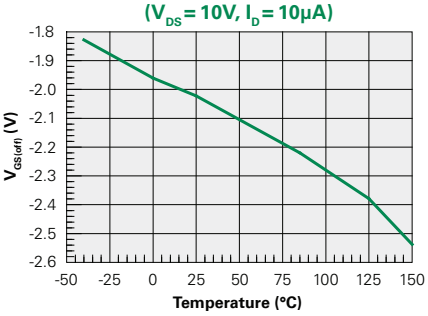
Switching Waveform & Test Circuit



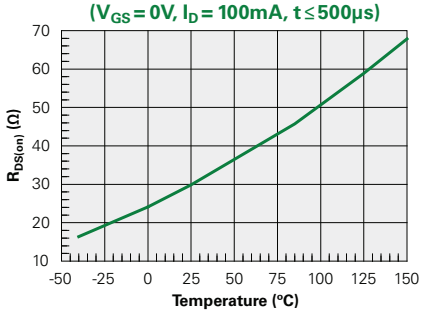


Characteristic Curves*

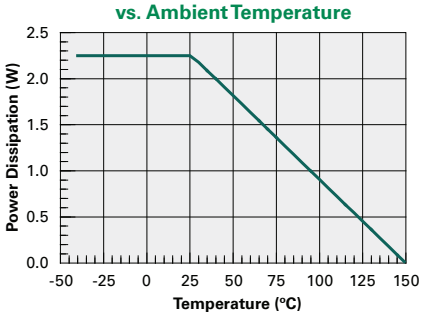
Threshold Voltage vs. Ambient Temperature (V_{DS} = 10V, I_D = 10µA)



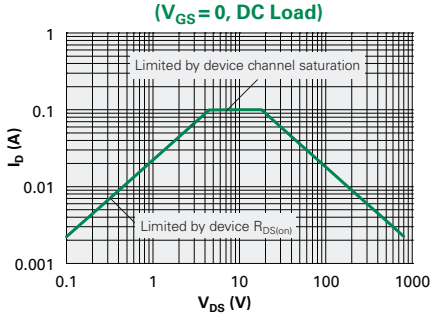
On-Resistance vs. Ambient Temperature (V_{GS} = 0V, I_D = 100mA, t ≤ 500µs)



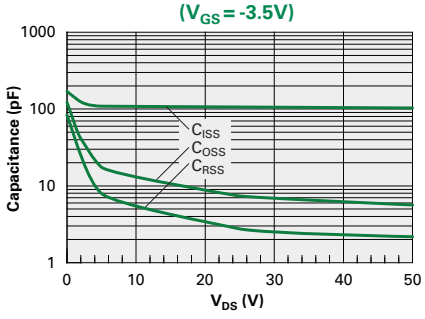
Maximum Power Dissipation vs. Ambient Temperature



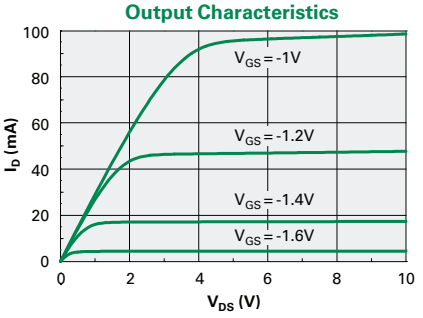
Forward Bias Safe Operating Area (V_{GS} = 0, DC Load)



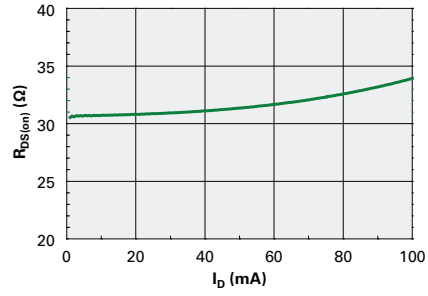
Capacitance vs. Drain-Source Voltage (V_{GS} = -3.5V)



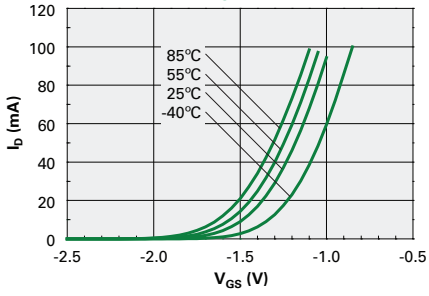
Output Characteristics



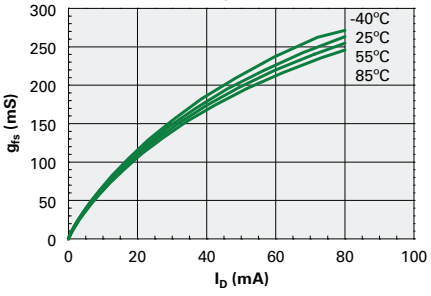
On-Resistance vs. Drain Current (V_{GS} = 0V, t ≤ 500µs)



Input Admittance (V_{DS} = 10V)



Transconductance vs. Drain Current (V_{DS} = 10V)



*Unless otherwise noted, data presented in these graphs is typical of device operation at T_A = 25°C.

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Manufacturing Information

Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. Littelfuse classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, IPC/JEDEC J-STD-020, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a Moisture Sensitivity Level (MSL) classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard IPC/JEDEC J-STD-033.

Device	Moisture Sensitivity Level (MSL) Classification
CPC3981Z	MSL 3

ESD Sensitivity

This product is ESD Sensitive, and should be handled according to the industry standard JESD-625.

Soldering Profile

Provided in the table below is the IPC/JEDEC J-STD-020 Classification Temperature (T_C) and the maximum total dwell time (t_P) in all reflow processes that the body temperature of these surface mount devices may be (T_C - 5)°C or greater. The device's body temperature must not exceed the Classification Temperature at any time during reflow soldering processes.

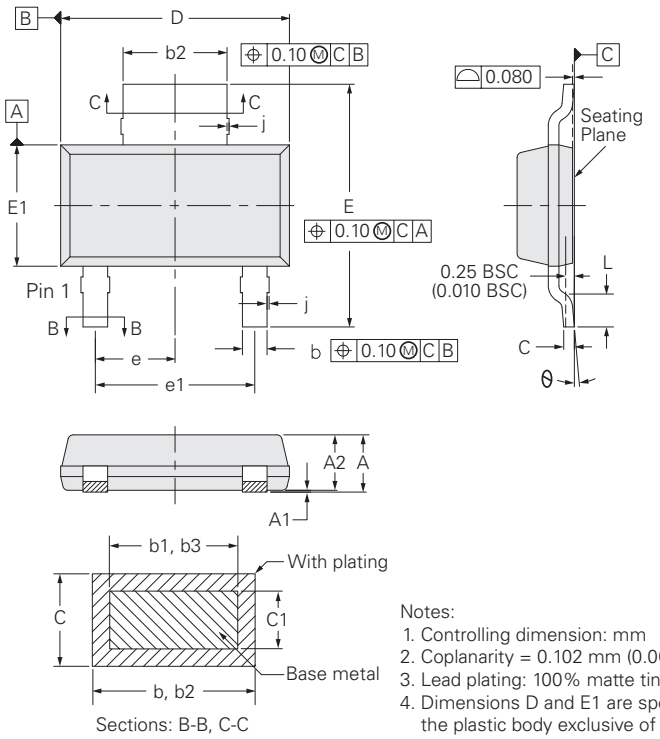
Device	Classification Temperature (T_C)	Dwell Time (t_P)	Max Reflow Cycles
CPC3981Z	260°C	30 seconds	3

Board Wash

Littelfuse recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to halide flux or solvents.

Mechanical Dimensions

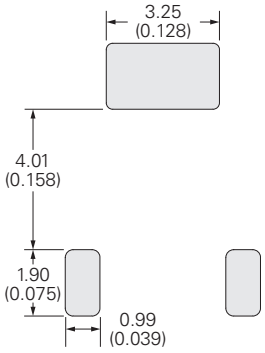
CPC3981Z Part Outline Drawing and PCB Land Pattern



Sections: B-B, C-C

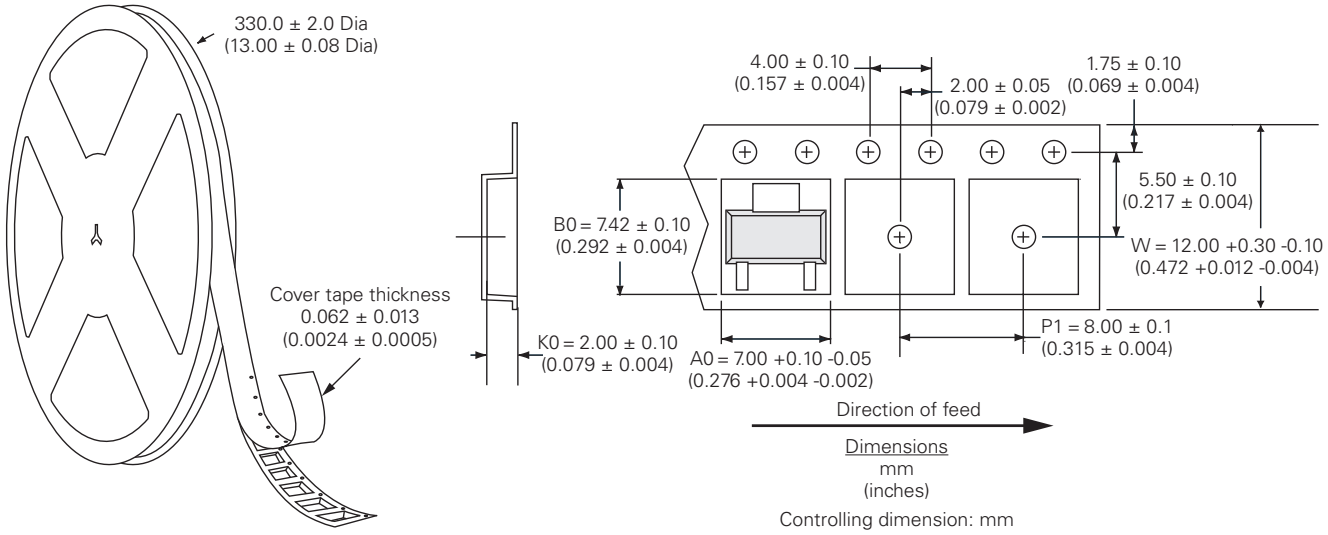
Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	-	1.80	-	0.071
A1	0.02	0.10	0.001	0.004
A2	1.50	1.70	0.059	0.067
b	0.66	0.84	0.026	0.033
b1	0.60	0.79	0.024	0.031
b2	2.90	3.10	0.114	0.122
b3	2.84	3.05	0.112	0.120
c	0.23	0.35	0.009	0.014
c1	0.23	0.33	0.009	0.013
D	6.30	6.70	0.248	0.264
E	6.70	7.30	0.264	0.287
E1	3.30	3.70	0.130	0.146
e	2.30 BSC		0.091 BSC	
e1	4.60 BSC		0.182 BSC	
L	0.81	1.10	0.032	0.043
θ	0°	10°	0°	10°
j	-	0.13	-	0.005

Recommended PCB Land Pattern



Notes:
1. Controlling dimension: mm
2. Coplanarity = 0.102 mm (0.004") max
3. Lead plating: 100% matte tin, 1000 µinches max
4. Dimensions D and E1 are specified at the outermost edges of the plastic body exclusive of mold flash, burrs, and interlead flash.

CPC3981ZTR Tape & Reel



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