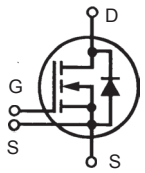
IXYS

HiPerFET™ Power MOSFETs Single Die MOSFET

IXFN 80N50

N-Channel Enhancement Mode
Avalanche Rated, High dv/dt, Low t_{rr}

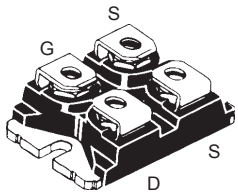
V_{DSS} = 500 V
I_{D25} = 80 A
$R_{DS(on)}$ = 55 mΩ
t_{rr} ≤ 250 ns



Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	500	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ	500	V
V_{GS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	T_C = 25°C, Chip capability	80	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}	320	A
I_{AR}	T_C = 25°C	80	A
E_{AR}	T_C = 25°C	64	mJ
E_{AS}	T_C = 25°C	6	J
dv/dt	$I_S \le I_{DM}$, di/dt ≤ 100 A/µs, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$, R_G = 2 Ω	5	V/ns
P_D	T_C = 25°C	780	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
V_{ISOL}	50/60 Hz, RMS t = 1 min	2500	V~
	I_{ISOL} ≤ 1 mA t = 1 s	3000	V~
M_d	Mounting torque	1.5/13	Nm/lb.in.
	Terminal connection torque	1.5/13	Nm/lb.in.
Weight		30	g

Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
V_{DSS}	V_{GS} = 0 V, I_D = 3 mA	500			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 8 mA	2.5		4.5	V
I_{GSS}	V_{GS} = ±20 V_{DC}, V_{DS} = 0			±200	nA
I_{DSS}	$V_{DS} = V_{DSS}$, T_J = 25°C			100	µA
	V_{GS} = 0 V, T_J = 125°C			2	mA
$R_{DS(on)}$	V_{GS} = 10 V, $I_D = 0.5 \bullet I_{D25}$ Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %			55	mΩ

miniBLOC, SOT-227 B (IXFN)
E153432



G = Gate D = Drain
S = Source

Either Source terminal of miniBLOC can be used as Main or Kelvin Source

Features

- International standard package
- miniBLOC, with Aluminium nitride isolation
- Low $R_{DS(on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
- Fast intrinsic Rectifier

Applications

- DC-DC converters
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- Temperature and lighting controls

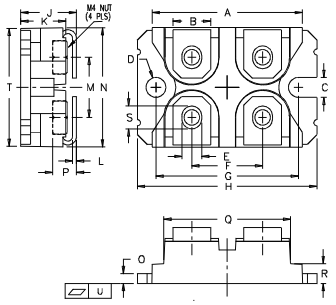
Advantages

- Easy to mount
- Space savings
- High power density

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Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
g_{fs}	V_{DS} = 15 V; I_D = 0.5 • I_{D25}, pulse test	50	70		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		9890		pF
C_{oss}			1750		pF
C_{rss}			460		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25} R_G = 1 Ω (External),		61		ns
t_r			70		ns
$t_{d(off)}$			102		ns
t_f			27		ns
$Q_{G(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25}		380		nC
Q_{GS}			80		nC
Q_{GD}			173		nC
R_{thJC}				0.16	K/W
R_{thCK}			0.05		K/W

miniBLOC, SOT-227 B



M4 screws (4x) supplied

Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	31.50	31.88	1.240	1.255
B	7.80	8.20	0.307	0.323
C	4.09	4.29	0.161	0.169
D	4.09	4.29	0.161	0.169
E	4.09	4.29	0.161	0.169
F	14.91	15.11	0.587	0.595
G	30.12	30.30	1.186	1.193
H	38.00	38.23	1.496	1.505
J	11.68	12.22	0.460	0.481
K	8.92	9.60	0.351	0.378
L	0.76	0.84	0.030	0.033
M	12.60	12.85	0.496	0.506
N	25.15	25.42	0.990	1.001
O	1.98	2.13	0.078	0.084
P	4.95	5.97	0.195	0.235
Q	26.54	26.90	1.045	1.059
R	3.94	4.42	0.155	0.174
S	4.72	4.85	0.186	0.191
T	24.59	25.07	0.968	0.987
U	-0.05	0.1	-0.002	0.004

Source-Drain Diode

Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
I_S	V_{GS} = 0 V			80	A
I_{SM}	Repetitive; pulse width limited by T_{JM}			320	A
V_{SD}	I_F = I_S, V_{GS} = 0 V, Pulse test, t < 300 ms, duty cycle d < 2 %			1.3	V
t_{rr}	I_F = 30A, -di/dt = 100 A/µs, V_R = 100 V			250	ns
Q_{RM}			1.2		µC
I_{RM}			8		A

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETS and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,881,106 5,017,508 5,049,961 5,187,117 5,486,715 6,306,728B1 4,850,072 4,931,844 5,034,796 5,063,307 5,237,481 5,381,025

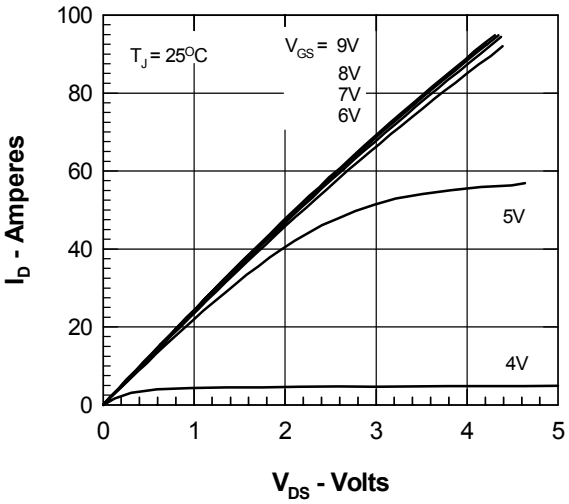


Fig. 1. Output Characteristics

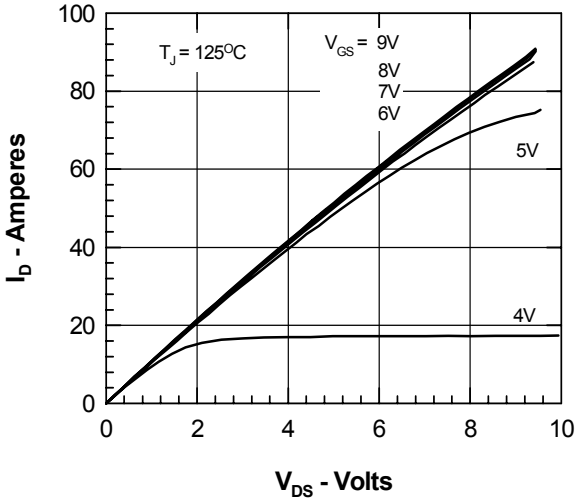


Fig. 2. High Temperature Output Characteristics

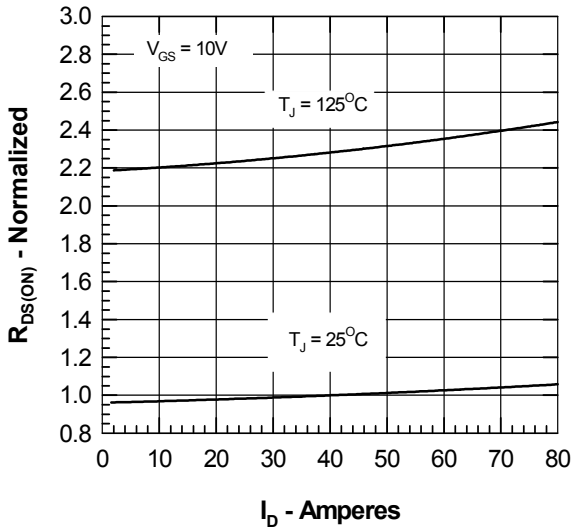


Fig. 3. Normalized $R_{DS(on)}$ vs. Drain Current

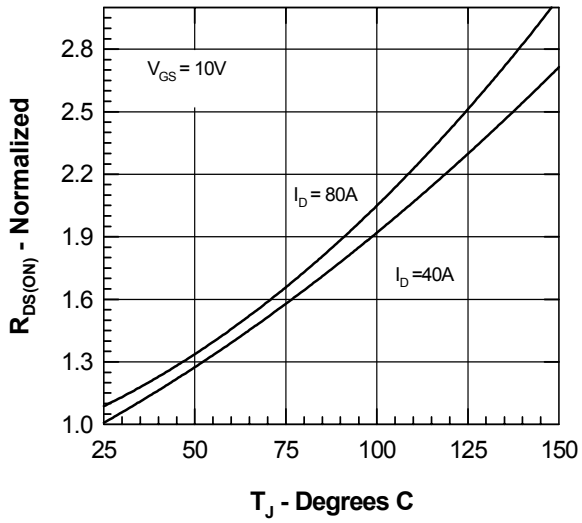


Fig. 4. Temperature Dependence of $R_{DS(on)}$

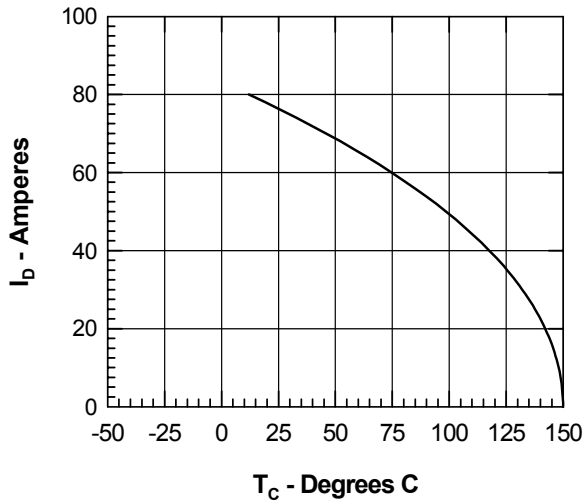


Fig. 5 Drain Current vs. Case Temperature

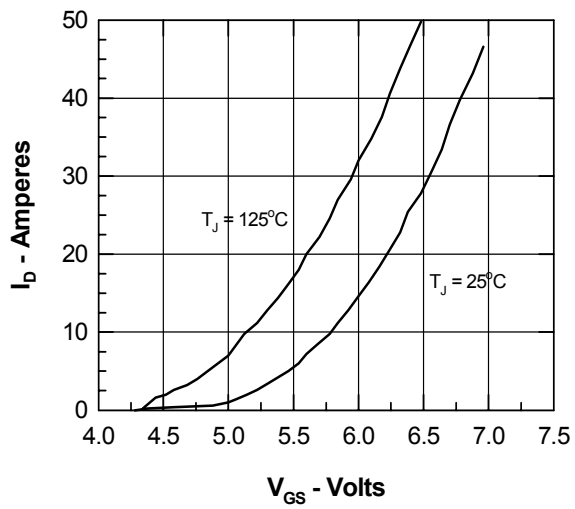


Fig. 6. Input Admittance

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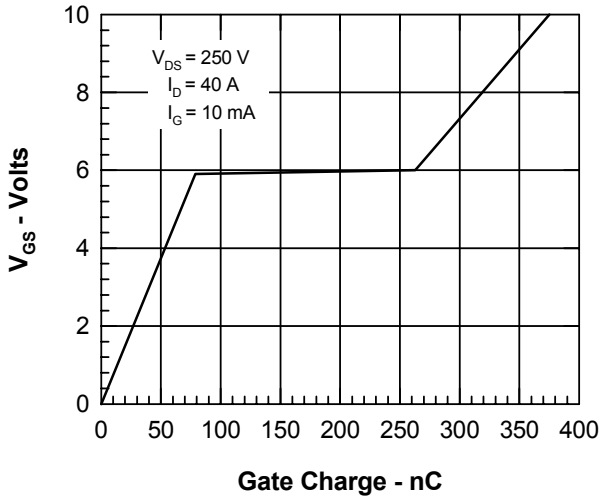


Fig. 7 Gate Charge Characteristic Curve

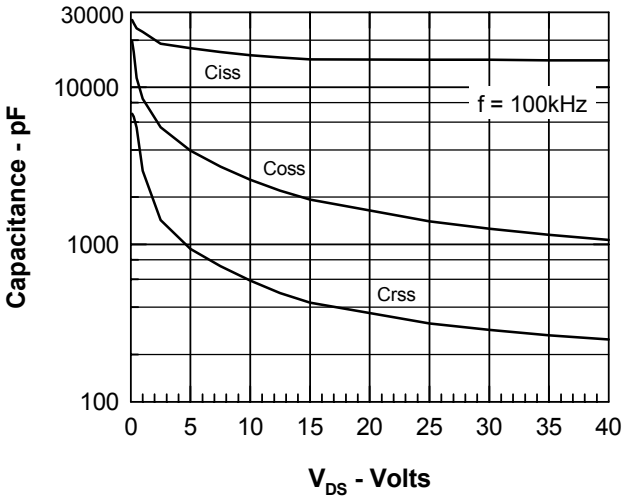


Fig. 8 Capacitance Curves

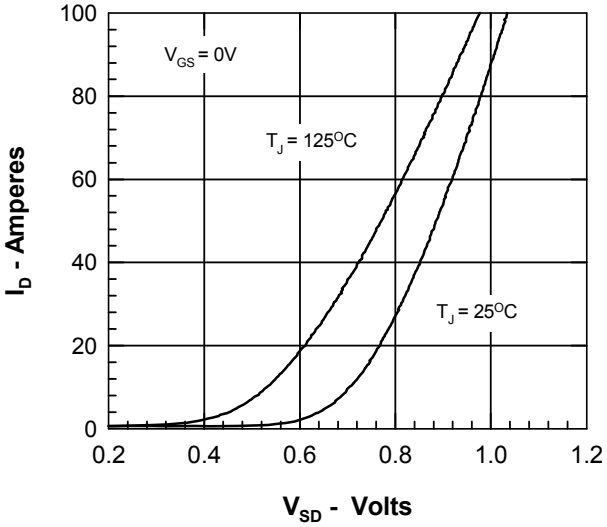


Fig. 9. Source-to-Drain Voltage Drop

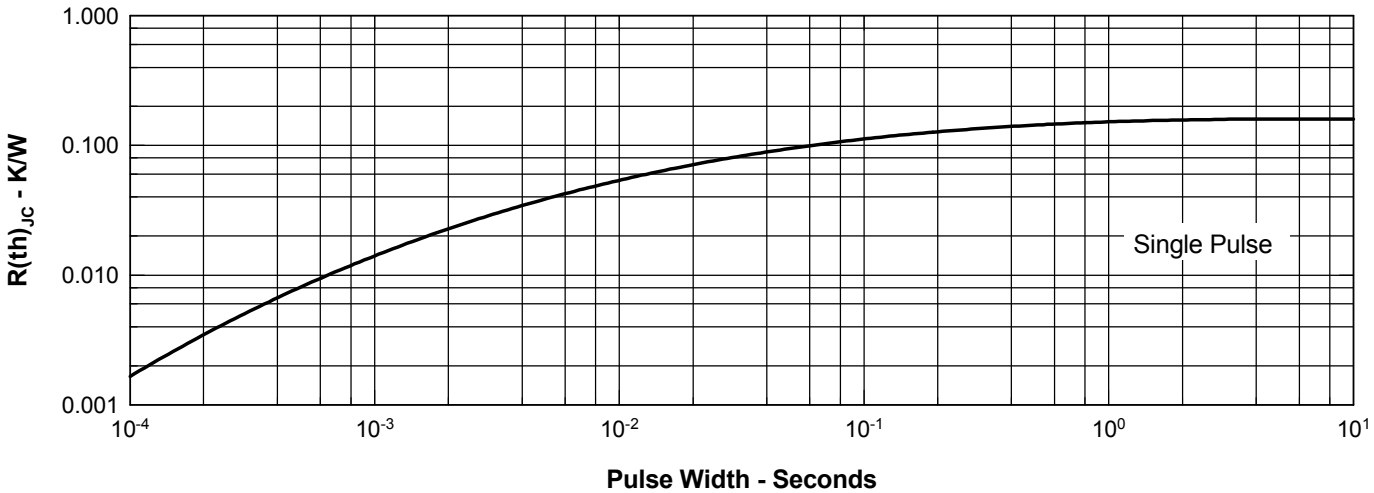


Fig.10. Transient Thermal Resistance

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