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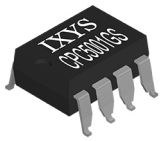
INTEGRATED CIRCUITS DIVISION



CPC5001
Dual, One Channel Each Direction Digital Optical Isolator

Features

- Isolates One Signal in Each Direction
- Operates From 2.7V to 5.5V
- Buffered Inputs - No External LED Drive Required
- Voltage Level Translation
- Hysteresis at Inputs for Noise Rejection
- Slew-Limited Drivers Reduce EMI
- Power-Down to Hi-Z Does Not Load Outputs
- 5Mbaud Data Rate
- 8-Pin DIP or Surface Mount Packages
- Flammability Rating UL 94 V-0

Applications

- Isolated Signal Monitoring and Control
- Power-Over-Ethernet
- Power Supply High-Side Interface
- Logic-Level Translation
- Microprocessor System Interface
- Inter-Integrated Circuit (I^2C) Interface
- Serial Peripheral Interface (SPI)
- Full Duplex Communication
- Isolated Line Receiver
- Isolated Data Acquisition Systems

Approvals

- UL Recognized Component: File # E76270
- CSA Certified Component: Certificate # 70157867
- TUV EN 62368-1: Certificate # B 082667 0008

Description

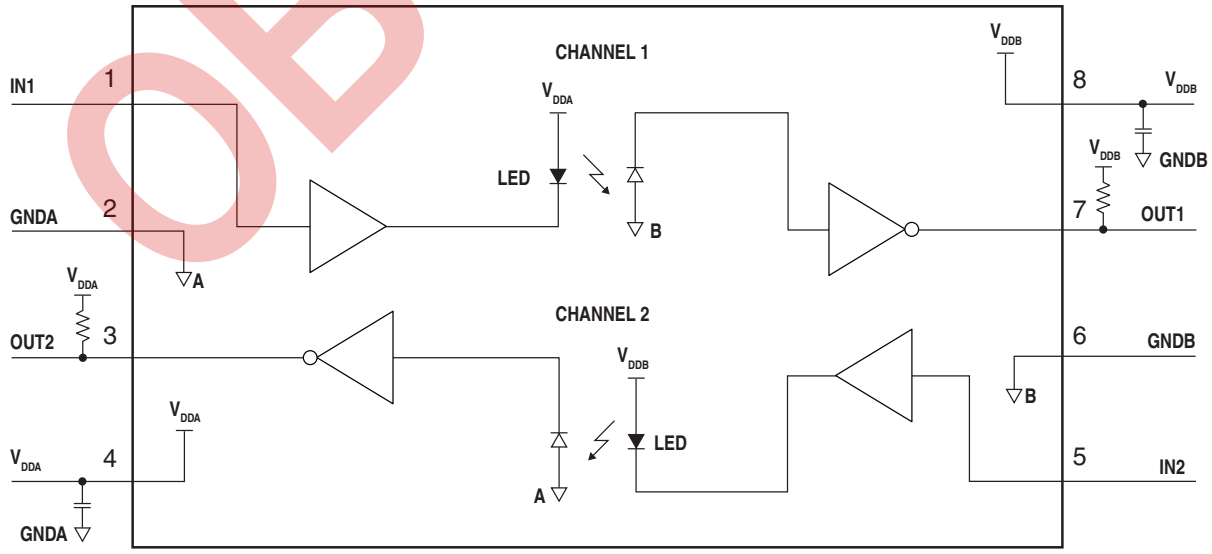
The CPC5001 is a dual, non-inverting digital optical isolator with buffered-logic inputs and open-drain outputs. Channel 1 propagates a signal from Side A to Side B, while Channel 2 sends a signal from Side B to Side A. It provides galvanic isolation up to $3750V_{rms}$. When the two sides are powered by supplies with different voltages, it also functions as a logic level translator for supply voltages as low as 2.7V or as high as 5.5V. Available in 8-pin DIP and surface mount packages, it functionally replaces two logic buffers and two single-channel optoisolators. Internal bandgap references regulate the LED drive currents to 3mA to reduce peak power requirements.

Unlike transformer or capacitive isolators, optical isolation passes DC signals, and does not need to be clocked periodically to refresh state. Buffered signals will always return to their proper value after a transient interruption at either side.

Ordering Information

Part	Description
CPC5001G	8-Pin DIP in Tubes (50 / Tube)
CPC5001GS	8-Pin Surface Mount (50 / Tube)
CPC5001GSTR	8-Pin Surface Mount (1000 / Reel)

Figure 1. CPC5001 Functional Block Diagram



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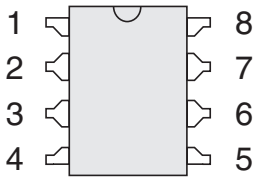
1 Specifications

1.1 Package Pinout



1.2 Pin Description

Pin#	Name	Description
1	IN1	Input, Channel 1
2	GNDA	Supply Return - Side A
3	OUT2	Output, Channel 2
4	V_{DDA}	Supply Voltage - Side A
5	IN2	Input, Channel 2
6	GNDB	Supply Return - Side B
7	OUT1	Output, Channel 1
8	V_{DDB}	Supply Voltage - Side B

1.3 Absolute Maximum Ratings

Electrical Absolute Maximum Ratings are at 25°C. Voltages with respect to local ground: GNDA or GNDB.

Parameter	Symbol	Min	Max	Units
Supply Voltage, Side A	V_{DDA}	-0.5	+6.5	V
Supply Voltage, Side B	V_{DDB}	-0.5	+6.5	V
Input Voltage	V_{IOx}	-0.3	V_{DDx} + 0.3	V
Total Package Power Dissipation [1]	P_{TOT}	-	800	mW
Isolation Voltage, Input to Output	-			V_{rms}
60 Seconds		3750	-	
2 Seconds		4500	-	
Operating Temperature	T_A	-40	+85	°C
Operating Relative Humidity (Non-condensing)	RH	5	85	%
Storage Temperature	T_{STG}	-50	+125	°C

[1] Derate total power by 7.5mW/°C above 25°C.

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 ESD Rating

ESD Rating (Human Body Model)
4000V

1.5 Thermal Characteristics

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Thermal Impedance, Junction to Ambient	Free Air	$R_{\theta JA}$	-	114	-	°C/W

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1.6 General Conditions

Unless otherwise specified, minimum and maximum values are guaranteed by production testing requirements. Typical values are characteristic of the device at 25°C, and are the result of engineering evaluations. They are provided for information purposes only, and are not part of the manufacturing testing requirements. Specifications cover the operating temperature range T_A = -40°C to +85°C, unless otherwise specified.

Side A is the same as Side B, and Channel 1 is the same as Channel 2; therefore, the electrical and timing specifications apply to both Sides/Channels.

1.7 Electrical Parametric Specifications

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Electrical						
Supply Voltage	I_{SINK}=6mA	V_{DD}	2.7	-	5.5	V
Supply Current	V_{DD}=3.3V, I_{SINK}=0mA	I_{DD}	-	4.3	-	mA
	I_{SINK}=6mA		-	4.4	-	
	V_{DD}=5.5V, I_{SINK}=0mA, T_A=25°C		-	5	7.5	
Leakage Current	IN1=OUT2=V_{DDA}, IN2=OUT1=V_{DDB}	I_{LEAK}	-	0.01	10	µA
Falling Input Low Threshold	2.7V ≤ V_{DD} ≤ 5.5V	V_{IL}	0.3V_{DD}	0.42V_{DD}	-	V
Rising Input High Threshold	2.7V ≤ V_{DD} ≤ 5.5V	V_{IH}	-	0.57V_{DD}	0.7V_{DD}	
Hysteresis	2.7V ≤ V_{DD} ≤ 5.5V	V_{HYST}	-	0.15V_{DD}	-	V
Output Drive	V_{DD}=2.7V, I_{SINK}=3mA	V_{OL}	-	0.21	0.35	V
	V_{DD}=2.7V, I_{SINK}=6mA		-	0.42	0.7	
	V_{DD}=3.3V, I_{SINK}=6mA		-	0.38	-	
Output Temperature Coefficient	2.7V ≤ V_{DD} ≤ 5.5V, I_{SINK}=6mA	TC	-	+1.2	-	mV/°C

1.8 Timing Specifications

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Timing						
Clock Frequency	I_{SINK}=6mA, C_{LOAD}=20pF	f_{MAX}	-	5	-	MHz
Propagation Delay (see Note 1)	V_{DDA}=V_{DDB}=3.3V, R_{PUA}=475Ω, R_{PUB}=475Ω C_{IN_A}=C_{IN_B}=20pF V_{IN}=0.5V_{DD_IN} to V_{OUT}=0.5V_{DD_OUT}					ns
High to Low		t_{PHL}	40	60	100	
Low to High		t_{PLH}	40	135	250	
Pulse Width Distortion	t_{PLH} - t_{PHL}	PWD	-25	75	170	ns

Note 1: See "Switching Waveforms" on page 5.

1.9 Common Mode Rejection Specifications

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Common Mode Rejection						
Common Mode Transient Immunity	V_{CM}=20V_{P-P} , V_{DD}=3.3V, T_A=25°C					
V_{OUT} = High	V_{OUT}>2V	CM_H	5	-	-	kV/µs
V_{OUT} = Low	V_{OUT}<0.8V	CM_L	7	-	-	

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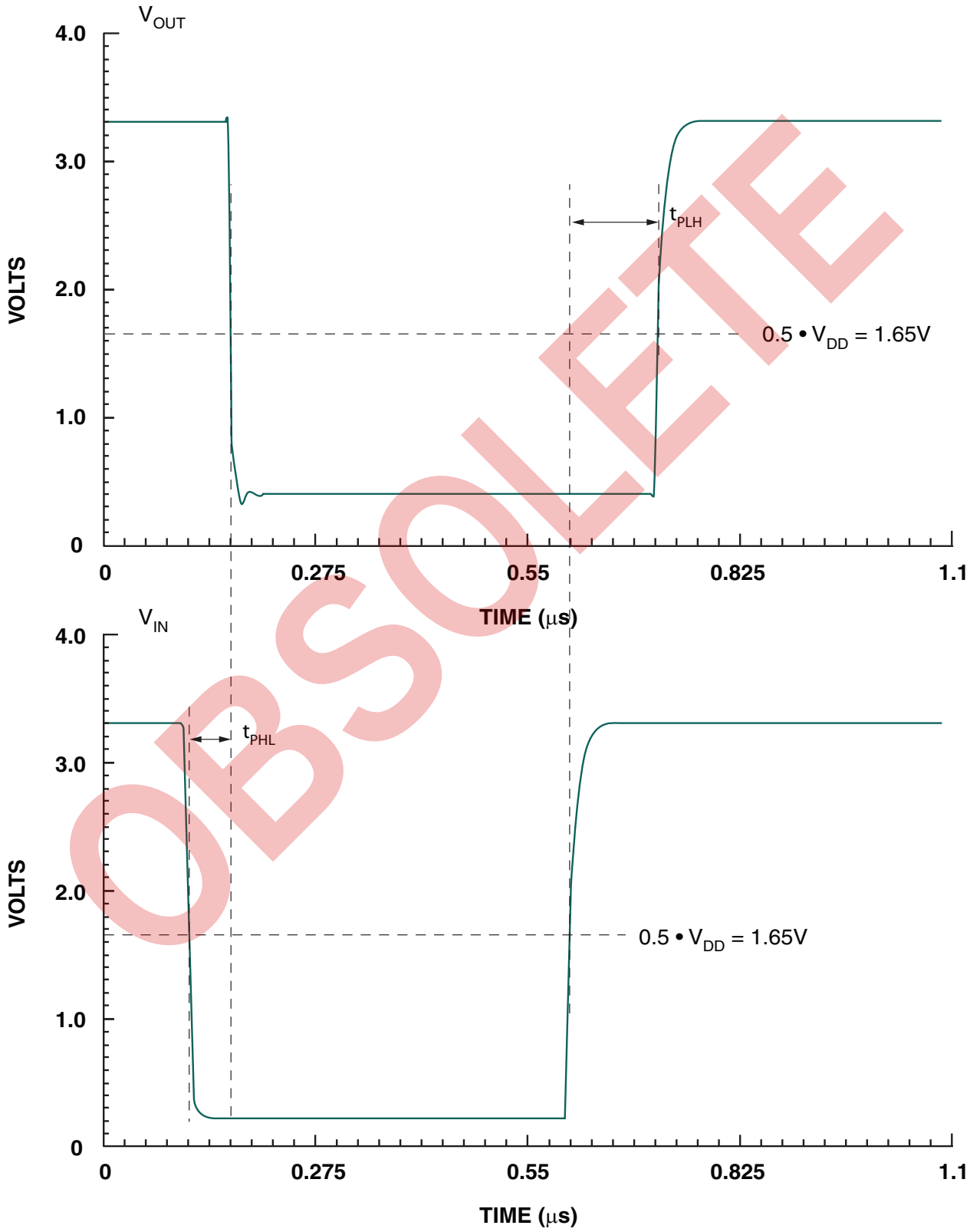
2 Switching Waveforms



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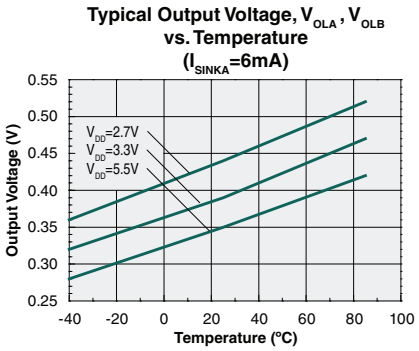
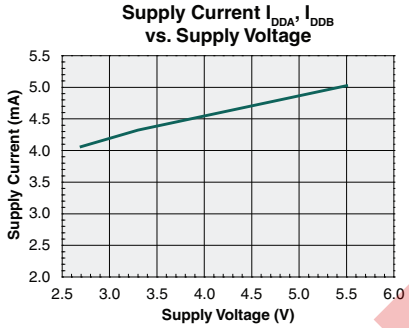
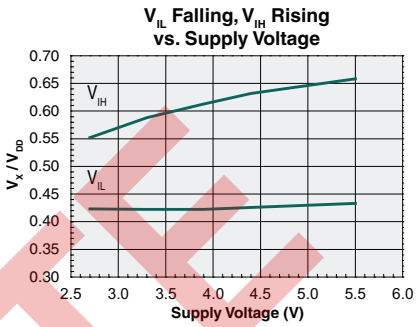
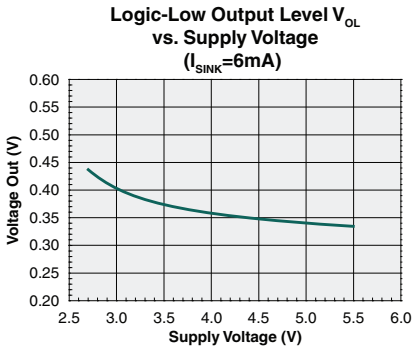
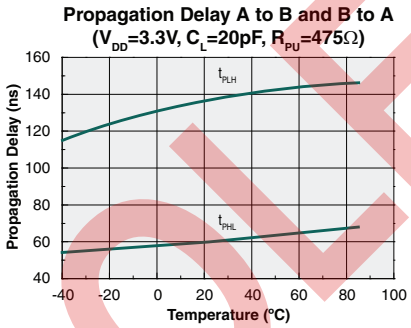
3 Performance Data*

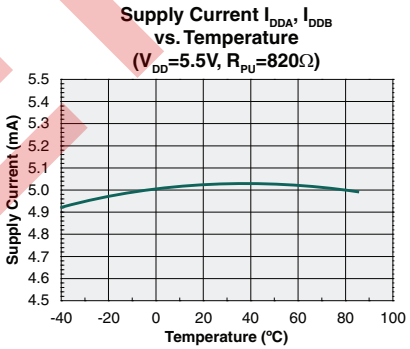












*Unless otherwise noted, data presented in these graphs is typical of device operation at 25°C.
For guaranteed parameters not indicated in the written specifications, please contact our applications department.

4 Functional Description

4.1 Introduction

The CPC5001 combines the functions of two input buffer/LED driver gates and two unidirectional logic optoisolators in a single 8-pin package. The isolators are arranged for one input and one output at each side of the isolation barrier, which enables Channel 1 to send signals from side A to Side B, and Channel 2 to send signals from the Side B to the Side A. If different supply voltage levels are used at each side, then the part, in conjunction with its external pullup resistors, will perform logic level translation for V_{DD} between 2.7V and 5.5V at either side.

The part provides galvanic isolation for voltages up to 3750V_{rms}. Its CMOS circuitry includes a bandgap reference to ensure that the LEDs receive consistent drive current levels over the allowed range of V_{DD} voltages. The supply currents at I_{DDA} and I_{DDB} are much smaller than those required by bipolar solutions, and are stable over temperature. The circuits also ensure that the I_{DD} current into each V_{DD} package pin remains constant for both high and low input signals. This can greatly reduce the size of external decoupling capacitors when compared with optoisolators fabricated in a bipolar process wherein the supply current can double when the LED is on.

The rotationally symmetric pinout ensures that the part operates normally even if installed with 180° rotation.

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5 Manufacturing Information

5.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Integrated Circuits classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
CPC5001GS	MSL 1

5.2 ESD Sensitivity

This product is ESD Sensitive, and should be handled according to the industry standard **JESD-625**.

5.3 Soldering Profile

Provided in the table below is the **IPC/JEDEC J-STD-020** Classification Temperature (T_C) and the maximum total dwell time (t_P) in all reflow processes that the body temperature of these surface mount devices may be (T_C - 5)°C or greater. The device's body temperature must not exceed the Classification Temperature at any time during reflow soldering processes.

Device	Classification Temperature (T_C)	Dwell Time (t_p)	Max Reflow Cycles
CPC5001GS	250°C	30 seconds	3

For through-hole devices, the maximum pin temperature and maximum dwell time through all solder waves is provided in the table below. Dwell time is the interval beginning when the pins are initially immersed into the solder wave until they exit the solder wave. For multiple waves, the dwell time is from entering the first wave until exiting the last wave. During this time, pin temperatures must not exceed the maximum temperature given in the table below. Body temperature of the device must not exceed the limit shown in the table below at any time during the soldering process.

Device	Maximum Pin Temperature	Maximum Body Temperature	Maximum Dwell Time	Max Reflow Cycles
CPC5001G	260°C	250°C	10 seconds*	1

*Total cumulative duration of all waves.

5.4 Board Wash

IXYS Integrated Circuits recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to halide flux or solvents.

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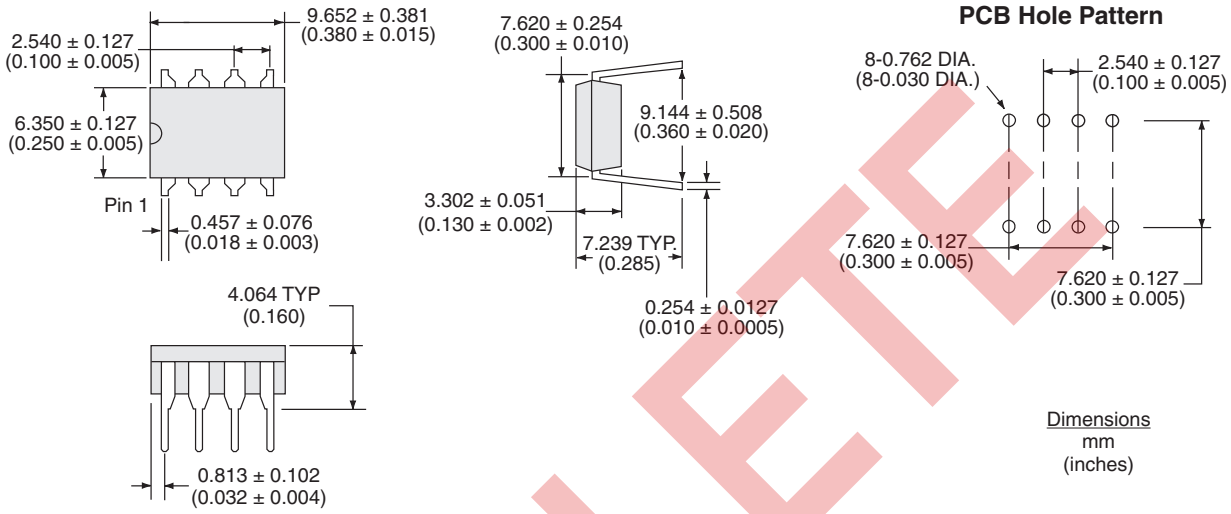
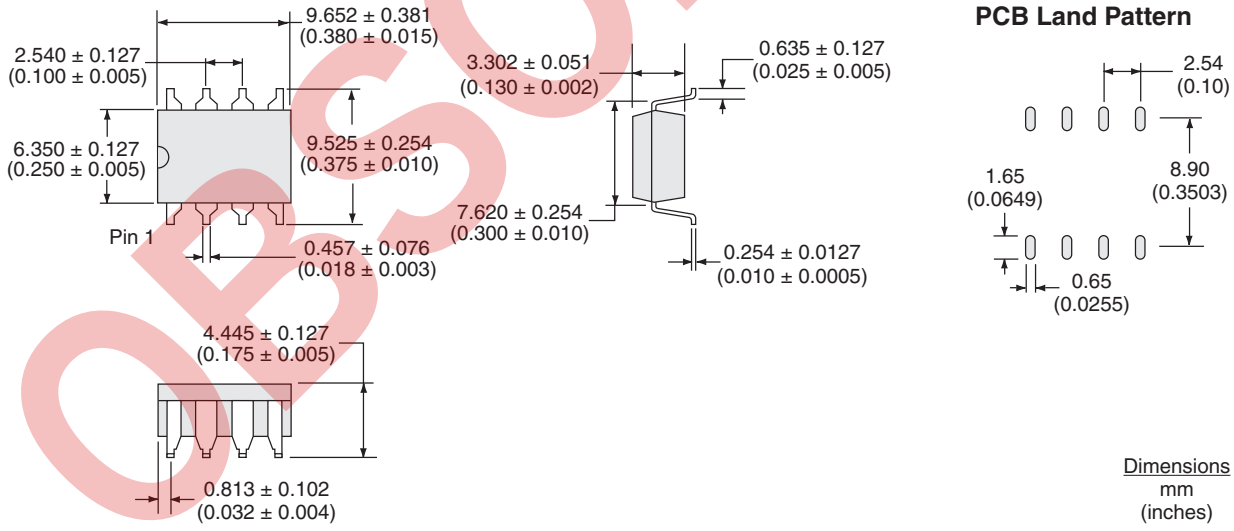
5.5 Mechanical Dimensions

5.5.1 CPC5001G Package



5.5.2 CPC5001GS Package



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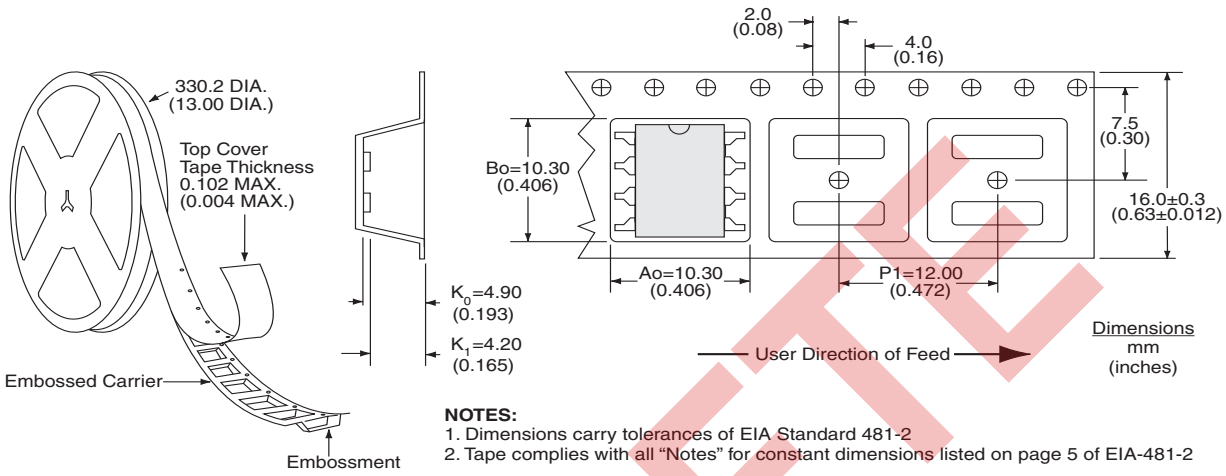
5.5.3 CPC5001GS Tape & Reel Information



NOTES:
1. Dimensions carry tolerances of EIA Standard 481-2
2. Tape complies with all "Notes" for constant dimensions listed on page 5 of EIA-481-2

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For additional information please visit our website at: https://www.ixysic.com

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