

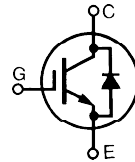
High Voltage, High Gain BIMOSFET™ Monolithic Bipolar MOS Transistor

IXBF22N300

$$V_{CES} = 3000V$$

$$I_{C90} = 22A$$

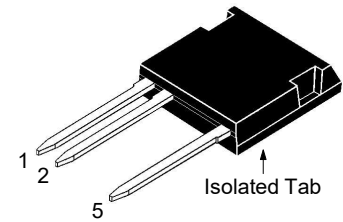
$$V_{CE(sat)} \leq 2.7V$$



(Electrically Isolated Tab)

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	$T_J = 25^\circ C$ to $150^\circ C$	3000	V
V_{CGR}	$T_J = 25^\circ C$ to $150^\circ C$, $R_{GE} = 1M\Omega$	3000	V
V_{GES}	Continuous	± 20	V
V_{GEM}	Transient	± 30	V
I_{C25}	$T_C = 25^\circ C$	38	A
I_{C90}	$T_C = 90^\circ C$	22	A
I_{CM}	$T_C = 25^\circ C$, 1ms	165	A
SSOA (RBSOA)	$V_{GE} = 15V$, $T_{VJ} = 125^\circ C$, $R_G = 15\Omega$ Clamped Inductive Load	$I_{CM} = 180$ $V_{CES} \leq 1500$	A V
T_{SC} (SCSOA)	$V_{GE} = 15V$, $T_J = 125^\circ C$, $R_G = 52\Omega$, $V_{CE} = 1500V$, Non-Repetitive	10	μs
P_C	$T_C = 25^\circ C$	150	W
T_J		-55 ... +150	$^\circ C$
T_{JM}		150	$^\circ C$
T_{stg}		-55 ... +150	$^\circ C$
T_L	Maximum Lead Temperature for Soldering 1.6 mm (0.062 in.) from Case for 10s	300	$^\circ C$
F_C	Mounting Force	20..120 / 4.5..27	N/lb
V_{ISOL}	50/60Hz, 5 Seconds	4000	V~
Weight		5	g

ISOPLUS i4-Pak™



1 = Gate
2 = Emitter
5 = Collector

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 4000V~ Electrical Isolation
- High Blocking Voltage
- High Peak Current Capability
- Low Saturation Voltage

Advantages

- Low Gate Drive Requirement
- High Power Density

Applications

- Switch-Mode and Resonant-Mode Power Supplies
- Uninterruptible Power Supplies (UPS)
- Laser Generators
- Capacitor Discharge Circuits
- AC Switches

Symbol	Test Conditions ($T_J = 25^\circ C$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$	3000		V
$V_{GE(th)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	3.0		5.0 V
I_{CES}	$V_{CE} = V_{CES}$, $V_{GE} = 0V$ Note 2, $T_J = 125^\circ C$			35 μA 1.5 mA
I_{GES}	$V_{CE} = 0V$, $V_{GE} = \pm 20V$			± 100 nA
$V_{CE(sat)}$	$I_C = 22A$, $V_{GE} = 15V$, Note 1 $T_J = 125^\circ C$		2.2 2.7	2.7 V V

Symbol Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)		Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$I_C = 22\text{A}, V_{CE} = 10\text{V}$, Note 1	13	22	S
C_{ies}	$V_{CE} = 25\text{V}, V_{GE} = 0\text{V}, f = 1\text{MHz}$		2200	pF
C_{oes}			85	pF
C_{res}			30	pF
Q_g	$I_C = 22\text{A}, V_{GE} = 15\text{V}, V_{CE} = 1500\text{V}$		110	nC
Q_{ge}			13	nC
Q_{gc}			45	nC
$t_{d(on)}$	Resistive Switching Times, $T_J = 25^\circ\text{C}$ $I_C = 22\text{A}, V_{GE} = 15\text{V}$ $V_{CE} = 960\text{V}, R_G = 15\Omega$		46	ns
t_r			360	ns
$t_{d(off)}$			205	ns
t_f			1820	ns
$t_{d(on)}$	Resistive Switching Times, $T_J = 125^\circ\text{C}$ $I_C = 22\text{A}, V_{GE} = 15\text{V}$ $V_{CE} = 960\text{V}, R_G = 15\Omega$		43	ns
t_r			700	ns
$t_{d(off)}$			220	ns
t_f			1650	ns
R_{thJC}				0.83 °C/W
R_{thCS}		0.15		°C/W

Reverse Diode

Symbol Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)		Characteristic Values		
		Min.	Typ.	Max.
V_F	$I_F = 22\text{A}, V_{GE} = 0\text{V}$, Note 1			2.7 V
t_{rr}	$I_F = 11\text{A}, V_{GE} = 0\text{V}, -di_F/dt = 100\text{A}/\mu\text{s}$ $V_R = 100\text{V}, V_{GE} = 0\text{V}$		1.4	μs
I_{RM}			30	A
Q_{RM}			21	μC

Notes:

1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.
2. Device must be heatsunk for high temperature leakage current measurements to avoid thermal runaway.

Additional provisions for lead-to-lead voltage isolation are required at $V_{CE} > 1200\text{V}$.

Littelfuse reserves the right to change limits, test conditions and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
	4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

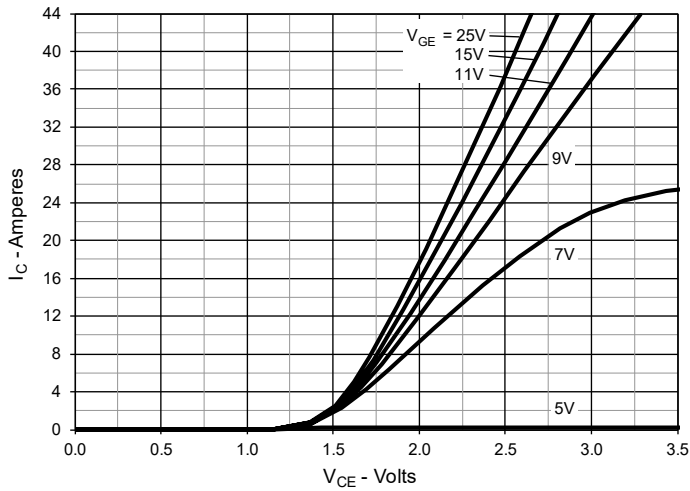


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

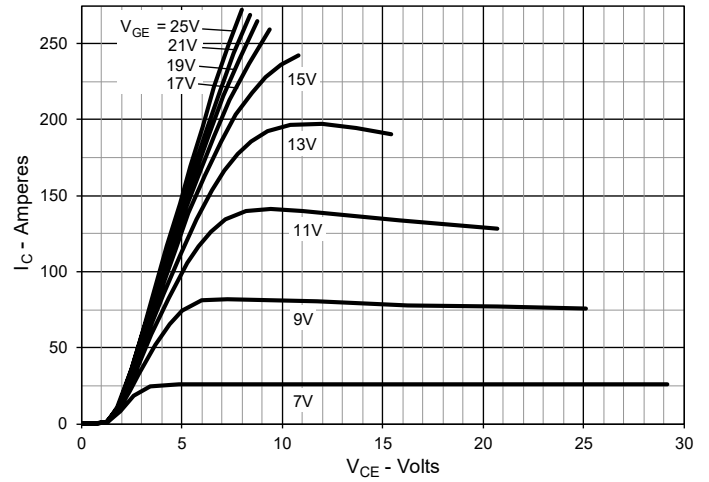


Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

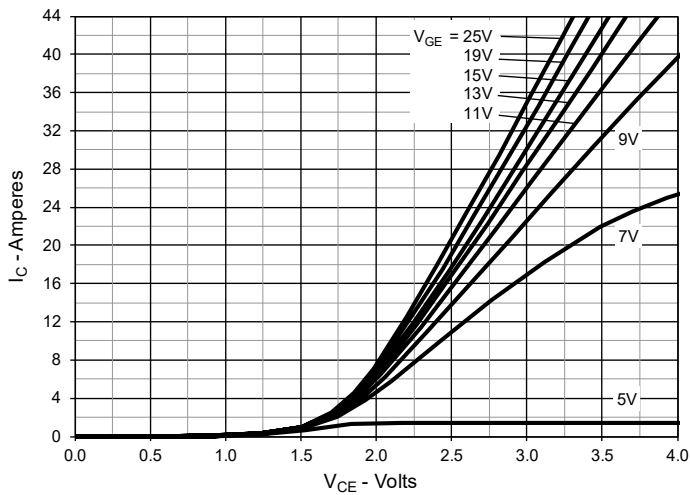


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

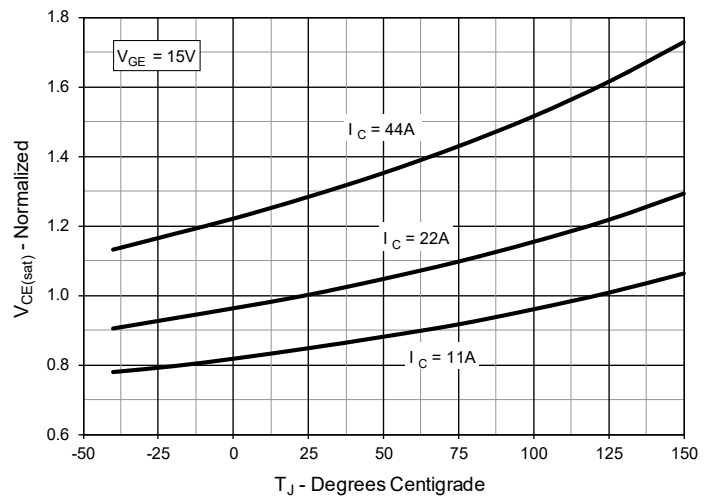


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

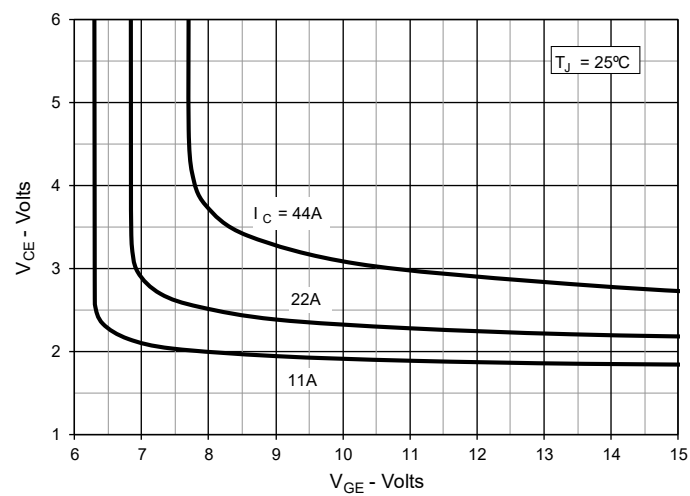


Fig. 6. Input Admittance

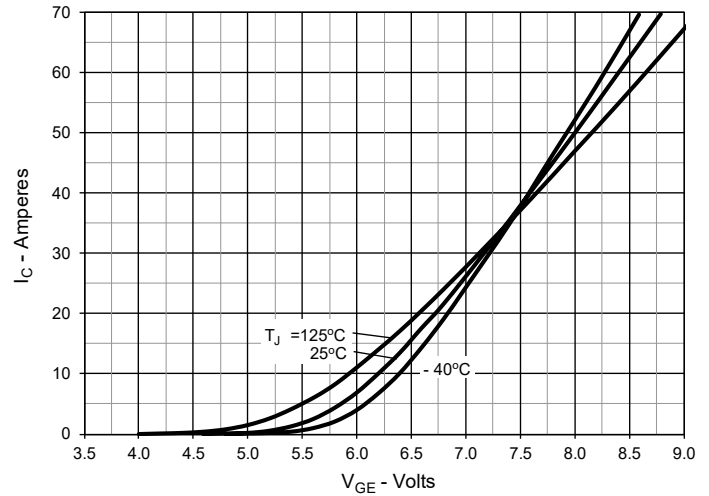


Fig. 7. Transconductance

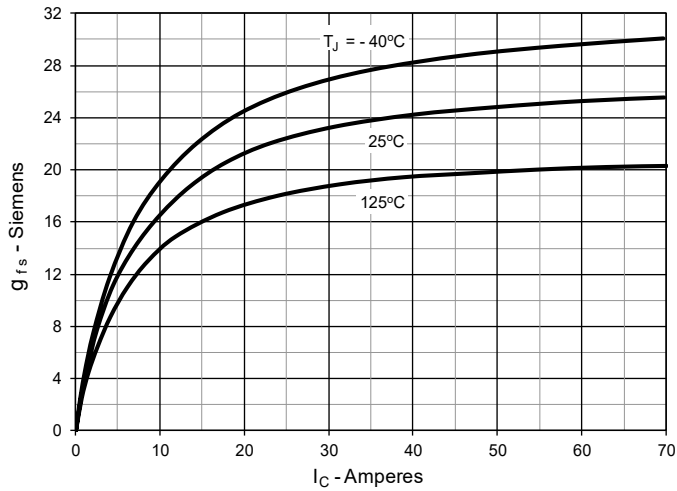


Fig. 8. Gate Charge

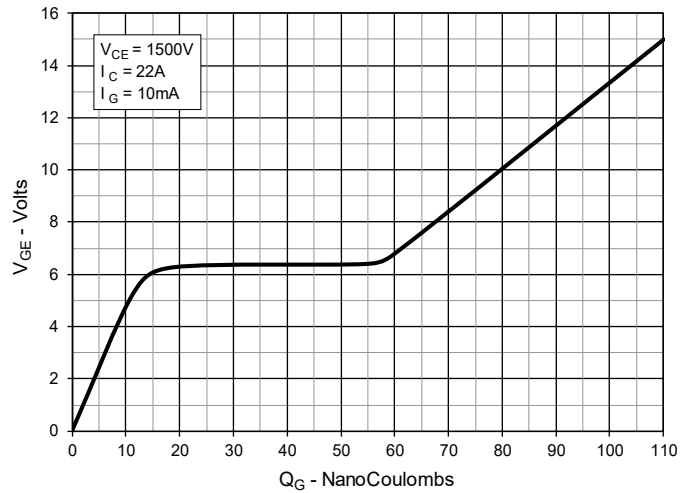


Fig. 9. Forward Voltage Drop of Intrinsic Diode

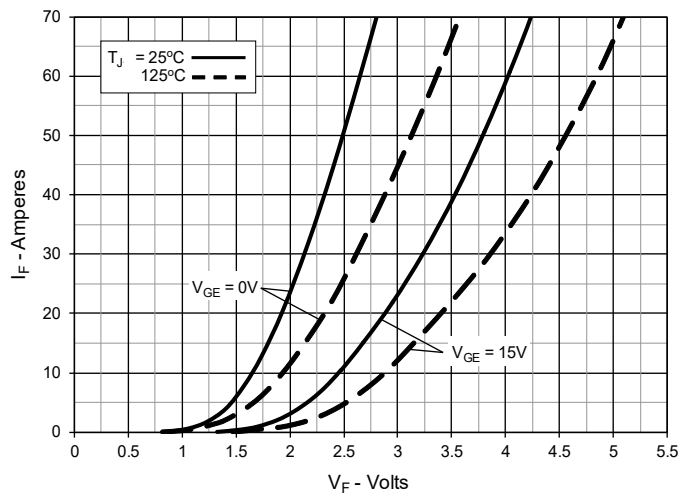


Fig. 10. Capacitance

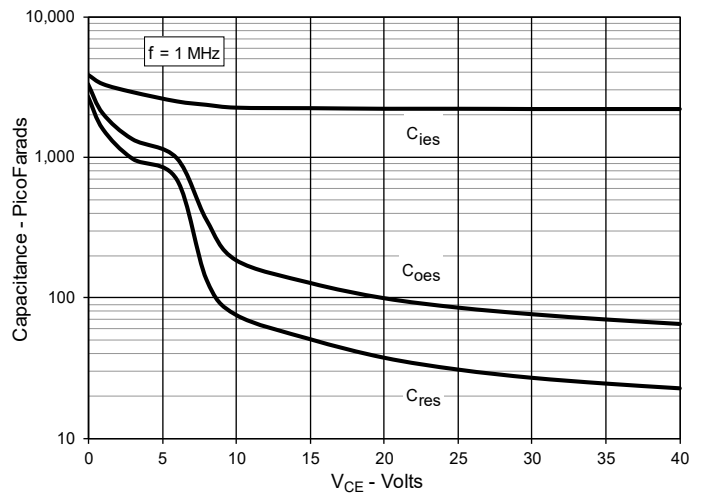


Fig. 11. Reverse-Bias Safe Operating Area

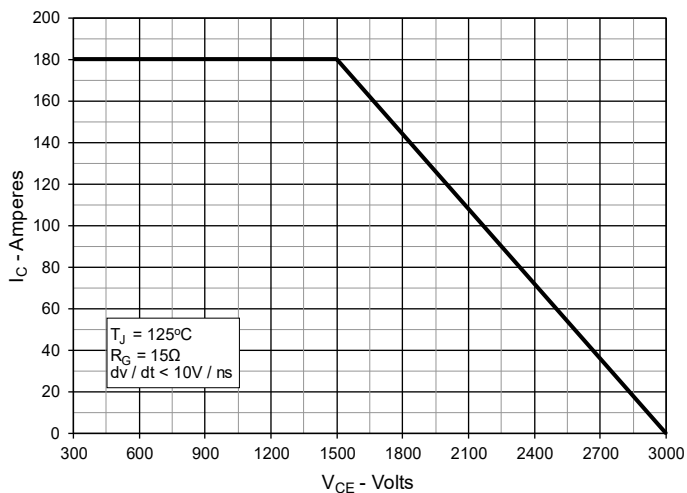


Fig. 12. Maximum Transient Thermal Impedance

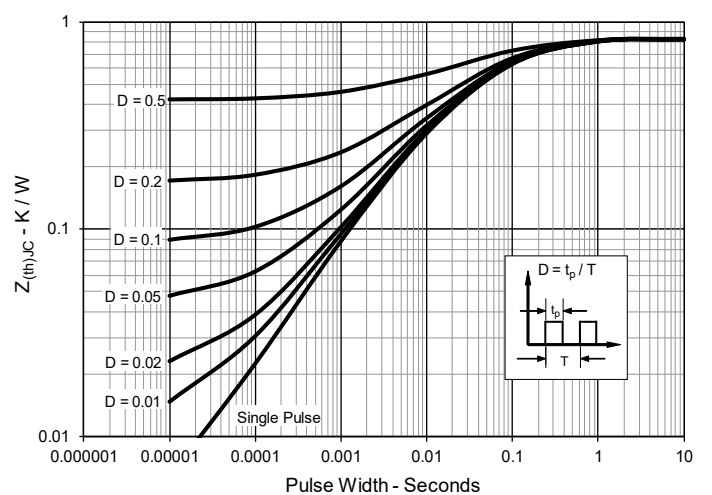


Fig. 13. Forward-Bias Safe Operating Area @ $T_C = 25^\circ\text{C}$

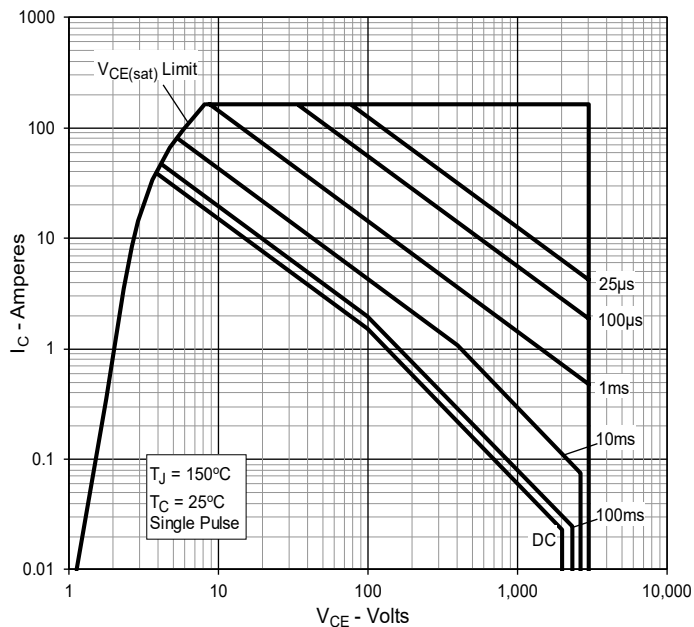
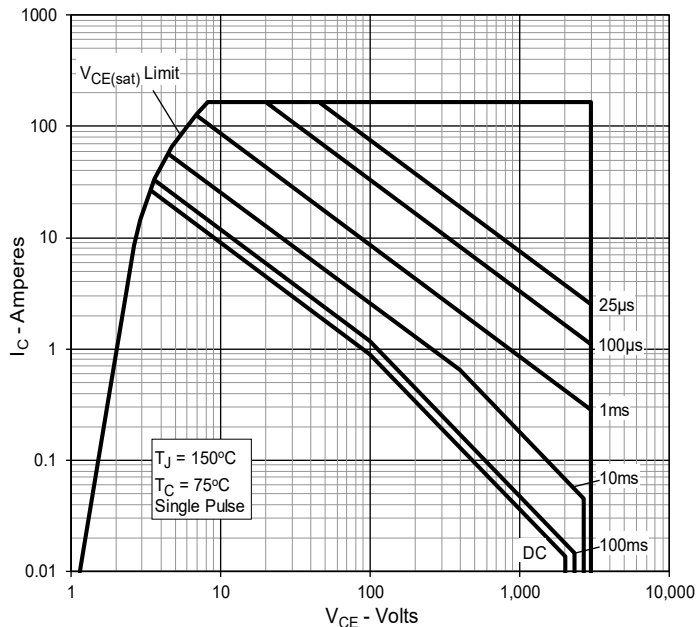
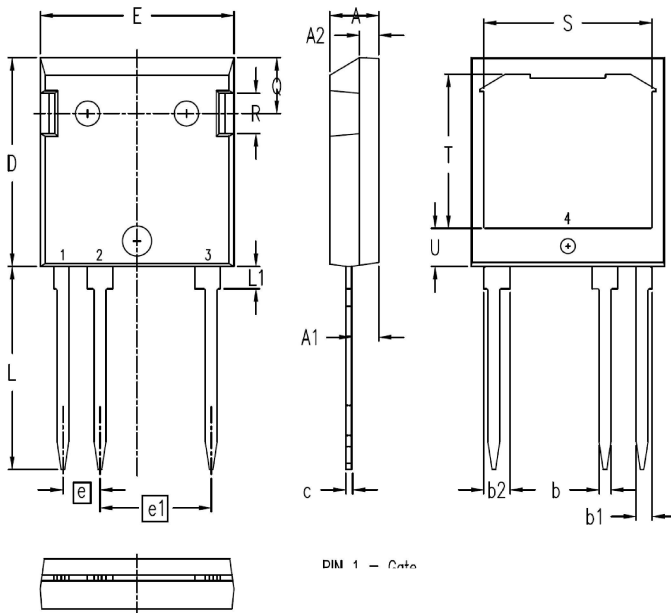


Fig. 14. Forward-Bias Safe Operating Area @ $T_C = 75^\circ\text{C}$



ISOPLUS i4-Pak Outline


- 1 = Gate**
- 2 = Emitter**
- 3,4 = Colector**

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.193	.201	4.90	5.10
A1	.106	.114	2.70	2.90
A2	.075	.083	1.90	2.10
b	.047	.055	1.20	1.40
b1	.061	.069	1.55	1.75
b2	.087	.094	2.20	2.40
c	.020	.029	0.51	0.74
D	.819	.846	20.80	21.50
E	.768	.799	19.50	20.30
e	.150 BSC		3.81 BSC	
e1	.450 BSC		11.43 BSC	
L	.780	.838	19.80	21.30
L1	.083	.094	2.10	2.40
Q	.213	.236	5.40	6.00
R	.157	.169	4.00	4.30
S	.673	.685	17.10	17.40
T	.602	.614	15.30	15.60
U	.142	.154	3.60	3.90