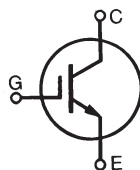


High Voltage IGBT

IXGL75N250

For Capacitor Discharge Applications

(Electrically Isolated Tab)



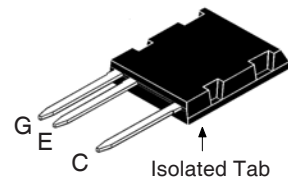
$$V_{CES} = 2500V$$

$$I_{C90} = 65A$$

$$V_{CE(sat)} \leq 2.9V$$

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	$T_J = 25^\circ C$ to $150^\circ C$	2500	V
V_{CES}	$T_J = 25^\circ C$ to $150^\circ C$, $R_{GE} = 1M\Omega$	2500	V
V_{GES}	Continuous	± 20	V
V_{GEM}	Transient	± 30	V
I_{C25}	$T_C = 25^\circ C$	110	A
I_{C90}	$T_C = 90^\circ C$	65	A
I_{CM}	$T_C = 25^\circ C$, $V_{GE} = 20V$, 1ms	580	A
SSOA	$V_{GE} = 15V$, $T_{VJ} = 125^\circ C$, $R_G = 1\Omega$	$I_{CM} = 200$	A
(RBSOA)	Clamped Inductive Load	$V_{CE} \leq 0.8 \cdot V_{CES}$	
P_C	$T_C = 25^\circ C$	430	W
T_J		-55 ... +150	$^\circ C$
T_{JM}		150	$^\circ C$
T_{stg}		-55 ... +150	$^\circ C$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ C$
T_{SOLD}	1.6 mm (0.062 in.) from Case for 10s	260	$^\circ C$
V_{ISOL}	50/60Hz, 1 minute	2500	V~
F_C	Mounting Force with Clip	30..170 / 7..36	Nm/lb-in.
Weight		8	g

ISOPLUS i5-Pak™



G = Gate C = Collector
E = Emitter

Features

- Very High Peak Current Capability
- Low Saturation Voltage
- MOS Gate Turn-On
- Rugged NPT Structure
- ISOPLUS i5-PAK™ High Voltage Package
 - Isolated Back Surface
 - Enlarged Creepage Towards Heat-Sink
 - Enlarged Creepage between High Voltage Pins
 - Application Friendly PinOut
 - High Reliability
 - Industry Standard Outline
 - UL Registered

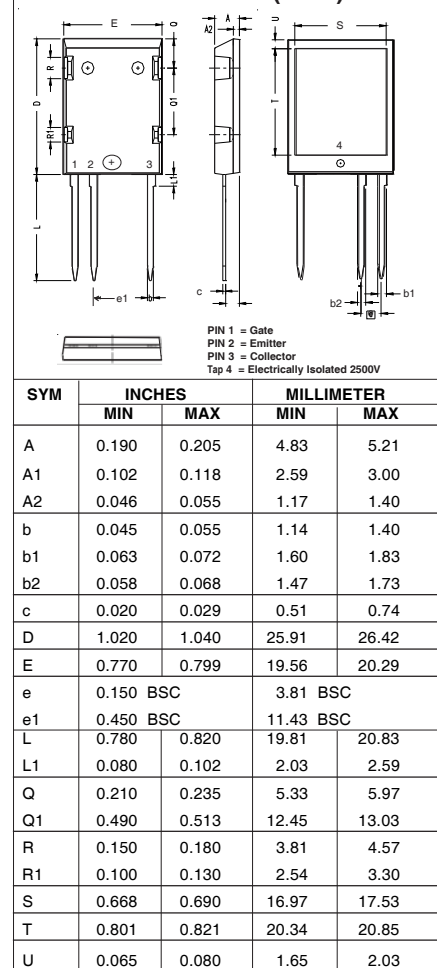
Applications

- Capacitor Discharge
- Pulser Circuits

Symbol	Test Conditions ($T_J = 25^\circ C$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{CES}	$I_C = 1mA$, $V_{GE} = 0V$	2500		V
$V_{GE(th)}$	$I_C = 4mA$, $V_{CE} = V_{GE}$	3.0		5.0 V
I_{CES}	$V_{CE} = 0.8 \cdot V_{CES}$, $V_{GE} = 0V$ Note 2, $T_J = 125^\circ C$			50 μA 5 mA
I_{GES}	$V_{CE} = 0V$, $V_{GE} = \pm 20V$			± 200 nA
$V_{CE(sat)}$	$I_C = 75A$, $V_{GE} = 15V$, Note 1		2.5	2.9 V
	$I_C = 300A$, $V_{GE} = 25V$		4.1	V

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$I_C = 60\text{A}$, $V_{CE} = 10\text{V}$, Note 1	35	58	S
C_{ies}	$V_{CE} = 25\text{V}$, $V_{GE} = 0\text{V}$, $f = 1\text{MHz}$		9000	pF
C_{oes}			345	pF
C_{res}			110	pF
Q_g	$I_C = 75\text{A}$, $V_{GE} = 15\text{V}$, $V_{CE} = 0.5 \cdot V_{CES}$		410	nC
Q_{ge}			63	nC
Q_{gc}			175	nC
$t_{d(on)}$	Resistive Switching Times		55	ns
t_r	$I_C = 150\text{A}$, $V_{GE} = 15\text{V}$		225	ns
$t_{d(off)}$	$V_{CE} = 1250\text{V}$, $R_G = 1\Omega$		270	ns
t_f			455	ns
R_{thJC}				0.29°C/W
R_{thCK}		0.15		$^\circ\text{C/W}$

ISOPLUS i5-Pak™ HV (IXGL) Outline



Notes:

1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.
2. Part must be heatsunk for high-temp I_{ces} measurement.

PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

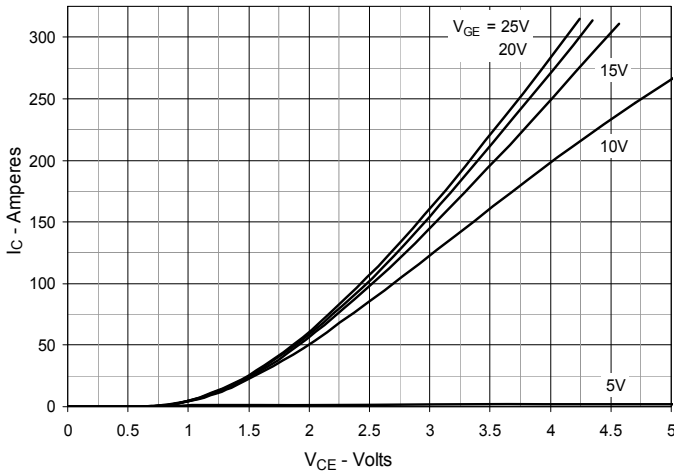


Fig. 2. Output Characteristics @ $T_J = 125^\circ\text{C}$

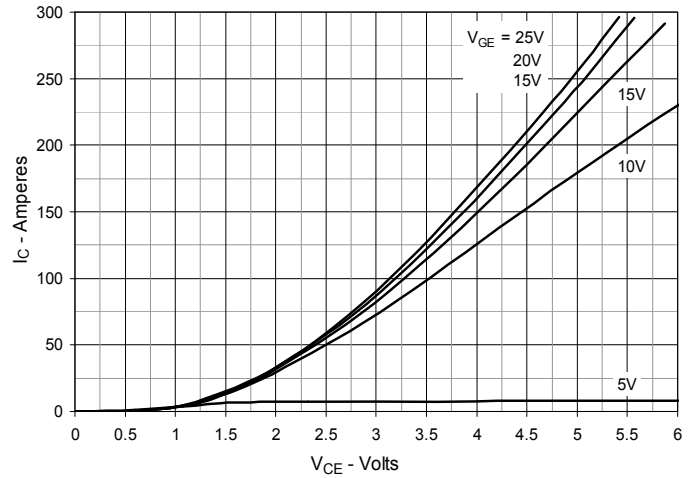


Fig. 3. Dependence of $V_{CE(sat)}$ on Junction Temperature

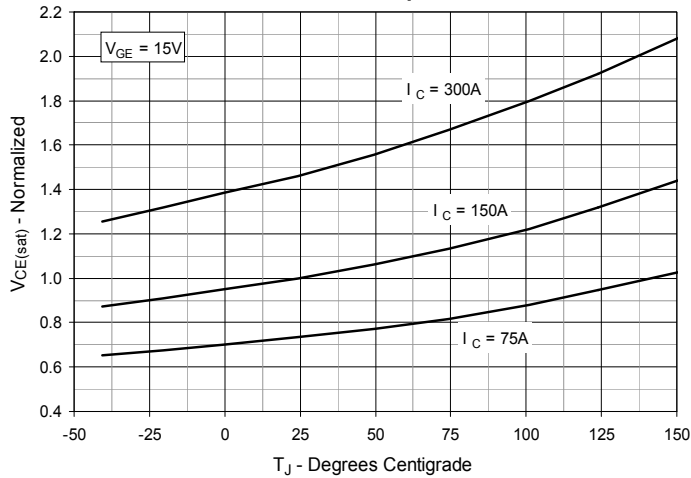


Fig. 4. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

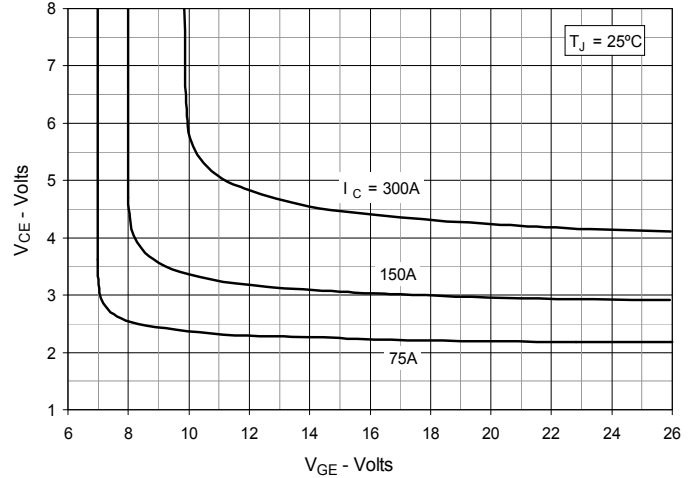


Fig. 5. Input Admittance

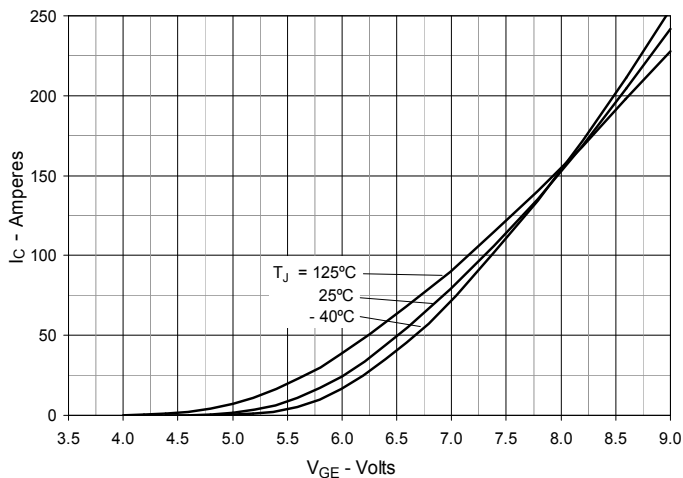


Fig. 6. Transconductance

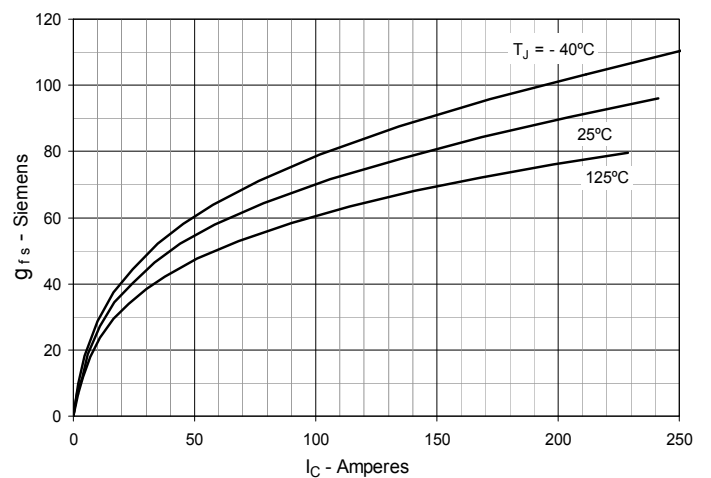


Fig. 7. Gate Charge

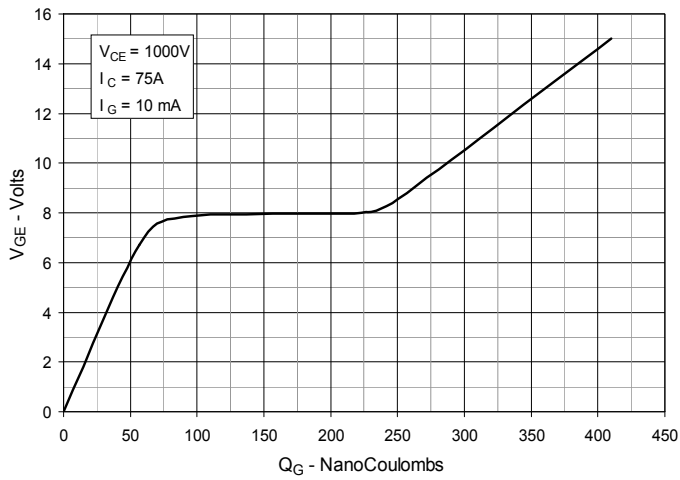


Fig. 8. Capacitance

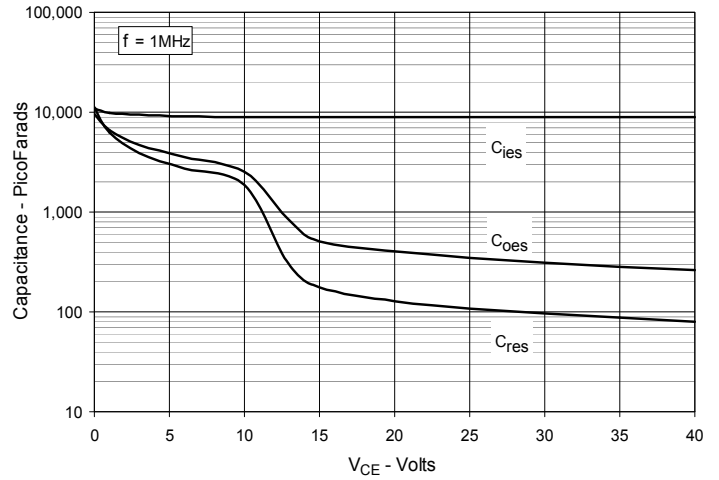


Fig. 9. Reverse-Bias Safe Operating Area

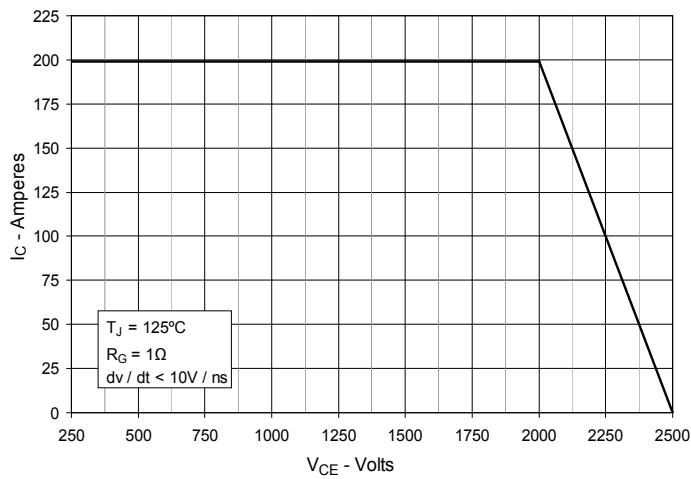


Fig. 10. Maximum Transient Thermal Impedance

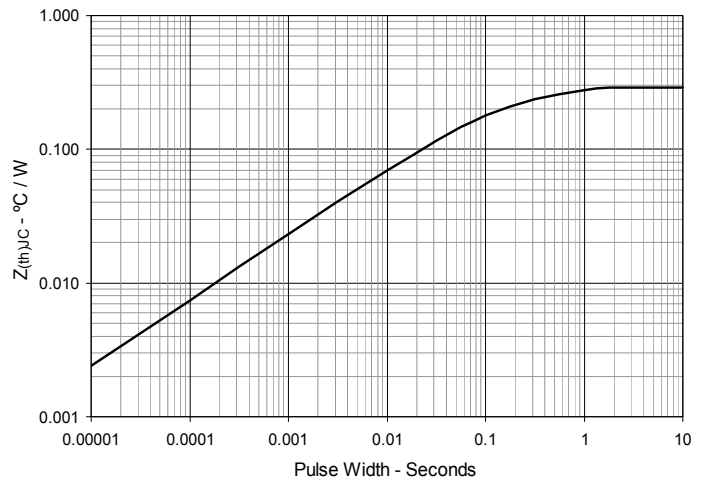


Fig. 11. Resistive Turn-on Rise Time vs. Junction Temperature

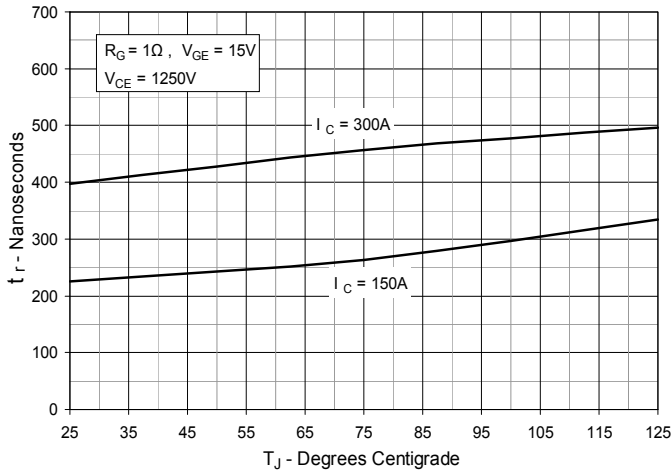


Fig. 12. Resistive Turn-on Rise Time vs. Collector Current

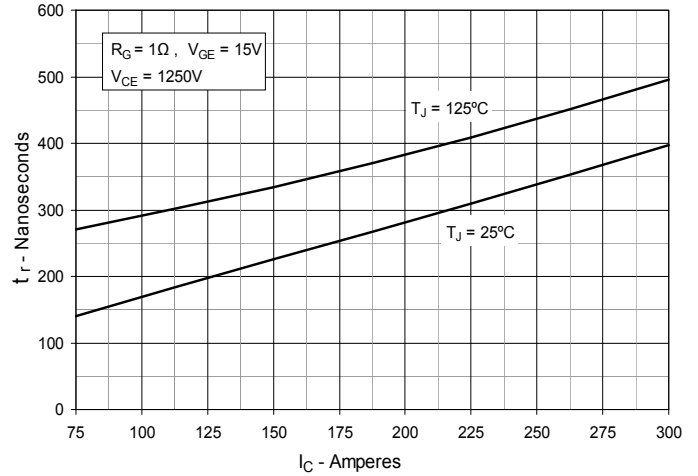


Fig. 13. Resistive Turn-on Switching Times vs. Gate Resistance

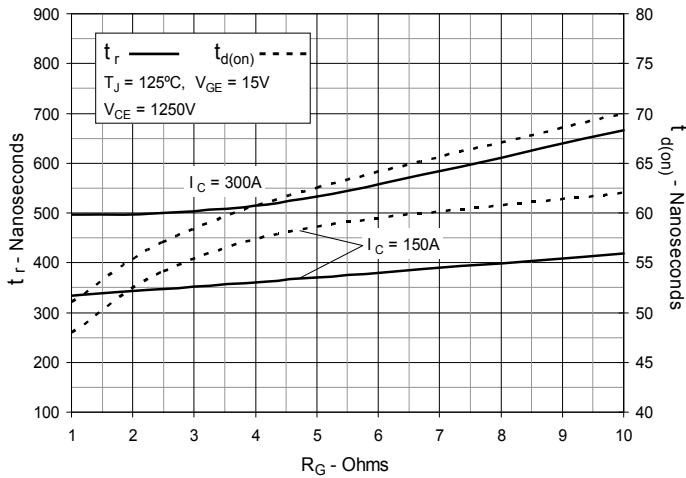


Fig. 14. Resistive Turn-off Switching Times vs. Junction Temperature

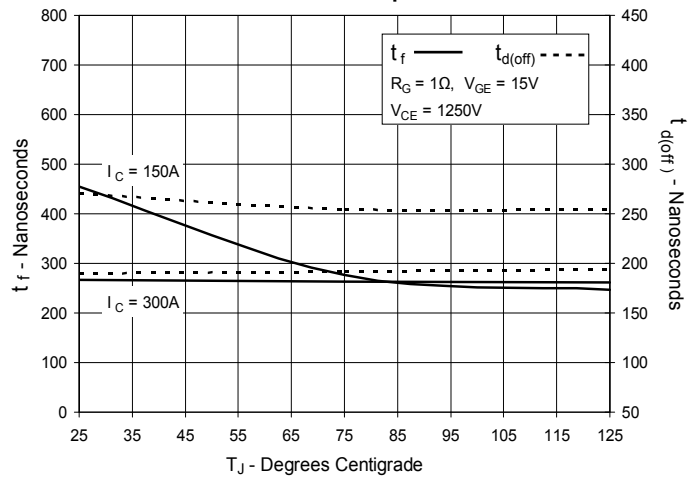


Fig. 15. Resistive Turn-off Switching Times vs. Collector Current

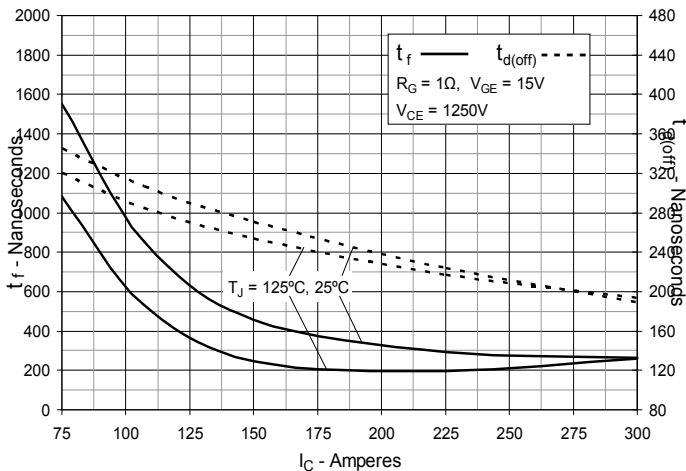
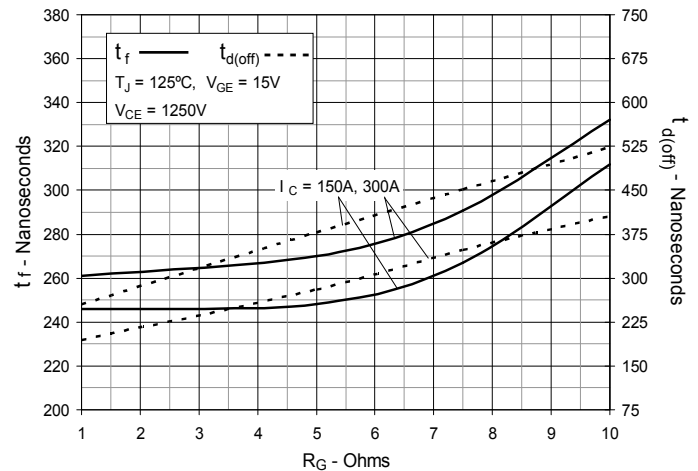


Fig. 16. Resistive Turn-off Switching Times vs. Gate Resistance





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