High Voltage Power MOSFET

N-Channel Enhancement Mode
Fast Intrinsic Diode
$\mathrm{V}_{\text {DSs }}=2500 \mathrm{~V}$
$\mathrm{I}_{\mathrm{D} 25}=1.4 \mathrm{~A}$
$\mathrm{R}_{\mathrm{DS}(\text { (n) })} \leq 28 \Omega$

TO-247 (IXTH)

$\mathrm{G}=$ Gate $\quad \mathrm{D}=$ Drain
S = Source $\quad$ Tab $=$ Drain

## Features

- High Blocking Voltage
- Fast Intrinsic Diode
- Low Package Inductance


## Advantages

- Easy to Mount
- Space Savings
- High Power Density



## Applications

- High Voltage Power Supplies
- Capacitor Discharge Applications
- Pulse Circuits
- Laser and X-Ray Generation Systems



## Source-Drain Diode



| TO-247 Outline |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |
| Dim. | ${ }_{\text {min }}^{\text {mili }}$ | max | min |  |
| A | 4.70 | 5.30 | 0.185 | 0.209 |
| A2 | ${ }_{2}^{2.21} 1.50$ | ${ }_{2}^{2.59}$ | 0.087 | 0.10 |
| ${ }_{\text {A2 }}$ | ${ }^{1.50} 0$ | ${ }_{1.40}^{2.49}$ | ${ }_{0}^{0.059}$ | (0.098 |
| ${ }^{\text {b2 }}$ | ${ }^{1.65}$ | ${ }^{2} .39$ | 0.006 | 0.094 |
| ${ }^{\text {b4 }}$ | 2.59 | ${ }^{3.43}$ | 0.102 | 0.135 |
|  | ${ }^{0.38}$ | 0.89 | 0.015 | 0.035 |
| D | ${ }^{20.79}$ | 21.45 | 0.819 | 0.845 |
| $\mathrm{D}_{2}$ | 0.51 | 1.35 | 0.020 | 0.053 |
| E | 15.48 | 16.24 | 0.610 | 0.640 |
| ${ }_{\text {E }}$ | 13.45 |  | 0.53 |  |
| $\stackrel{\text { E2 }}{\text { E }}$ | ${ }_{4.35}^{4.45}$ |  | ${ }_{0}^{0.170} 0$ | ${ }_{\text {BSC }}^{0.216}$ |
| L | 19.80 | 20.30 | 0.078 | 0.800 |
| ${ }_{\text {OP }}$ | 3.55 | ${ }_{3.49}^{4.49}$ | 0.140 | ${ }_{0}^{0.144}$ |
| ${ }^{\text {op }}$ |  | 7.39 |  | 0.290 |
| $\stackrel{\square}{\text { a }}$ | ${ }_{6.38}^{5.14}$ |  | 0.212 0.24 | ${ }_{\text {BSC }}^{0.244}$ |

Notes: 1. Pulse test, $\mathrm{t} \leq 300 \mu \mathrm{~s}$, duty cycle, $\mathrm{d} \leq 2 \%$.
2. Additional provisions for lead-to-lead voltage isolation are required at $V_{D S}>1200 \mathrm{~V}$.

## ADVANCE TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

Fig. 1. Output Characteristics @ $\mathrm{T}_{\mathbf{J}}=\mathbf{2 5}^{\circ} \mathrm{C}$


Fig. 3. $\mathrm{R}_{\mathrm{DS}(\mathrm{on})}$ Normalized to $\mathrm{I}_{\mathrm{D}}=0.7 \mathrm{~A}$ Value vs. Junction Temperature


Fig. 5. Maximum Drain Current vs.
Case Temperature


Fig. 2. Output Characteristics $@ \mathrm{~T}_{\mathrm{J}}=125^{\circ} \mathrm{C}$


Fig. 4. $\mathrm{R}_{\mathrm{DS}(\mathrm{on})}$ Normalized to $\mathrm{I}_{\mathrm{D}}=0.7 \mathrm{~A}$ Value vs. Drain Current


Fig. 6. Input Admittance
 IXTH1R4N250P3

Fig. 7. Transconductance


Fig. 9. Gate Charge


Fig. 8. Forward Voltage Drop of Intrinsic Diode


Fig. 10. Capacitance


Fig. 11. Maximum Transient Thermal Impedance


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Fig. 12. Forward-Bias Safe Operating Area


Fig. 13. Forward-Bias Safe Operating Area


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