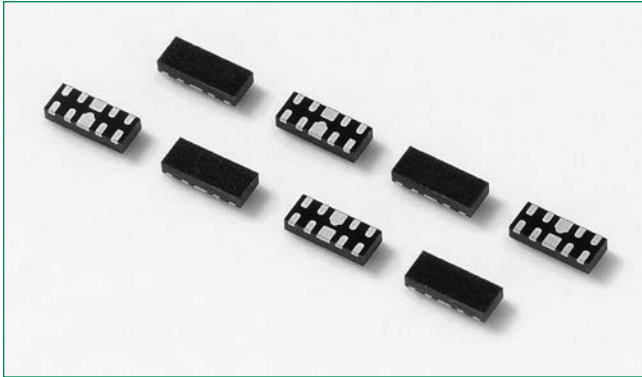
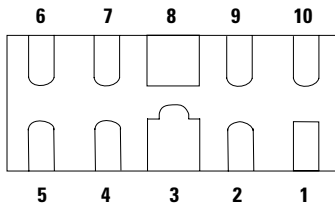


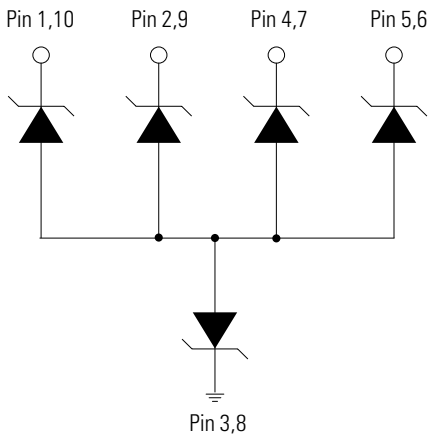
SP1064 Series 8.5pF, 15 kV Diode Array



Pinout



Functional Block Diagram



Description

The SP1064 is an avalanche breakdown diode fabricated in a proprietary silicon avalanche technology protect each I/O pin to provide a high level of protection for electronic equipment that may experience destructive electrostatic discharges (ESD). These robust diodes can safely absorb repetitive ESD strikes above the maximum level specified in IEC 61000-4-2 international standard (Level 4, ±8kV contact discharge) without performance degradation. Their very low loading capacitance also makes them ideal for protecting high speed signal pins.

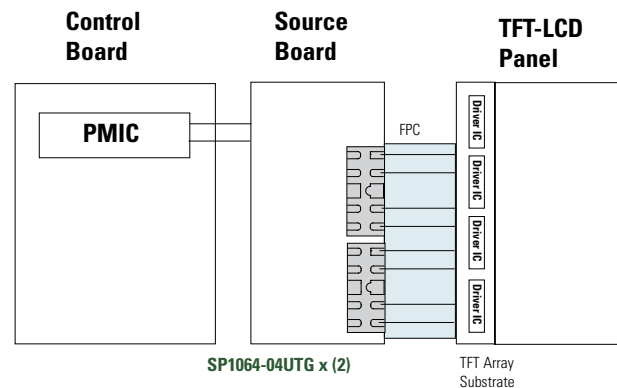
Features

- ESD, IEC 61000-4-2, ±15kV contact, ±20kV air
- EFT, IEC 61000-4-4, 40A (5/50ns)
- Lightning, 2A (8/20µs as defined in IEC 61000-4-5, 2nd Edition)
- Low capacitance of 8.5pF (TYP) per I/O
- Low leakage current of 0.05µA (TYP) at 60V
- Small form factor µDFN(JEDEC MO-229) package saves board space
- Lead free and RoHS compliant
- AEC-Q101 qualified

Applications

- LCD/PDP TVs
- DVD Players
- Desktops
- MP3/PMP
- Set Top Boxes
- Mobile Phones
- Notebooks
- Digital Cameras

Application Example



Life Support Note:

Not Intended for Use in Life Support or Life Saving Applications

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Absolute Maximum Ratings

| Symbol | Parameter | Value | Units |
|------------|----------------------------------|------------|-------|
| I_{PP} | Peak Current ($t_p=8/20\mu s$) | 2.0 | A |
| T_{OP} | Operating Temperature | -40 to 125 | °C |
| T_{STOR} | Storage Temperature | -55 to 150 | °C |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the component. This is a stress only rating and operation of the component at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics ($T_{OP}=25^\circ C$)

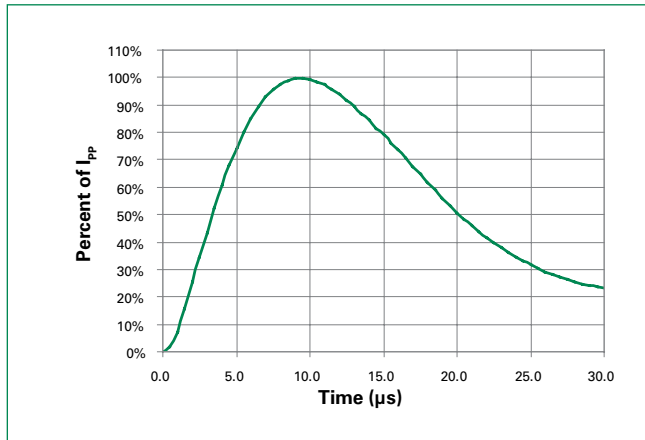
| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|------------------------------------|------------|-------------------------------------|----------|------|-----|----------|
| Reverse Standoff Voltage | V_{RWM} | $I_R \leq 1\mu A$ | | | 60 | V |
| Reverse Leakage Current | I_{LEAK} | $V_R=60V$, Any I/O to GND | | 0.05 | | μA |
| Clamp Voltage ¹ | V_C | $I_{PP}=1A$, $t_p=8/20\mu s$, Fwd | | 81 | | V |
| | | $I_{PP}=2A$, $t_p=8/20\mu s$, Fwd | | 95 | | V |
| Dynamic Resistance ³ | R_{DYN} | TLP, $t_p=100ns$, I/O to GND | | 4 | | Ω |
| ESD Withstand Voltage ¹ | V_{ESD} | IEC 61000-4-2 (Contact) | ± 15 | | | kV |
| | | IEC 61000-4-2 (Air) | ± 20 | | | kV |
| Line Capacitance ^{1,2} | C_L | Reverse Bias=0V; f=1MHz | | 8.5 | | pF |

Note 1: Parameter is guaranteed by design and/or component characterization.

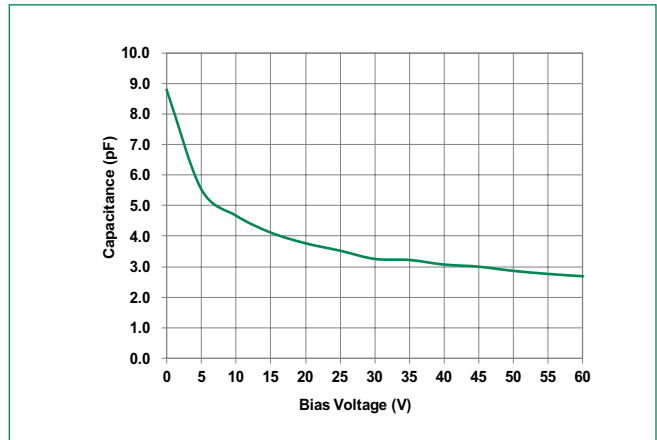
Note 2: Test equipment accuracy $\pm 50\%$.

Note 3: Transmission Line Pulse (TLP) with 100ns width, 2ns rise time, and average window $t_1=70ns$ to $t_2=90ns$

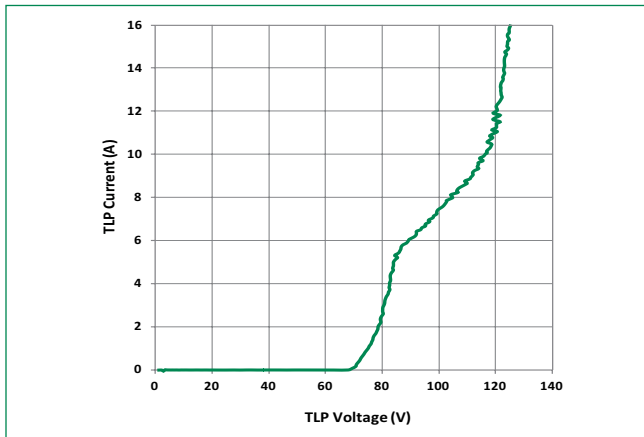
8/20 μs Pulse Waveform



Capacitance vs. Reverse Bias

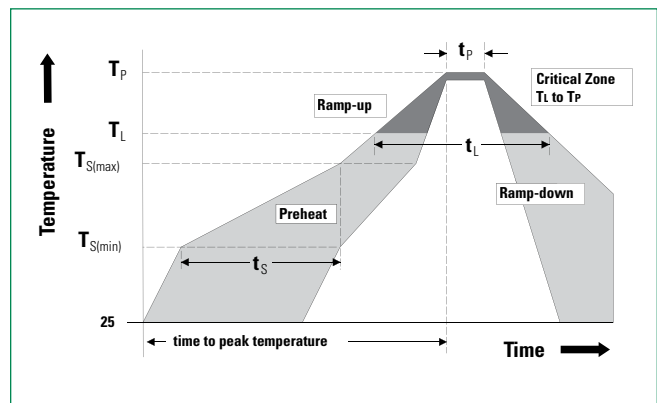


Transmission Line Pulsing (TLP) Plot



Soldering Parameters

| | | |
|--|------------------------------------|-------------------------|
| Reflow Condition | | Pb – Free assembly |
| Pre Heat | - Temperature Min ($T_{s(min)}$) | 150°C |
| | - Temperature Max ($T_{s(max)}$) | 200°C |
| | - Time (min to max) (t_s) | 60 – 180 secs |
| Average ramp up rate (Liquidus) Temp (T_L) to peak | | 3°C/second max |
| $T_{S(max)}$ to T_L - Ramp-up Rate | | 3°C/second max |
| Reflow | - Temperature (T_L) (Liquidus) | 217°C |
| | - Temperature (t_L) | 60 – 150 seconds |
| Peak Temperature (T_p) | | 260 ^{+0/-5} °C |
| Time within 5°C of actual peak Temperature (t_p) | | 20 – 40 seconds |
| Ramp-down Rate | | 6°C/second max |
| Time 25°C to peak Temperature (T_p) | | 8 minutes Max. |
| Do not exceed | | 260°C |



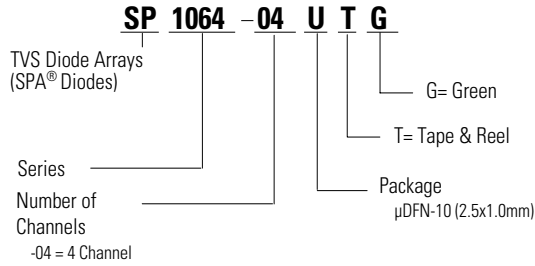
Product Characteristics

| | |
|----------------------------|--|
| Lead Plating | Tin |
| Lead Material | Copper Alloy |
| Lead Coplanarity | 0.0004 inches (0.102mm) |
| Substitute Material | Silicon |
| Body Material | Molded Compound |
| Flammability | UL Recognized compound meeting flammability rating V-0 |

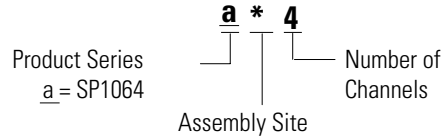
Ordering Information

| Part Number | Package | Min. Order Qty. |
|--------------|---------|-----------------|
| SP1064-04UTG | μDFN-10 | 3000 |

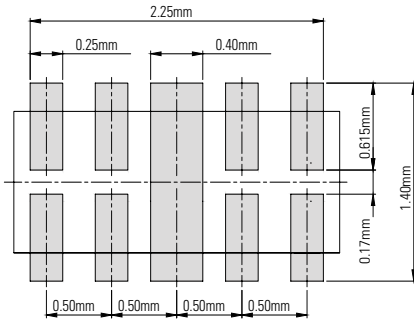
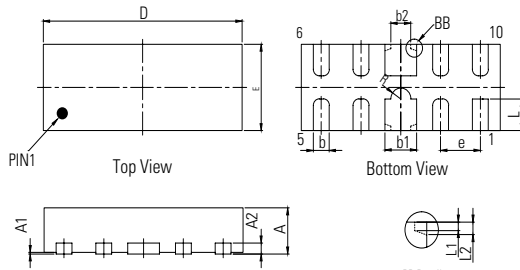
Part Numbering System



Part Marking System



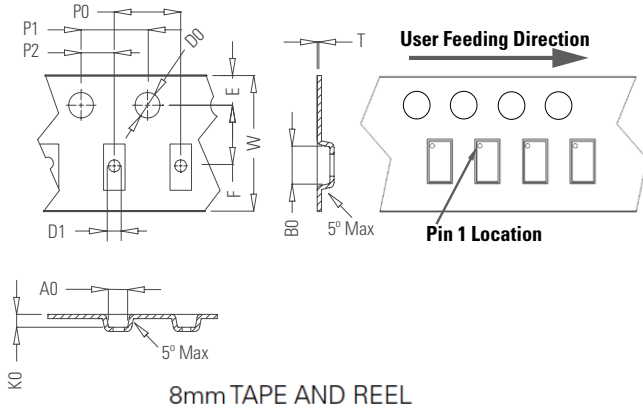
Package Dimensions — μDFN-10 (2.5x1.0x0.5mm)



Recommended Soldering Layout

| Package | μDFN-10 (2.5x1.0x0.5mm) | | | |
|-----------|-------------------------|------|----------------------|-------|
| JEDEC | MO-229 | | | |
| Symbol | Millimeters | | Inches | |
| | Min | Max | Min | Max |
| A | 0.45 | 0.55 | 0.018 | 0.022 |
| A1 | 0.00 | 0.05 | 0.000 | 0.002 |
| A2 | 0.10 | 0.20 | 0.004 | 0.008 |
| b | 0.15 | 0.25 | 0.006 | 0.010 |
| b1 | 0.35 | 0.45 | 0.014 | 0.018 |
| b2 | 0.25 REF (Optional) | | 0.010 REF (Optional) | |
| D | 2.40 | 2.60 | 0.098 | 0.106 |
| E | 0.90 | 1.10 | 0.037 | 0.045 |
| L | 0.30 | 0.45 | 0.012 | 0.018 |
| e | 0.50 BSC | | 0.020 BSC | |
| R | 0.05 | 0.15 | 0.002 | 0.006 |

Embossed Carrier Tape & Reel Specification — μ DFN-10



| Package | μ DFN-10 (2.5x1.0x0.5mm) |
|---------|------------------------------|
| Symbol | Millimeters |
| A0 | 1.30 +/- 0.10 |
| B0 | 2.83 +/- 0.10 |
| D0 | \varnothing 1.50 + 0.10 |
| D1 | \varnothing 1.00 + 0.25 |
| E | 1.75 +/- 0.10 |
| F | 3.50 +/- 0.05 |
| K0 | 0.65 +/- 0.10 |
| P0 | 4.00 +/- 0.10 |
| P1 | 4.00 +/- 0.10 |
| P2 | 2.00 +/- 0.05 |
| T | 0.254 +/- 0.02 |
| W | 8.00 + 0.30 /- 0.10 |

