**Description**

The SRDA3.3 integrates low capacitance rail-to-rail diodes with an additional zener diode to protect I/O pins against ESD and lightning induced surge events. This device can safely absorb up to 35A per IEC61000-4-5 (tp=8/20μs) without performance degradation and a minimum ±30kV ESD per IEC61000-4-2 international standard. Its low loading capacitance makes it ideal for high-speed interface protection.

**Features**

- Lightning protection, IEC61000-4-5, 35A (8/20μs)
- EFT, IEC61000-4-4, 50A (5/50ns)
- ESD, IEC61000-4-2, ±30kV contact, ±30kV air
- Low clamping voltage
- Low leakage current
- SOIC-8 surface mount package (JEDEC MS-012)

**Applications**

- Tertiary (IC Side) Protection:
  - T1/E1/T3/E3
  - HDSL/SDSL
  - Ethernet
- RS232, RS485
- Video Line Protection
- Security Cameras
- Storage DVRs
- Network Equipment
- Instrumentation, Medical Equipment

**Application Example**

The SRDA3.3 Series 8pF 35A Diode Array provides protection against ESD and lightning induced surge events. It is suitable for use in various applications such as T1/E1/T3/E3 interface protection, HDSL/SDSL, Ethernet, RS232, RS485, and more. The device can safely absorb up to 35A without performance degradation and can handle ±30kV ESD per IEC61000-4-2 international standard. Its low loading capacitance makes it ideal for high-speed interface protection.
Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak Pulse Power (8/20μs)</td>
<td>$P_{pp}$</td>
<td>600</td>
<td>W</td>
</tr>
<tr>
<td>Peak Pulse Current (8/20μs)</td>
<td>$I_{pm}$</td>
<td>35</td>
<td>A</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>$T_{op}$</td>
<td>-40 to 125</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>$T_{STOR}$</td>
<td>-55 to 150</td>
<td>°C</td>
</tr>
</tbody>
</table>

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics ($T_{op} = 25°C$)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reverse Stand-Off Voltage</td>
<td>$V_{RWM}$</td>
<td>$I_{f} \leq 1$μA</td>
<td>-</td>
<td>-</td>
<td>3.3</td>
<td>V</td>
</tr>
<tr>
<td>Reverse Breakdown Voltage</td>
<td>$V_{BR}$</td>
<td>$I_{f} \leq 2$μA</td>
<td>3.5</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Snap Back Voltage</td>
<td>$V_{SB}$</td>
<td>$I_{f} = 50$mA</td>
<td>2.9</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Reverse Leakage Current</td>
<td>$I_{R}$</td>
<td>$V_{f} = 3.3$V</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>μA</td>
</tr>
<tr>
<td>Clamping Voltage, Line-Ground</td>
<td>$V_{C}$</td>
<td>$I_{f} \leq 1$A, $t_{p} = 8/20$ μs</td>
<td>-</td>
<td>5.7</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Clamping Voltage, Line-Ground</td>
<td>$V_{C}$</td>
<td>$I_{f} \leq 10$A, $t_{p} = 8/20$ μs</td>
<td>-</td>
<td>10.1</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Clamping Voltage, Line-Ground</td>
<td>$V_{C}$</td>
<td>$I_{f} \leq 30$A, $t_{p} = 8/20$ μs</td>
<td>-</td>
<td>17.7</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Dynamic Resistance, Line-Ground</td>
<td>$R_{DYN}$</td>
<td>$(V_{C2} - V_{C1})/(I_{PP2} - I_{PP1})$</td>
<td>-</td>
<td>0.5</td>
<td>-</td>
<td>Ω</td>
</tr>
<tr>
<td>ESD Withstand Voltage</td>
<td>$V_{ESD}$</td>
<td>IEC61000-4-2 (Contact Discharge)</td>
<td>±30</td>
<td>-</td>
<td>-</td>
<td>kV</td>
</tr>
<tr>
<td>Diode Capacitance</td>
<td>$C_{O-I/O}$</td>
<td>Reverse Bias=0V</td>
<td>-</td>
<td>4.0</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td>$C_{O-GND}$</td>
<td>Reverse Bias=0V</td>
<td>-</td>
<td>8.0</td>
<td>-</td>
<td>pF</td>
</tr>
</tbody>
</table>

1 Parameter is guaranteed by design and/or device characterization.

Normalized Capacitance vs. Bias Voltage

Non-Repetitive Peak Pulse Power vs. Pulse Time
Clamping Voltage vs. \( I_{PP} \)

- **Clamping Voltage** \( V_C \) (V)
  - 20
  - 10
  - 2
  - 1
  - 0

- **Peak Pulse Current** \( I_{PP} \) (A)
  - 5
  - 15
  - 25
  - 30
  - 35

Power Derating Curve

- **% of Rated Power or \( I_{PP} \)**
  - 110
  - 100
  - 90
  - 80
  - 70
  - 60
  - 50
  - 40
  - 30
  - 20
  - 10

- **Ambient Temperature** \( T_A \) (°C)
  - 0
  - 25
  - 50
  - 75
  - 100
  - 125
  - 150

Pulse Waveform

- **Percent of \( I_{PP} \)**
  - 110%
  - 100%
  - 90%
  - 80%
  - 70%
  - 60%
  - 50%
  - 40%
  - 30%
  - 20%
  - 10%
  - 0%

- **Time** (μs)
  - 0.0
  - 5.0
  - 10.0
  - 15.0
  - 20.0
  - 25.0
  - 30.0

Product Characteristics

- **Lead Plating**: Matte Tin
- **Lead Material**: Copper Alloy
- **Lead Coplanarity**: 0.0004 inches (0.102mm)
- **Substitute Material**: Silicon
- **Body Material**: Molded Epoxy
- **Flammability**: UL 94 V-0

Notes:
1. All dimensions are in millimeters.
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.

Soldering Parameters

- **Reflow Condition**: Pb – Free assembly
- **Pre Heat**
  - Temperature Min \( T_{S(min)} \): 150°C
  - Temperature Max \( T_{S(max)} \): 200°C
  - Time (min to max) \( t_s \): 60 – 180 secs
- **Average ramp up rate (Liquidus) Temp \( T_L \) to peak**
  - 3°C/second max
- **\( T_{S(max)} \) to \( T_L \) - Ramp-up Rate**
  - 3°C/second max
- **Reflow**
  - Temperature \( T_L \) (Liquidus)
    - 217°C
  - Temperature \( T_f \)
    - 60 – 150 seconds
- **Peak Temperature \( T_P \)**
  - 260°C
- **Time 5°C of actual peak Temperature \( t_{f} \)**
  - 20 – 40 seconds
- **Ramp-down Rate**
  - 6°C/second max
- **Time 25°C to peak Temperature \( T_P \)**
  - 8 minutes Max.
- **Do not exceed**
  - 260°C
**Part Numbering System**

SRDA 3.3 - 4 BTG

- **G**: Green
- **T**: Tape & Reel
- **B**: SOIC-8
- **4**: 4 Channels

**Ordering Information**

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package</th>
<th>Marking</th>
<th>Min. Order Qty.</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRDA3.3-4BTG</td>
<td>SOIC-8</td>
<td>SRDA3.3</td>
<td>2500</td>
</tr>
</tbody>
</table>

**Package Dimensions — Mechanical Drawings and Recommended Solder Pad Outline**

- **JEDEC MS-012**
- **Dimensions**
  - **A**: 1.35 - 1.75 mm, 0.053 - 0.069 inches
  - **A1**: 0.10 - 0.25 mm, 0.004 - 0.010 inches
  - **A2**: 1.25 - 1.65 mm, 0.050 - 0.065 inches
  - **B**: 0.31 - 0.51 mm, 0.012 - 0.020 inches
  - **c**: 0.17 - 0.25 mm, 0.007 - 0.010 inches
  - **D**: 4.80 - 5.00 mm, 0.189 - 0.200 inches
  - **E**: 5.80 - 6.20 mm, 0.228 - 0.244 inches
  - **E1**: 3.80 - 4.00 mm, 0.150 - 0.157 inches
  - **e**: 1.27 BSC
  - **L**: 0.40 - 1.27 mm, 0.016 - 0.050 inches

**Recommended Soldering Pad Outline (Reference Only)**

**Embossed Carrier Tape & Reel Specification — SOIC Package**

- **Dimensions**
  - **E**: 1.65 - 1.85 mm, 0.065 - 0.073 inches
  - **F**: 5.4 - 5.6 mm, 0.213 - 0.220 inches
  - **P2**: 1.95 - 2.05 mm, 0.077 - 0.081 inches
  - **D**: 1.5 - 1.6 mm, 0.059 - 0.063 inches
  - **D1**: 1.50 Min, 0.059 Min
  - **P0**: 3.9 - 4.1 mm, 0.154 - 0.161 inches
  - **10P0**: 40.0 +/- 0.20 mm, 1.574 +/- 0.008 inches
  - **W**: 11.9 - 12.1 mm, 0.468 - 0.476 inches
  - **P**: 7.9 - 8.1 mm, 0.311 - 0.319 inches
  - **A0**: 6.3 - 6.5 mm, 0.248 - 0.256 inches
  - **B0**: 5.1 - 5.3 mm, 0.2 - 0.209 inches
  - **K0**: 2 - 2.2 mm, 0.079 - 0.087 inches
  - **t**: 0.30 +/- 0.05 mm, 0.012 +/- 0.002 inches